Modeling DC-DC Converter Efficiency and Power Management in Ultra Low Power Systems

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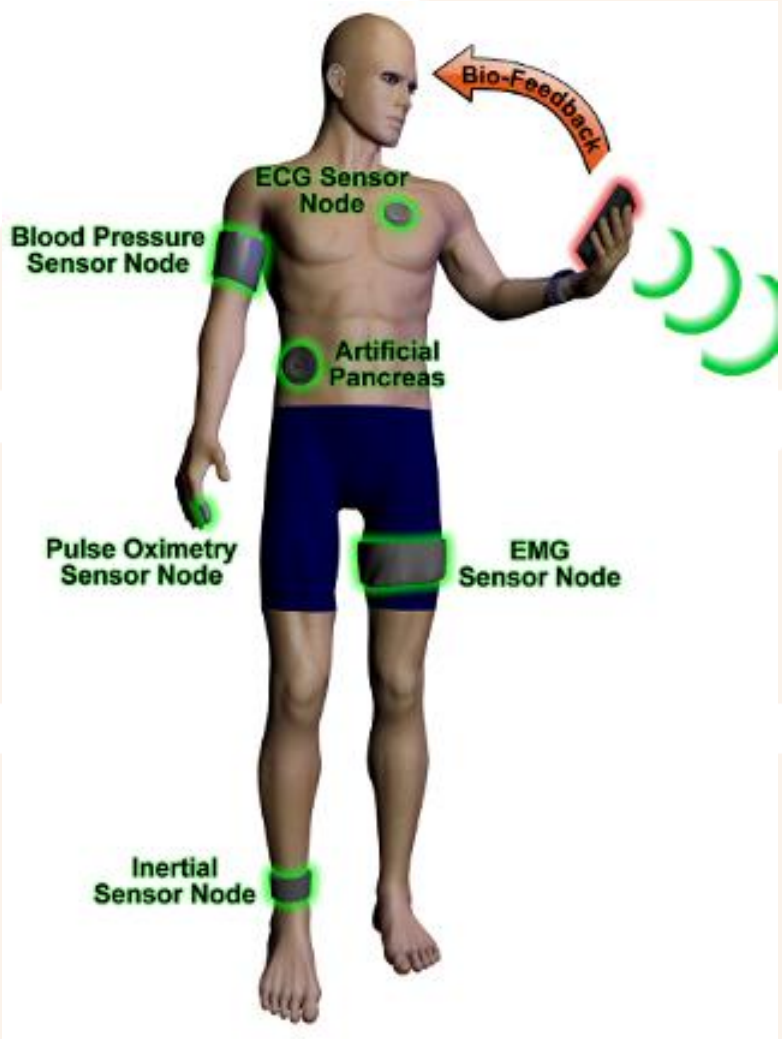
Robust Low Power VLSI

Ultra Low Power SoCs (like BSN)



Features

- Comprehensive and unobtrusive human health monitoring.

Needs

- Small Form Factor, light wait
- Long battery life/ run on harvested energy
- Low cost.
- Efficient Power Management

Ex :- Fan Zhang et al. ”A batteryless 19μW MICS/ISM-band energy harvesting body area sensor node SoC.” *ISSCC 2012*

Power Management Techniques

- Power Management techniques are commonly employed to increase the life-time of ULP system ex. DVFS, Clock gating, Power gating etc.
- These techniques have an impact on the efficiency of DC-DC converter, ex. DVFS changes load and output voltage of the converter.
- The benefits of these techniques cannot be established in isolation from DC-DC converter.
- In this talk we present a model and a framework to correctly study the benefits of Power Management techniques in conjunction with DC-DC converter

Outline

- **Model of DC-DC converter**
- Framework to obtain energy cost
- Block level Power Management Technique
- Results

Model of a DC-DC converter

- Efficiency of DC-DC converter decreases at both light load and heavy load (considering PWM scheme)

$$P_{LOSS} \propto aI_L + b/I_L$$

- Efficiency peaks at a given load and decrease on either side.
- We model Efficiency with load current as

$$\eta i = \eta 2 - (\eta 2 - \eta 1) * (log(I_L/I_O))^2/4 \quad \ldots\ldots\ldots\ldots\ldots\ldots (i)$$

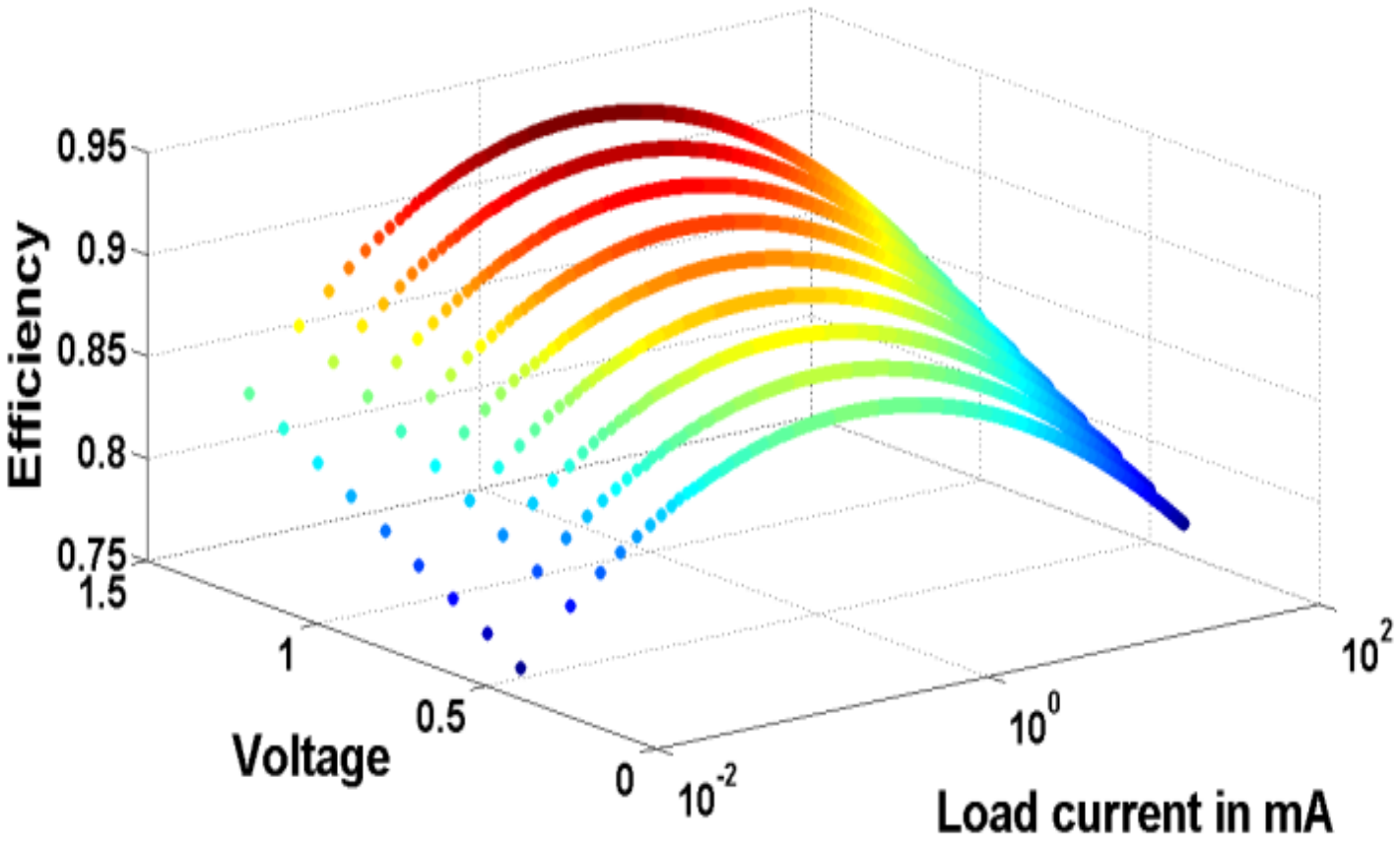
Where η2 is the peak efficiency occurring at load Io, η1 is the minimum efficiency at a given load.

- For a buck converter, the efficiency of a converter decreases linearly as the output voltage decreases

$$\eta v = \eta 1 + m * (V - Vmin)$$

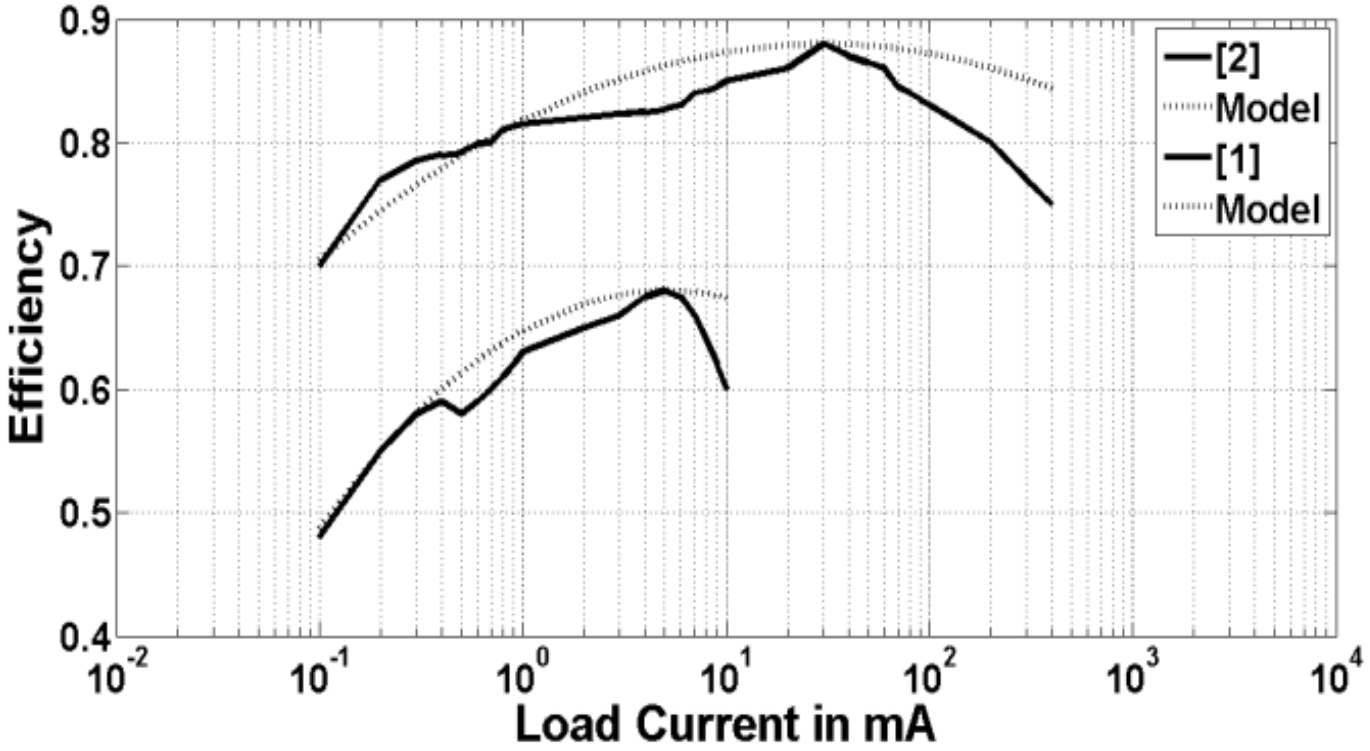
Model of a DC-DC converter

$\eta = \eta v * \eta i$



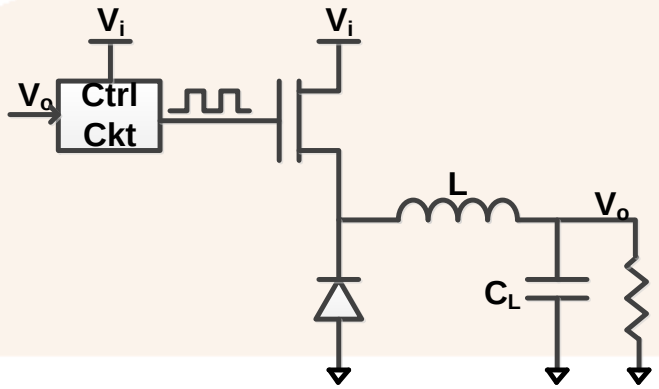
Comparison

We compare the model with the converters reported in literature



Proposed Model was close to 90% accurate

Additional Energy Overheads



- Settling Time

  $\Delta T = T/V * \Delta V$

  Where T is the settling time of the converter when output voltage is charged to V from ground.

- Rail Switching Energy: Charging and discharging CL entails loss, When Vo changes to V1 from V2

  *Ec=Vin*CL*{(max(V1-V2,0)}* ,

  Work is not done by Vi when V1 is lower than V2.

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Framework to calculate Energy cost

- Total Energy is broken down into two components, operating cost and conversion cost.

Operating cost:

$$Eop=V1*i1*(T1+\Delta T1)/\eta 1+V2*i2*(T2+\Delta T2)/\eta 2+\ldots$$

Conversion cost *:*

$$Ec=Vin*CL*\{(max(V1-V2,0)+max(V2-V3,0)\ldots\}$$

Total Energy:

$$Eop+Ec$$

Outline

- Model of DC-DC converter
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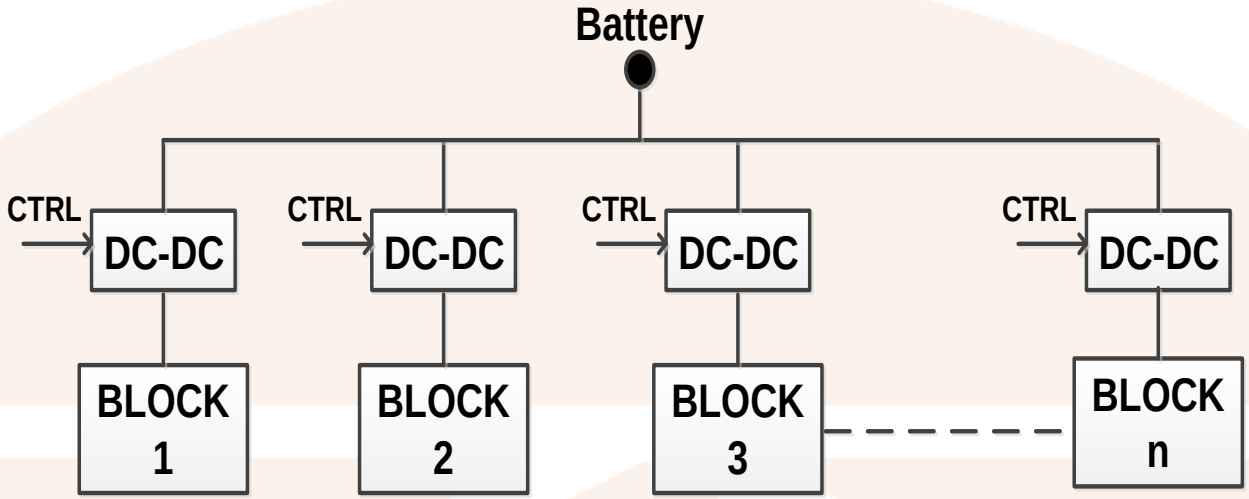
Block Level DVFS



- Idealized implementation to study the benefits of DVFS at block level.
- Each block has a dedicated VDD and implements its own DVFS.
- Each block is implemented as chain of inverters with different depth

Block Level DVFS

VDD	Load	Time of operation
V1 V	i1 uA	T1+ΔT1 uS
V2 V	i2 uA	T2+ΔT2 uS
….	….	…..

Optimal condition for a block

VDD	Load	Time of operation
0.9 V	100uA	6+2 uS
1.2 V	900uA	5+3 uS
….	….	…..

Example Table

- For each block a table for operating condition can be obtained as shown, illustrating load and output voltages etc.
- Energy overhead can be obtained as

  $Eop=V1*i1*(T1+\Delta T1)/\eta 1+V2*i2*(T2+\Delta T2)/\eta 2+\ldots$

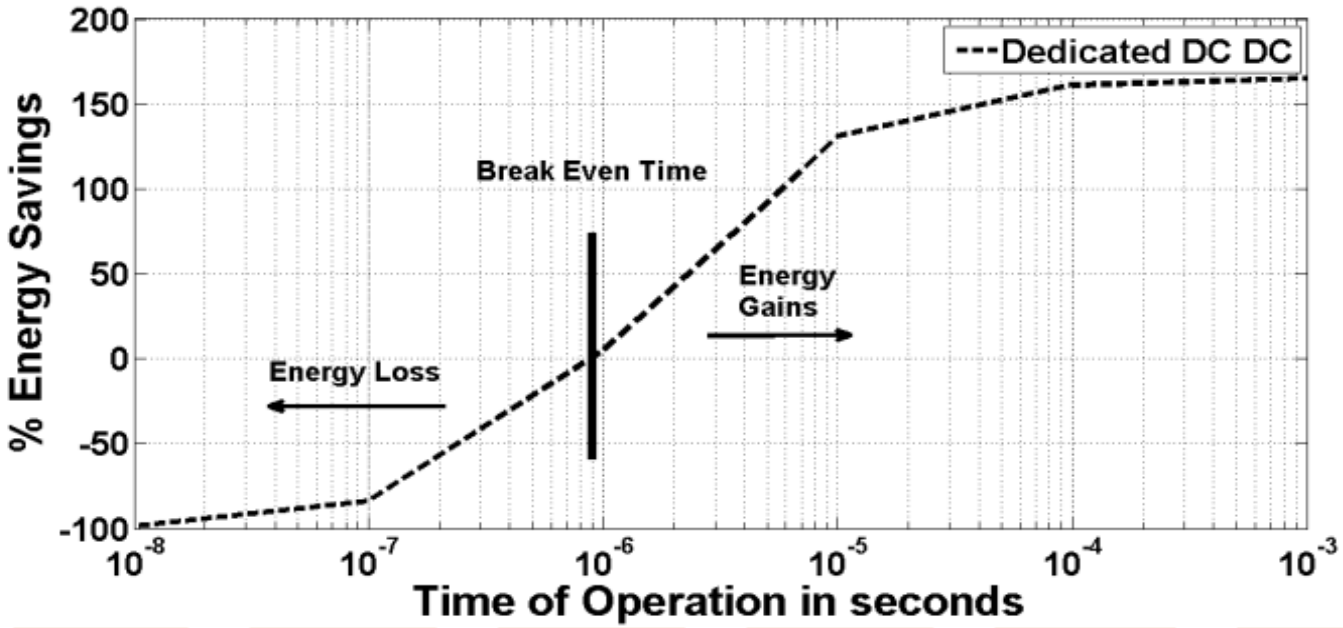
  Eop is the operating energy and ŋ is calculated using (iii)

  $Ec=Vin*CL*\{(max(V1-V2,0)+max(V2-V3,0)\ldots\}$

  $Total\ Energy= Eop+Ec.$

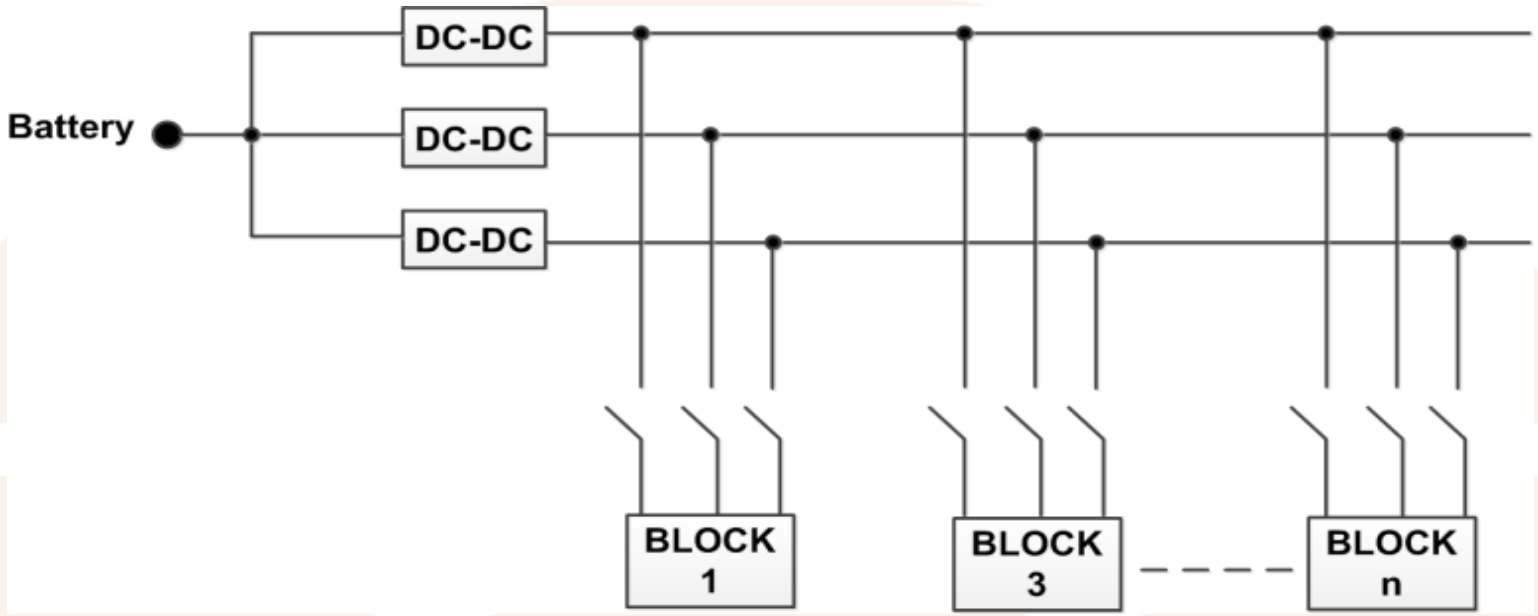
Comparison

We compare the model with the case where no power Management is implemented using the model



- Figure shows that no energy benefits can be realized if rail switches at faster rate than 1µs.
- >2.5x energy benefits can be realized using DVFS

PDVS



- Panoptic Dynamic Voltage scaling has been used to implement block level DVFS [3].
- In PDVS a block can dither between two rails to obtain an ideal operating condition
- It does not require rail to change and saves overheads

PDVS Operating Condition

VDD	Load			T_{op}
	0.4V	0.8V	1.2V	
V1 V	i11 uA	0	0	T11
V1 V	0	i12 uA	0	T12
V2 V	0	i21 uA	0	T21
V2 V	0	0	i22 uA	T21
….	….	…..	…..	…..

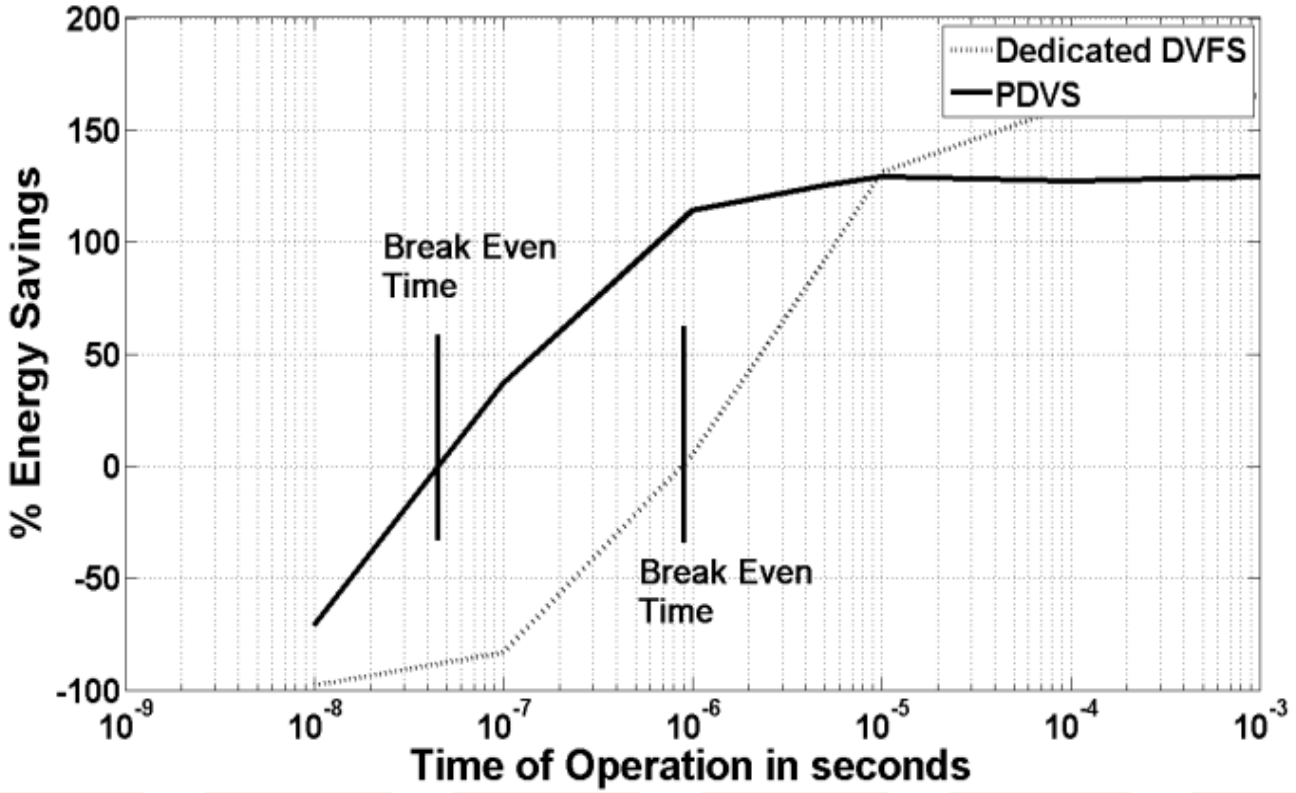
- Operating table for each block is broken down in PDVS, like shown above
- On each power supply we get the following condition,

Load			dT_{OP}
0.4V	0.8V	1.2V	
$i_1(t)$	$i_2(t)$	$i_3(t)$	1e-9

$$Eop= 0.4*\int i1(t) /\eta1(i1)* dt+0.8*\int i2(t) /\eta2(i2)* dt+1.2*\int i3(t) /\eta2(i2)* dt$$

Result

We compare PDVS with block level DVFS using the model



PDVS can start realizing energy benefits at VDD switching time of 10ns, however maximum energy benefit is lower because PDVS sees wider load variation

Conclusion

- A power model which can accurately predict the behavior of DC-DC converter in a dynamic environment has been presented.
- The model has been validated and compared with existing literature.
- We use this model to study block level power management techniques for an SOC, ex PDVS.
- The model predicts that there is a break-even time, before the benefit of voltage scaling becomes positive.

Acknowledgement

This work was supported in part by the NSF NERC ASSIST center (EEC-1160483)

References

1. Jinwen Xiao , et. al “A 4-μa quiescent-current buck converter” *JSSC Dec 2004*.
2. Y. Yorozu, et. al. “Electron spectroscopy studies….,” IEEE Transl. J. Magn. Japan, August 1987
3. Yousef Shakhsheer, et al, “A 90nm data flow processor demonstrating… “. *CICC 2011*