Standby Power Reduction Using Dynamic Voltage Scaling and Canary Flip-Flop Structures

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***Abstract*—Lowering V_{DD} during standby mode reduces power by decreasing both voltage and current. Analysis of flip-flop structures shows how low the voltage can scale before destroying the state information. Measurements of a 0.13-μm, dual—V_T test chip show that reducing V_{DD} to near the point where state is lost gives the best power savings. We show that "canary" flip-flops provide a mechanism for observing the proximity to failure for the flip-flops. The canary flip-flops enable closed-loop standby voltage scaling for achieving savings near the optimum. This approach potentially provides over 2× higher savings than an optimal open-loop approach without loss of state.**

***Index Terms*—Canary flip-flop, low power, minimum V_{DD}, standby power reduction, voltage scaling.**

I. Introduction

THE well-known increase in leakage currents with each new process generation has made leakage power a significant part of overall power consumption in both active and standby modes [1]. Although subthreshold leakage dominates for 0.13-μm devices, gate leakage, gate-induced drain leakage (GIDL), and reverse-biased diode leakage are becoming relatively more significant [2]. For energy-constrained systems or circuits with lifetime requirements, leakage reduction is especially important during standby mode. Voltage scaling for standby power reduction was suggested since both subthreshold current and gate current decrease dramatically with V_{DD} (αV^4 for gate leakage) [3]. Lowering V_{DD} thus saves standby power by decreasing both standby current and voltage.

The analysis in this paper assumes that a dynamic power supply can scale its voltage output to the required levels. For simplicity, the overhead of this theoretical supply is ignored. In reality, it would factor into the savings analysis. The existence of dynamic voltage dc–dc converters with high efficiencies over a broad range [4], [5] suggests the feasibility of designing one or more converters to implement this technique.

One existing approach to voltage scaling uses diode stacks together with power gating MOSFETs to pinch in the rail voltages during standby mode [6]. The quantity and sizes of the devices used in the diode stack determine the reduced V_{DD} value and the increased V_{SS} value during standby mode. In order to preserve state, the total voltage drop across the circuits (V_{DS}) is only decreased by about 40%. This paper examines the potential power savings from lowering the supply voltage and shows that greater reduction of V_{DD} is preferable. At the same time, careful treatment of a circuit's storage elements will allow state preservation.

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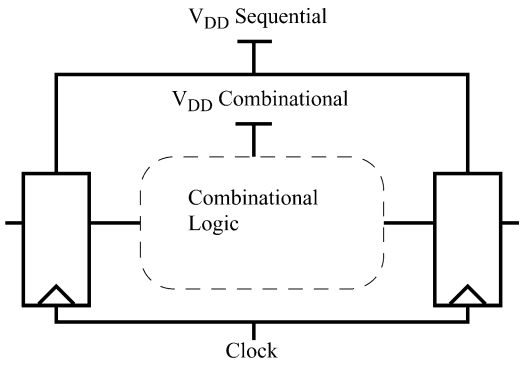

Fig. 1. Theoretically optimal savings using two power supplies. Combinational supply gated (i.e., $V_{DD} = 0$) during sleep, and sequential supply scales to V_{DD} optimal (lowest voltage which preserves state).

II. Potential Power Savings From Lowering V_{DD}

This section describes what power savings are possible from reducing V_{DD}. The standby power supply for a circuit can be gated (i.e., $V_{DD} = 0$) to draw zero power, but the circuit will lose all of its state. If two power supplies are separately routed to combinational and to sequential logic, the combinational logic supply voltage can be gated while sequential elements use a different power supply (Fig. 1). Separating the power supplies provides immediate power savings because all of the combinational logic draws no power during standby. The sequential supply may also decrease during standby to save power, but it must remain above some minimum point to hold its state. The optimal V_{DD} for power savings using this technique is the lowest voltage for which the circuit retains state. Separating the power supplies to the combinational and sequential logic may be impractical because of overhead or routing costs. The rest of the paper assumes that the entire circuit under test shares the same power supply, although the results are applicable to the case where two supplies are used.

The potential savings from lowering the standby voltage supply come from two factors. The decreasing voltage itself provides a linear reduction in power. For a 0.13-μm process with nominal V_{DD} of 1.2 V, voltage scaling to 300 mV reduces the voltage contribution to power by 4×. The current component of power also decreases. The BSIM2 model for subthreshold current incorporates a linearized body coefficient,

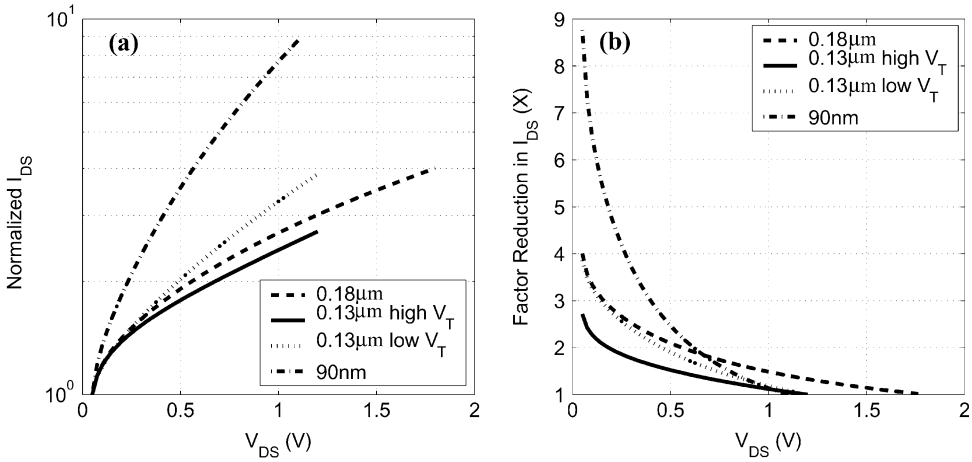

Fig. 2. Impact of DIBL on power savings for NFETs with $V_{GS} = 0$ in three technologies: (a) normalized I_{DS} versus V_{DS} and (b) I_{DS} reduction versus V_{DS}. PFET characteristics are similar.

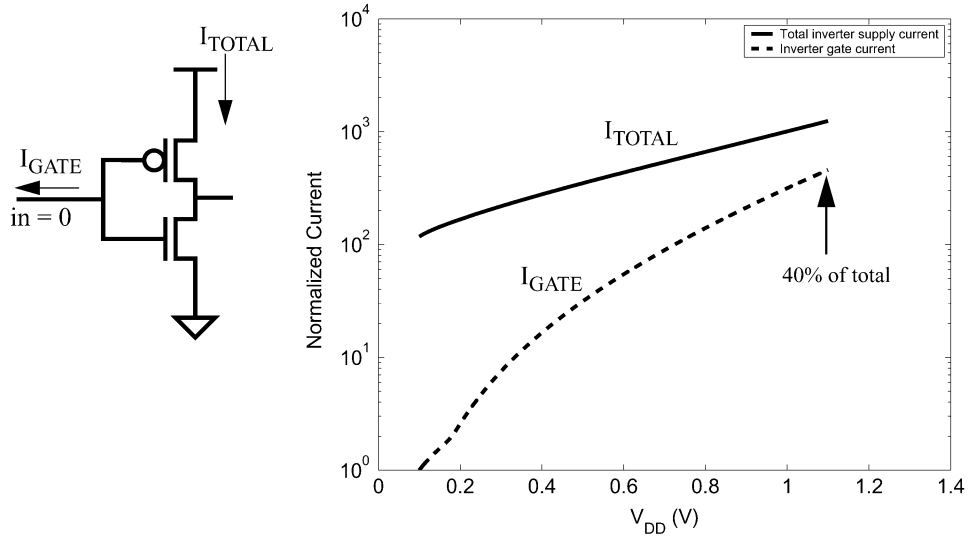

Fig. 3. Contribution of gate leakage to total inverter off current in 90-nm process (in $= 0$). Gate current is 40% of total current at nominal V_{DD}, but diminishes rapidly as V_{DD} scales.

γ, and linearized drain-induced barrier lowering (DIBL) parameter, η, to its subthreshold current equation [7], [8]:

$$I_{subth} = I_o \cdot e^{\frac{V_{GS}-V_{T0}-\gamma V_{SB}+\eta V_{DS}}{n \cdot V_{th}}} \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right) \quad (1)$$

$$\text{where } I_o = \mu_o C_{ox} \frac{W}{L_{eff}} \left(\frac{kT}{q}\right)^2 e^{1.8}. \quad (2)$$

Equation (1) indicates that lowering V_{DD} will produce a corresponding exponential reduction in subthreshold current resulting from DIBL. At very low V_{DS} values, the parenthetical term produces a more pronounced rolloff in subthreshold current. The amount of total power savings from voltage scaling depends on the DIBL factor. Fig. 2 plots normalized I_{DS} versus V_{DS} for $V_{GS} = 0$ in three commercial technologies. The plots show that the DIBL effect reduces current by roughly $2\times$ to $4\times$ when V_{DD} scales from its nominal value to about 300 mV. The rolloff in current at lower V_{DD} corresponds to the parenthetical term in (1). Thus, the total theoretical power savings are on the order of $8\times$ to $16\times$ for scaling down to the 300-mV range. Dramatic additional savings arise from the rolloff in subthreshold current at even lower supply voltages.

Gate leakage comprises an appreciable percentage of total leakage in deeply scaled processes. Fig. 3 shows total current and gate current for an inverter with its input at 0 in a 90-nm process. At V_{DD} nominal of 1.1 V, 40% of the total leakage is gate leakage. The figure shows that this component rapidly diminishes with V_{DD} and quickly becomes insignificant. Thus, voltage scaling provides even more power savings for processes with gate leakage by eliminating this component of leakage at the scaled supply value.

III. Saving State at Low V_{DD}

A. Master–Slave Flip-Flops

Since the largest theoretical power savings come from scaling V_{DD} down as low as possible, knowing the failure point for sequential devices in the circuit is imperative. This section examines the failure point for generic master–slave flip-flops

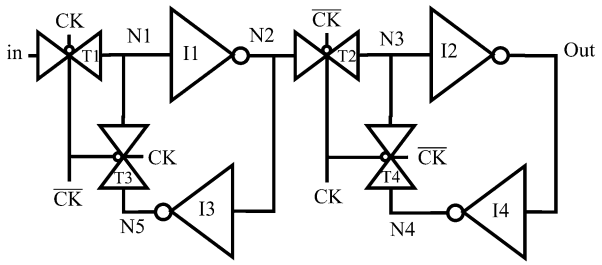

Fig. 4. Schematic of master-slave flip-flop (MSFF).

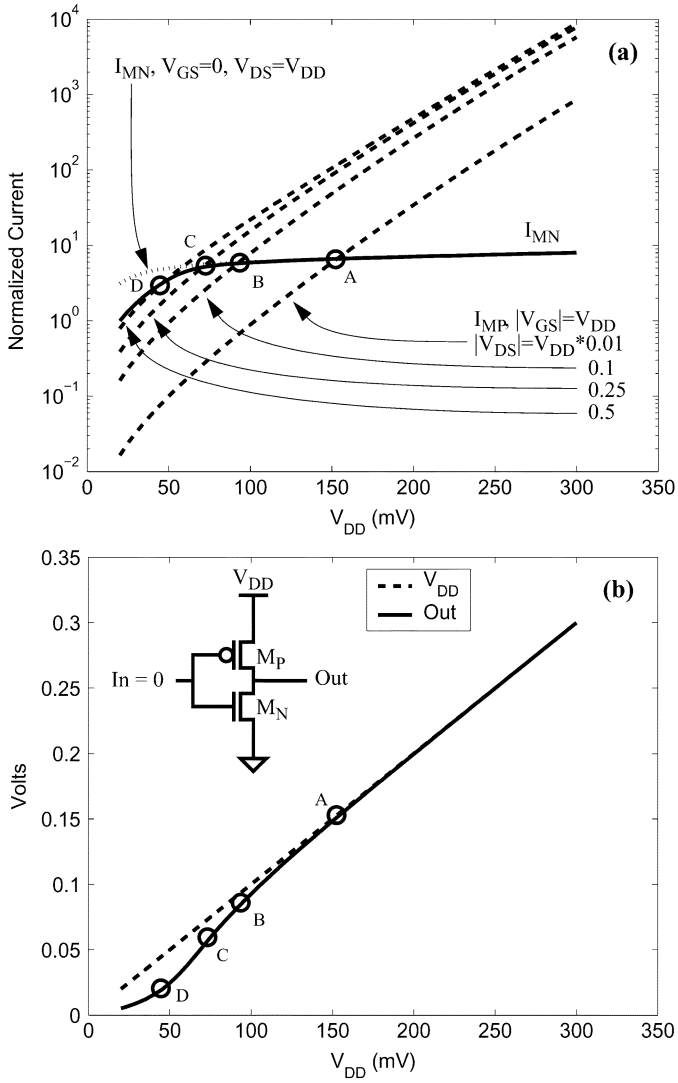

Fig. 5. Analysis of inverter with scaled V_{DD}. Output voltage drops below V_{DD} because reduced $|V_{GS}|$ for M_P forces $|V_{DS}|$ for M_P to increase to supply the current through $M_N (I_{MN})$. (a) shows currents and (b) shows the output voltage versus V_{DD}.

(MSFFs). Fig. 4 shows the schematic of an MSFF. When the flip-flop holds data, CK is high, so Tl and T4 are off, and the back-to-back inverters I1 and I3 store the flip-flop state. The rest of this section explores the minimum voltage required for an MSFF to hold its state.

Observing the behavior of a single inverter with V_{DD} scaling adds insight to the analysis. Fig. 5 shows the output voltage [Out in (b)] and the current [I_{MN} in (a)] of an inverter as V_{DD}

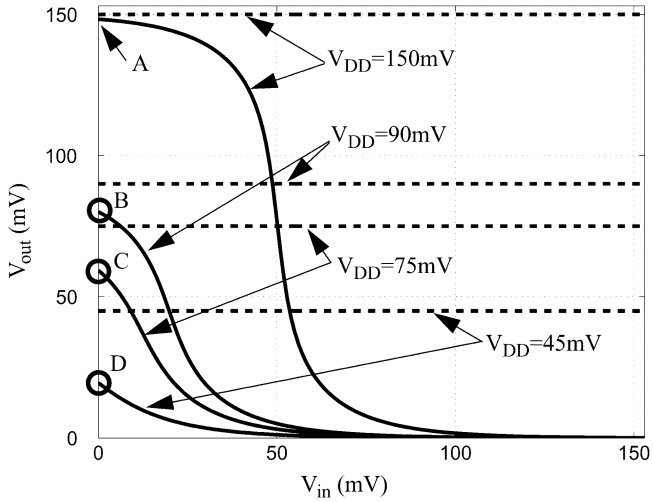

Fig. 6. VTCs of inverter at labeled points from Fig. 5.

scales. The output voltage clearly differs from the power supply value starting near 150 mV. When $V_{DD} > |V_{Tp}|$, then M_P remains in the triode region. Once V_{DD} drops below the threshold voltage, (1) describes its behavior. Substituting into (1) gives the subthreshold current for M_N and M_P (using $|V_{GS}|$ and $|V_{DS}|$) based on V_{DD}:

$$I_{M_N} = I_{oM_N} \cdot e^{\frac{-V_{T0n}+\eta_n V_{out}}{n \cdot V_{th}}} \cdot \left(1 - e^{-\frac{V_{out}}{V_{th}}}\right) \tag{3}$$

$$I_{M_P} = I_{oM_P} \cdot e^{\frac{V_{DD}-|V_{T0P}|+\eta_P(V_{DD}-V_{out})}{n \cdot V_{th}}} \cdot \left(1 - e^{-\frac{V_{DD}-V_{out}}{V_{th}}}\right). \tag{4}$$

When V_{DD} is near $|V_{Tp}|$ then $|V_{GS}| = V_{DD}$ for M_P and $V_{GS} = 0$ for M_N. Since the current through both devices must be the same, then $|V_{DS}|$ for M_P must remain small so that the parenthetical term in (4) offsets the exponential increase in current from the larger $|V_{GS}|$. As V_{DD} decreases further, it does not heavily impact current through M_N, c.f. (3). On the other hand, the first exponential term in (4) continues to drop quickly. This is illustrated in Fig. 5(a). The dashed lines plot current through M_P assuming $|V_{GS}| = V_{DD}$ and $|V_{DS}|$ is a fixed fraction of V_{DD}. For these example cases, the crossover points with I_{MN} are labeled in Fig. 5(a), and the corresponding output voltages are labeled in Fig. 5(b). The plot shows that $|V_{DS}|$ of M_P must increase in order for its current to balance with I_{MN} causing V_{out} to drop below V_{DD} by an appreciable amount. The output voltage plot in Fig. 5(b) is essentially a snapshot of the voltage transfer curves (VTCs) of the inverter for an input voltage of 0. To illustrate this, the VTCs at the labeled points are shown in Fig. 6. The labeled points in Fig. 6 again show the voltage droop for an input voltage of 0 (V_{OH} decreases below V_{DD}). Also, the inverter gain decreases at low values of V_{DD}, pushing V_{IL} to the left on the VTC. Another way to explain the output voltage droop is that the nonlinear resistance of M_P starts off much less than that of M_N, which is roughly constant with V_{DD}. But the resistance of M_P becomes significant at some point when V_{DD} has dropped far enough (about 150 mV in Fig. 5), and the resulting voltage divider effect causes the output voltage to drop away from V_{DD}. The inverter also shows how sizing can affect

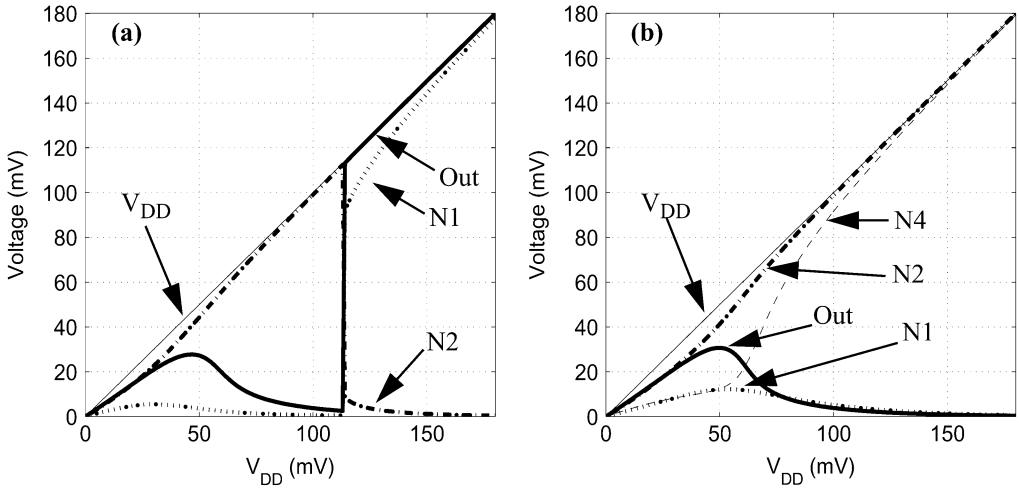

Fig. 7. DC sweep of unbalanced MSFF in 0.18-μm technology showing two types of failure: (a) fails to hold a '1' because state switches, and (b) fails to hold a '0' because output stage switches.

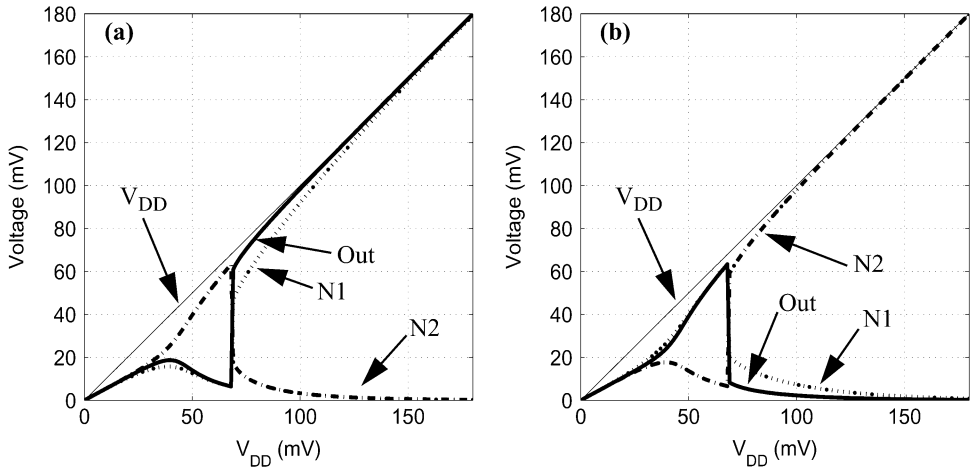

Fig. 8. DC sweep of MSFF sized for balanced failure points: (a) fails to hold a '1' and (b) fails to hold a '0'.

the failure point. Increasing the size of PMOS devices moves the dashed lines in Fig. 5(a) up so that the voltage droop in Fig. 5(b) occurs at lower V_{DD}.

Fig. 7 shows a dc sweep of V_{DD} for a 0.18-μm MSFF with inverters I3 and I4 minimum sized and the critical path elements sized for equal rise and fall times. The flip-flop can fail because the drooping voltages in the back-to-back inverters cause the state to switch, as in Fig. 7(a). In this plot, the MSFF is holding a logical one, and *in* is 0 to show the worst-case where leakage through T1 acts to degrade the voltage at Nl even further. At a V_{DD} of 120 mV, the voltage at N2 has risen to the V_{IL} point of I3, so the gain of I1 and I3 causes the state to transition. Fig. 7(b) shows the same flip-flop holding a zero ($in =$ '1'). In this case, the state never transitions, but the voltages at nodes N2 and N1 converge, and the output stage switches. It has been shown that the magnitude of gain for inverters must remain above one for bistable operation in digital circuits [10], and this constraint imposes a theoretical limit on the lowest supply voltage for back-to-back inverters to hold their state [11]. If the gain drops below one, then both nodes will converge to a single value. Although this does not occur for the unbalanced MSFF in Fig. 7(b), the reduced voltage at N2 causes the output stage to switch, as shown by the rise in *Out* and fall in N4 at 60 mV. Increasing the size of the PMOS in I1 holds nodes N2 and N3 closer to V_{DD} and enhances the ability of the flip-flop to hold the zero. At the same time, this sizing change will degrade the ability of the flip-flop to hold a logical one because I1 will be less suited to hold nodes N2 and N3 at zero. Changing the sizes of the inverters to improve holding one state always degrades the ability to hold the other state. Balancing the sizes in the MSFF allows it to hold either state to below 70 mV in the worst case, as shown in Fig. 8.

B. Leakage Feedback Flip-Flip

The previous section described data retention for MSFFs. Similar analysis can apply to other sequential devices as well. This section examines the leakage feedback flip-flop (LFBFF) [9]. The LFBFF is a multi-threshold CMOS (MTCMOS) storage device that retains its state even during sleep mode by selectively maintaining an active path to power or ground. MTCMOS logic uses high V_T devices as power gating switches to reduce leakage current during sleep mode.

Fig. 9 shows a schematic of the LFBFF holding a logical one in sleep mode. As with the MSFF, the logical one nodes are

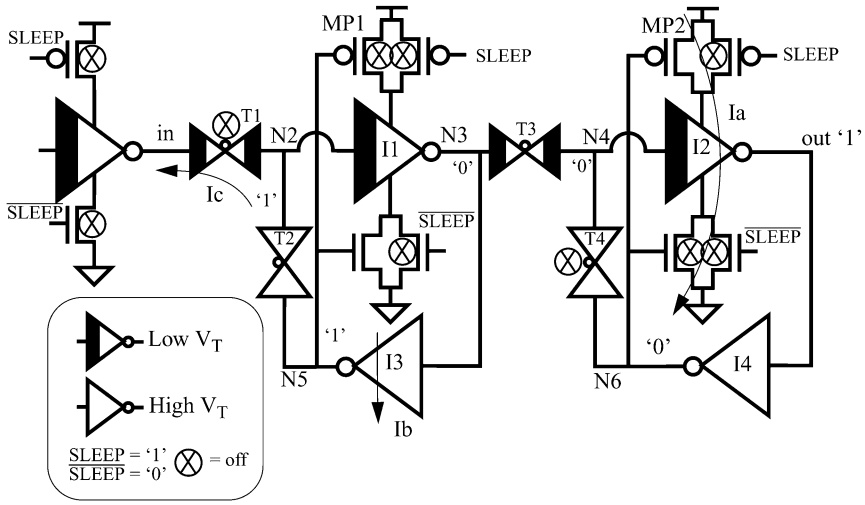

Fig. 9. Schematic of LFBFF in standby (sleep) mode.

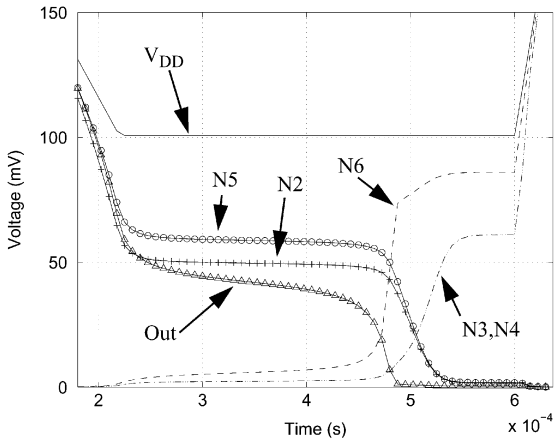

Fig. 10. Simulation of minimum sized LFBFF failing to hold a one at $V_{DD} = 100$ mV.

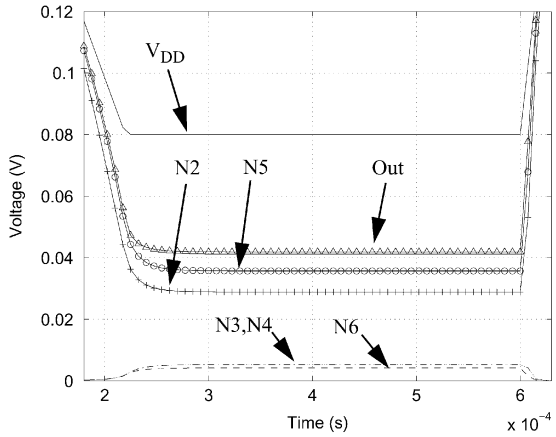

Fig. 11. Simulation of critical path LFBFF holding a one at $V_{DD} = 80$ mV.

the initial point of failure for the flip-flop as the power supply lowers. The two key nodes for storing a one are the N2/N5 node and the output node. For simplicity, this analysis ignores the contribution of the sleep devices that are turned off by the sleep signal and considers only the conditionally off devices. Initially, M_{P1}, M_{P2}, and inverters I3 and I4 are all minimum sized. The output retains a correct value as long as M_{P2} can supply all of the current, I_a, drawn by the two NMOS sleep devices with $|V_{DS}|$ (for M_{P2}) near 0. As previously shown with the inverter example, increasing the size of M_{P2} will extend the ability of the output node to hold a one at lower supply voltages.

Fig. 10 shows a transient simulation of the failure of a minimum sized LFBFF to hold a one in a dual-V_T, 0.13-μm technology. This failure occurs with a supply voltage of 100 mV. The figure shows that node N6 begins to increase its voltage value well before the flip-flop actually fails. As the output node voltage (input to I4) begins to drop below the V_{DD} value, the PMOS device in inverter I4 sees larger $|V_{GS}|$, and the NMOS in I4 loses some of its current drive. Consequently, node N6 rises above zero to balance the current in the inverter. The increase of N6 aggravates the situation with I_a by reducing the gate drive for M_{P2} and increasing the gate drive of the NMOS sleep device. This feedback degrades the ability of M_{P2} to sustain I_a without the output voltage dropping even more. A similar situation causes the logical one at node N5 to transition to zero. Fig. 9 shows two currents, I_b and I_c, that act to pull node N5/N2 toward ground. $|V_{DS}|$ for the PMOS in inverter I3 must increase for that device to maintain I_b as the voltage supply drops.

Increasing the width of M_{P2} above minimum size allows that FET to sustain the large leakage current I_a without requiring a larger $|V_{DS}|$. Similarly, raising the size of the PMOS device in inverter I3 would hold N5 at a logical one for lower supplies. Balancing the device sizes in the LFBFF permits the flip-flop to hold a logical one or zero at a supply voltage of 80 mV in simulation. Fig. 11 shows a transient simulation of the correct operation. Note that the output node and all the internal voltages settle to a steady state at the lower supply voltage and then return to the proper levels when the supply voltage rises again [12].

C. LFBFF Measurements

The energy savings achieved by standby voltage scaling are demonstrated on a 0.13-μm, dual-V_T test chip that uses LFBFFs as storage elements in a small FPGA architecture. This test chip previously demonstrated leakage reduction techniques using MTCMOS circuits [13]. The ability of the LFBFFs to cut off high leakage paths during sleep mode in an MTCMOS

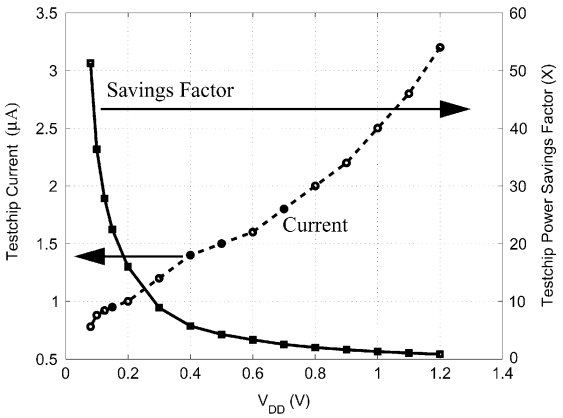

Fig. 12. Measured test chip current and power savings in sleep mode versus V_{DD}.

circuit means that any power savings from standby voltage scaling come in addition to the savings achieved by entering sleep mode. The combined use of MTCMOS sleep mode with standby voltage scaling can produce dramatic total reductions in power.

Fig. 12 shows the measured dependence of current on V_{DD} for the entire test chip during sleep mode. It also shows the measured power savings for the test chip using dynamic voltage scaling. These measurements show the current drawn by the test chip while the sleep signal is asserted and the high V_T devices limit the leakage current. Results from [13] show that using MTCMOS logic allows the chip to reduce its standby current during sleep mode by about 8× without lowering V_{DD} at all. Thus, since Fig. 12 shows sleep mode measurements, the savings shown in the figure are in addition to the previously mentioned sleep mode savings, so the total measured savings relative to active mode idle current is 8× greater than the values shown in Fig. 12. Both curves in the figure follow the trend described in Section II. The power savings increase rapidly for V_{DD} below about 200 mV as a result of the rolloff in subthreshold current.

Measurements from the test chip show that the simulations give good approximations to the actual ability of the flip-flops to hold state. To measure the failure point, data was shifted into the LFBFFs on the chip during active mode. The chip was then placed into sleep mode, and the power supply was lowered to the test value where it stayed for an extended period of time. Then the supply returned to its nominal value and the data were shifted out and compared to the expected values. The measurements show that the LFBFFs on the test chip hold both one and zero consistently at and above 95 mV, while the LFBFFs in simulation held their state down to 80 mV.

IV. Detecting Proximity to Failure

The minimum voltage scaling value in simulation shows some discrepancy from the value measured on the test chip. This indicates that an open-loop design for voltage scaling should be conservative. An open-loop design is one in which the value for the scaled voltage supply is fixed at design time. This predetermined value should account for variations in process corner, temperature, threshold voltage, etc. A closed-loop solution can achieve higher savings without losing state [12]. By monitoring how close the critical path flip-flops are to failure, the supply voltage can be dynamically adjusted for maximum savings under different environmental conditions such as varying temperatures.

A. Canary Flip-Flops

We propose using "canary" flip-flops sized to fail at higher supply voltages than the critical path flip-flops for detecting proximity to failure. The analysis of the MSFF and LFBFF shows that sizing can adjust the failure point for holding a zero or a one, but improving one case degrades the other. Referring to Fig. 4, the MSFF improves its ability to hold a logical one when the PMOS/NMOS ratio is decreased in I1 or increased in I3 or I2. These same changes degrade the ability of the MSFF to hold a logical zero, so this knowledge can be used to build a bank of canary flip-flops that fail to hold a zero at higher V_{DD} values than the base design. For simplicity, we consider changing the PMOS/NMOS ratio only in I1. Fig. 13 shows how the size of this inverter affects the failure voltage. In Fig. 13(a), the results of a dc sweep for different sizes of I1 is shown. Fig. 13(b) shows the failure voltage from plot (a) versus the PMOS/NMOS ratio of I1, normalized to the base case. Clearly, this example shows that a fine granularity of failure points is possible for relatively small sizing changes in a single inverter. Applying sizing changes to the rest of the flip-flop allows for a greater failure range, up to 300 mV for the MSFF. Reversing the sizing analysis allows for a bank of canary flip-flops to predict failure for holding a logical one.

Canary flip-flops can only provide a convincing guarantee that the core flip-flops are safe if they consistently fail at a higher supply voltage than the core flip-flops. To test the robustness of the canary flip-flop approach, we designed two banks of LFBFF canary flip-flops. The first bank is sized to fail at the typical process corner for nine different voltages above the critical path flip-flop while holding a one. The second bank serves the same task for storing a zero. The sizing lessons from the MSFF transfer directly to the LFBFF, but the LFBFF also has the pull-up and pull-down sleep devices available for sizing changes. Our canary flip-flops exploited sizing changes in these devices as well.

Fig. 14 shows simulation results for the LFBFF canary flip-flops at all process corners. The horizontal axis shows the sizing category for the flip-flops in each bank where number "1" is the critical path flip-flop and number "10" is sized to fail at the highest voltage. The typical corner (TT) shows a smooth gradient of failure voltages across the sizing categories. The smoothness of the curve changes at other corners, but the critical path flip-flops always fail at the lowest supply voltage. This result indicates that the canary flip-flops will correctly alert a controller to how close the supply voltage comes to the ultimate failure point at every process corner. Simulations of the canary flip-flops over different temperatures also maintain the gap between the canary and core failure points. Fig. 15 shows a simulation for the banks of LFBFFs where the canary flip-flops fail before the core flip-flops across the full range of temperatures.

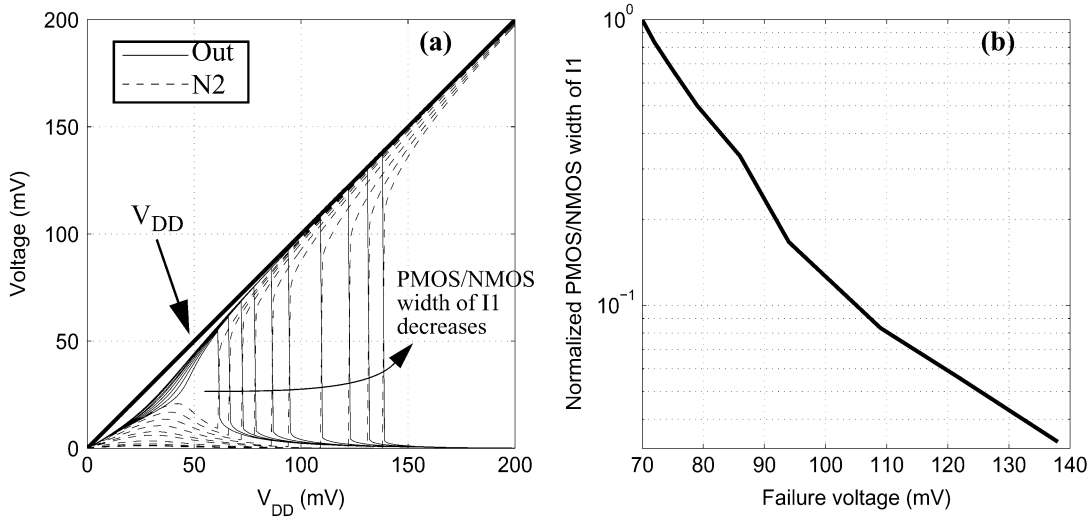

Fig. 13. Canary flip-flop sizing for MSFF in 0.18 μm technology: (a) overlayed dc sweeps of canary MSFFs holding '0'. Failure voltage increases as PMOS/NMOS width of I1 decreases. (b) Failure voltage of canary MSFFs versus PMOS/NMOS width of I1 normalized to base case.

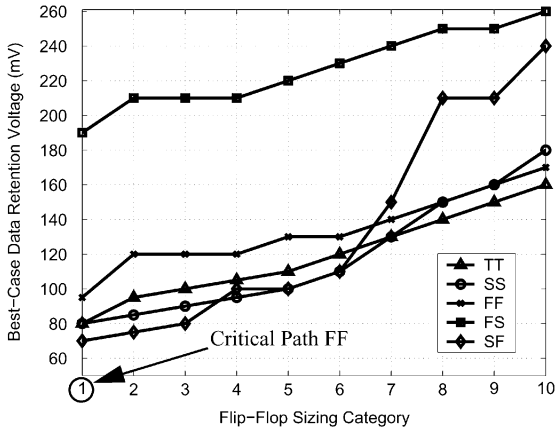

Fig. 14. Simulation of LFBFF canary flip-flop banks at all process corners. The voltage plotted is the lowest supply voltage at which the given flip-flop continues to hold state correctly. Each line represents the worst case from storing '0' and '1' for the given corner.

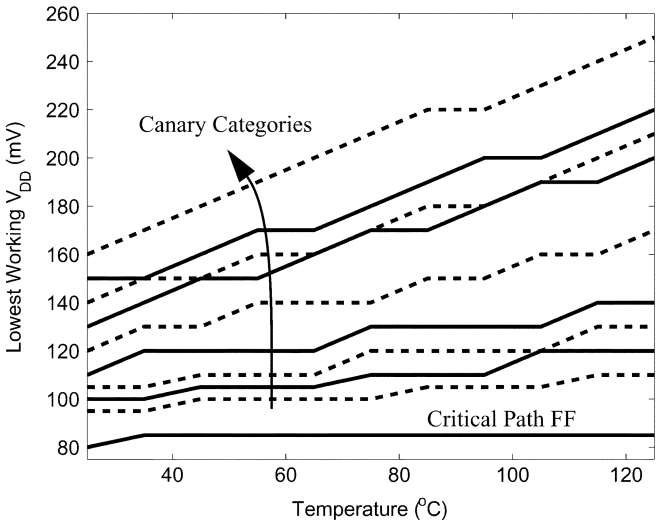

Fig. 15. Simulation of LFBFF canary flip-flop banks over temperature. The voltage plotted is the lowest supply voltage at which the given flip-flop continues to hold state correctly. Each line represents the worst case from storing '0' and '1' for the given corner. The canary flip-flops consistently fail before the critical path flip-flops at all temperatures.

B. Closed-Loop Standby Voltage Scaling

A closed-loop control of the standby voltage supply based on feedback from the canary flip-flops can lower the supply voltage very close to the minimum value without causing the critical path flip-flops to fail. The process corner plot also tells exactly how much power savings the closed-loop approach can offer above the optimal open-loop design. The critical path flip-flop fails at the worst case corner at just below 200 mV. At the other corners, it operates down to below l00 mV. Supposing that an aggressive open-loop design can safely scale V_{DD} to 200 mV for all cases, the closed-loop approach gives over 2$\times$ additional savings at any other corner by scaling down near l00 mV (see Fig. 12). Thus, the closed-loop approach offers significant power savings even over the optimal open-loop approach.

A controller using canary flip-flops has several other advantages as well. First, since the flip-flop bank is designed to fail with a thermometer pattern, any notches in the failure sequence (i.e., category 6 fails before category 7) would indicate large process variation within the die. If the canary flip-flops are placed around the chip in proximity with the core flip-flops, then there is increased likelihood that they will detect severe variation in V_T. If this situation is detected, then the controller could scale less aggressively in response. Secondly, the flip-flop bank effectively estimates how close the core flip-flops are to failure, allowing a tradeoff between reliability and power savings. Less aggressive scaling can be used for critical data, while less critical data makes aggressive voltage scaling possible. Finally, the closed-loop approach tracks changes in the environment. Any change that affects the core flip-flops has a similar impact on the canary flip-flops. Since the canary flip-flops fail before the core devices, then the system continues to work as the environment fluctuates.

V. Conclusion

Examining the potential savings from scaling V_{DD} in standby mode shows that lowering the supply close to the minimum

value for holding state is worthwhile. Since open-loop approaches will need to be conservative, we propose a closed-loop approach using canary flip-flops. Simulations show that the canary flip-flops consistently fail at higher supply voltages than the core flip-flops at all process corners and operating temperatures. The success of the canary flip-flops makes a closed-loop approach to standby voltage scaling feasible. Measurements show that this approach would give power savings of over 40× in a 0.13-μm, dual-V_T test chip. This is over 2× better than an optimal open-loop approach.

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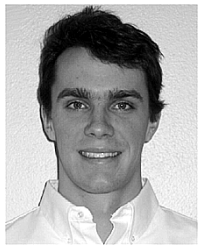

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