

*Review*

## **A DC-DC Converter Efficiency Model for System Level Analysis in Ultra Low Power Applications**

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**Abstract:** This paper presents a model of inductor based DC-DC converters that can be used to study the impact of power management techniques such as dynamic voltage and frequency scaling (DVFS). System level power models of low power systems on chip (SoCs) and power management strategies cannot be correctly established without accounting for the associated overhead related to the DC-DC converters that provide regulated power to the system. The proposed model accurately predicts the efficiency of inductor based DC-DC converters with varying topologies and control schemes across a range of output voltage and current loads. It also accounts for the energy and timing overhead associated with the change in the operating condition of the regulator. Since modern SoCs employ power management techniques that vary the voltage and current loads seen by the converter, accurate modeling of the impact on the converter efficiency becomes critical. We use this model to compute the overall cost of two power distribution strategies for a SoC with multiple voltage islands. The proposed model helps us to obtain the energy benefits of a power management technique and can also be used as a basis for comparison between power management techniques or as a tool for design space exploration early in a SoC design cycle.

**Keywords:** power management; modeling; DC-DC converter; DVS; DVFS; Ultra low power SoC; efficiency

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**1. Introduction**

This paper presents a model for inductor based DC-DC converters and its application to quantify the benefits of power management techniques for ultra low power (ULP) SoCs. Various power management techniques, such as dynamic voltage and frequency scaling (DVFS), clock gating, and power gating are now commonly employed in many SoCs. However, the power benefits of these techniques cannot be quantified accurately without assessing their impact on the DC-DC converter that delivers power. For example, DVFS uses a high voltage to support higher performance and lower voltage to save power. However, changing the output voltage of a DC-DC converter incorporates significant power overhead, and the efficiency can vary widely across voltage and current loads. These overheads may offset the benefits from DVFS. There is a need to characterize the benefits of power management techniques like DVFS in conjunction with their impact on the DC-DC converter. This is particularly important for ultra-low energy near- or sub-threshold systems that operate in a very dynamic power environment, and whose power constraints are stringent. This paper presents a model [1] that enables the study of power management techniques by taking into account their impact on DC-DC converters of different topologies. The model is based on an analytical treatment of inductor based DC-DC converters, and it captures their efficiency trends with varying current load and output voltage. Since parameter selection will influence the specific behavior of the modeled converter, the model provides a rapid and effective tool for early design phase exploration of the impact of a converter by using parameters based on different prior designs or by sweeping parameters to investigate the optimal design requirements for the overall system.

**Figure 1.** Structure of the proposed model. (a) DC-DC efficiency modeling; (b) System energy cost model.

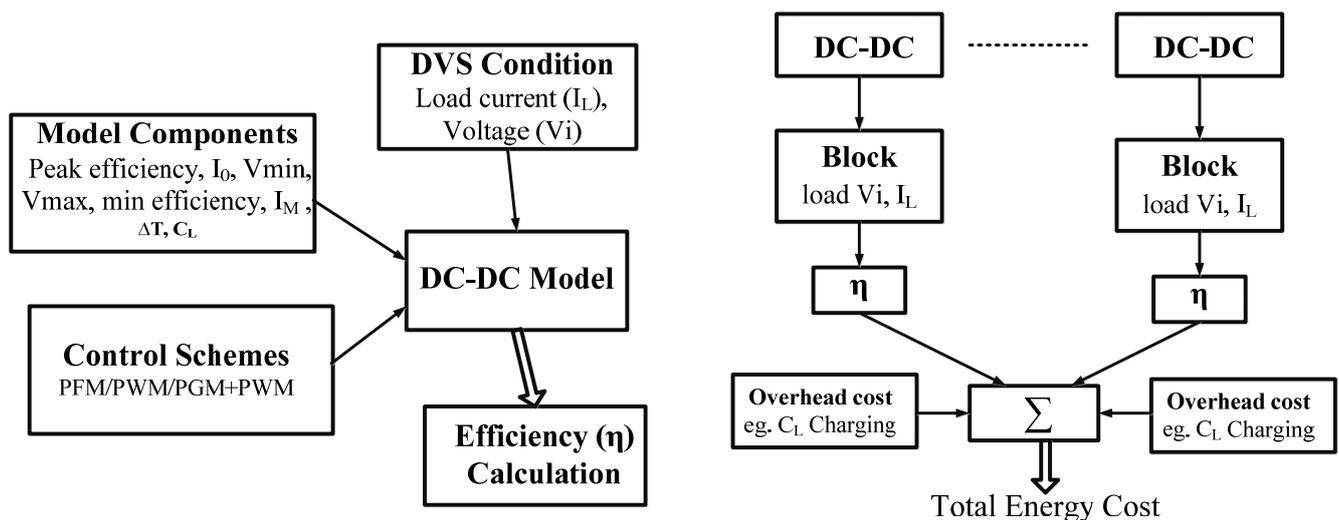
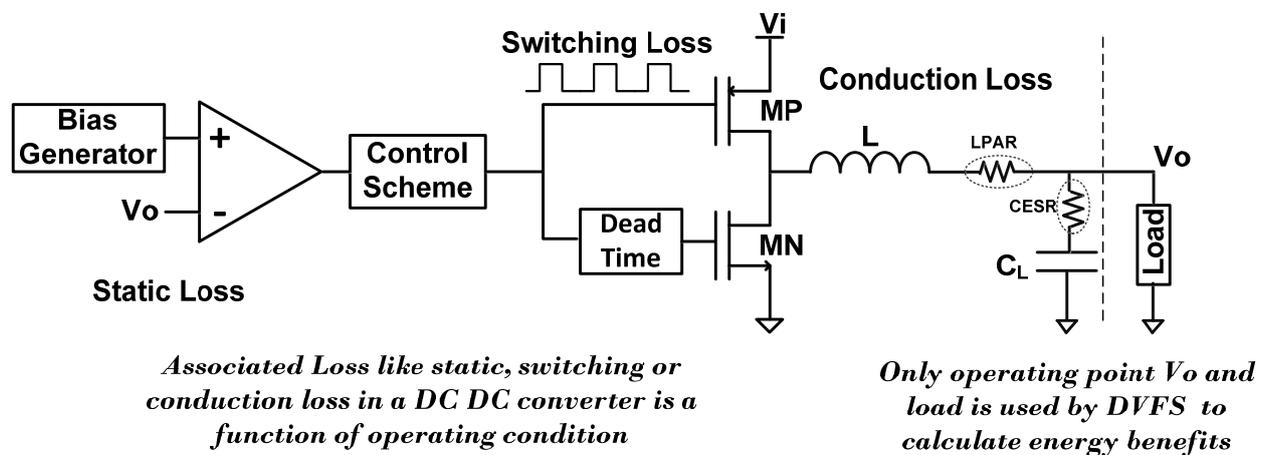


Figure 1 shows the structure of the proposed model, which is broken into two parts. First, a model of inductor based DC-DC converters (Figure 1a) takes the operating condition of a workload as an input, which includes peak efficiency, load at which the peak occurs, minimum efficiency, maximum and minimum output voltages, settling time, and the decoupling capacitance of the DC-DC converter, and generates an efficiency calculation. In order to capture the dynamic load condition of the converter

in the context of the operation of a specific power management scheme, the second part of the model (Figure 1b) uses one or more of the DC-DC converter models in a larger system model that includes the input voltage ( $V_i$ ), output voltage ( $V_o$ ), load current ( $I_L$ ), time of operation, parasitic capacitance on the block, switching frequency, and activity factor. These parameters can change dynamically in power management techniques like DVFS. Using these parameters as input, the model calculates the overhead cost and change in the efficiency of each DC-DC converter in the system and provides the total system level energy consumed while executing a power management technique for the given workload profile.

The energy savings for a power management technique are typically reported at the load circuit operating voltage and load level in literature [2]. For example, the authors in [2] report the energy savings obtained by scaling the voltage and frequency to a lower value. The paper does not calculate the total energy drawn from the original source of the supply voltage, for example a battery, which may not change linearly with load at the final circuit. Changing the operating condition of a voltage regulator causes deviation from its optimal behavior. If the output voltage of a buck converter is reduced, the efficiency of the converter degrades. Also, reducing the output voltage means that the capacitor  $C_L$  is discharged to a lower voltage by dissipating its stored energy. The actual benefits can be obtained by taking these losses and overhead into account. Figure 2 shows a block diagram of a typical inductor based DC-DC converter. It includes a bias generator and comparators that cause the static loss. The control scheme that implements the switching pattern of the power switches MP and MN can vary across topologies. The switching loss is a function of the control scheme and the load. The power switches MP and MN, parasitic resistance of inductor ( $L_{PAR}$ ), and capacitor ( $C_{ESR}$ ) cause the conduction loss, which is determined by the load current and output voltage. These losses are all a function of the operating condition. The proposed model accurately predicts the trends in behavior of DC-DC converters across topologies implementing both pulse width modulation (PWM) and pulse frequency modulation (PFM) control schemes.

**Figure 2.** Loss mechanisms inside a typical switching DC-DC converter.



**2. DC-DC Converter Model**

In order to model DC-DC converter trends and to capture the impact of DC-DC converters on power management strategies, it is essential to account for the converter efficiency, which is the power

delivered to the load divided by the total power drawn by the converter. This efficiency of the DC-DC converter is a function of its output load, output voltage ( $V_o$ ), the switching frequency, the switch resistance, and the parasitic resistance in the inductor and capacitor (Figure 2). In this section, we derive models for the efficiency for both PWM and PFM control schemes. Additionally, it is important to model how the converter will respond to changes in its usage. In a dynamic power environment like DVFS,  $V_o$  and load current vary dynamically, which changes the efficiency of the converter and results in energy overhead. Also, the converter can take significant time to settle from one voltage to another, resulting in timing overhead. Additional energy overhead comes in the form of charging and discharging of the decoupling capacitor. To quantify the benefit of a given power management technique like DVFS, we need to account for these overheads in addition to modeling the efficiency at a fixed load. In this section, we derive and describe the proposed model for an inductor based DC-DC converter that accounts for these overheads and that can be used in a larger system model to study specific power management techniques.

### 2.1. DC-DC Efficiency with Load Current

#### 2.1.1. Model for PWM Control Scheme

Voltage and frequency are varied in DVFS to trade off power consumption with speed. This changes the load current and output voltage of the DC-DC converter, which changes its efficiency. In this section, we define a model that captures the change in efficiency that results from changing load conditions. One prior work [3] models the power loss in a DC-DC Buck converter using a PWM switching scheme with the following equation:

$$P_{Buck} = a \sqrt{(I_L^2 + \Delta i^2/3)f_s} + b \left\{ \frac{I_L^2}{\Delta i f_s} + \frac{\Delta i}{3f_s} + \frac{C_L V_{DD1}^2}{R_{L0} \Delta i} \right\} + d f_s \Delta i \quad (1)$$

where  $I_L$  is the load current;  $\Delta i$  is the current ripple in the converter;  $f_s$  is the switching frequency;  $C_L$  is the decoupling capacitor;  $R_{L0}$  is the inductor series resistance; and  $a$ ,  $b$ , and  $d$  are constants. Equation (1) represents the power loss in terms of various constants that cannot be obtained and that are non-intuitive to approximate prior to the design of converter, so it is difficult to apply this equation for design space exploration or for general modeling of DC-DC converter trends.

Instead, we propose a model that accurately captures the trends in the efficiency of the DC-DC converter in terms of the peak and minimum efficiency values of the converter, which can be either predicted, specified as targets, or pulled from prior work. To derive this simplified model, we begin by following previous work [3,4] in the observation that Equation (1) leads to an efficiency in the form

$$\eta_{I_L} = \eta_2 - (\eta_2 - \eta_1) * (\log(I_L/I_o))^2/4 \quad (2)$$

where  $\eta_2$  is the peak efficiency occurring at load  $I_o$ , and  $\eta_1$  is the minimum efficiency at a given load. For the verification of the model proposed in Equation (2), let us consider the following cases.

For a light load condition in Equation (1),

$$I_L \sim \Delta i$$

So the power loss given by Equation (1) in the buck converter takes the form of

$$P_{Buck} = \alpha I_L + \beta / I_L$$

The efficiency of the converter will be given by power delivered ( $VI_L$ ) over power drawn:

$$\eta_{I_L} = VI_L / (VI_L + \alpha I_L + \frac{\beta}{I_L}) \tag{3}$$

Expanding Equation (3) using Taylor’s series we get:

$$\eta_{I_L} = V / (V + \alpha) \{ 1 - \frac{\beta}{(V+\alpha)I_L^2} + \frac{\beta^2}{(V+\alpha)^2 I_L^4} + \dots \} \tag{4}$$

It is clear from Equation (3) that the efficiency decreases as load current decreases for the cases of light load conditions on the converter. The proposed equation in the model is given by:

$$\eta_{I_L} = \eta_2 - (\eta_2 - \eta_1) * (\log(I_L/I_O))^2 / 4$$

This expression also decreases for the light load condition, capturing the correct behavior of DC-DC converter efficiency trend. We know from Taylor’s series that:

$$\ln(I_L/I_O) = -\{ (\frac{I_O}{I_L} - 1) - 1/2 (\frac{I_O}{I_L} - 1)^2 + \dots \} \tag{5}$$

Since,  $I_O \gg I_L$  and converting natural logarithm into logarithm of base 10 we get:

$$\log(I_L/I_O) = -2.303 \{ (\frac{I_O}{I_L}) - 1/2 (\frac{I_O}{I_L})^2 + \dots \}$$

So the efficiency equation in Equation (2) can be rewritten as:

$$\eta_{I_L} = \eta_2 - 2.303(\eta_2 - \eta_1) / 4 * \{ (\frac{I_O}{I_L})^2 - (\frac{I_O}{I_L})^3 + \dots \}$$

$$\eta_{I_L} > \eta_2 - 2.303(\eta_2 - \eta_1) / 4 * (\frac{I_O}{I_L})^2 \tag{6}$$

*Using,  $x > \log x$*

The proposed model in Equation (2) for the DC-DC converter reduces to Equation (6) under light load, which follows the behavior of DC-DC converter reported in literature [3] and compares well with Equation (4) with maximum efficiency  $\eta_2$  in Equation (2) can be obtained by equating the constants in Equations (4) and (2),

$$\eta_2 = V / (V + \alpha) \tag{7}$$

Equations (2) and (6) are not bounded for the cases when  $I_L$  becomes very small, but it can predict the behavior for light load condition in a PWM control switching scheme based DC-DC converter with less than 5% error. Figure 4 shows this result.

Now consider the case when load is very high compared to the point of peak efficiency. The constant  $a$  in Equation (1) represents the resistance of the MOS transistor used for switching [3]. The model of [3] assumes it to be a constant. However, the resistance of MOS transistor increases with the increase in load current and it is given by:

$$R_D = K * (1 + \frac{I_L}{I_{DSAT}}) \tag{8}$$

where  $I_{DSAT}$  is the saturation current of the transistor. Clearly, as load current increases, the resistance increases. For light load condition, it is correct to assume that resistance does not change as  $I_{DSAT}$  is much larger compared to  $I_L$ . However, with an increase in load, the MOS resistance increases, causing elevated conduction loss. Also, at higher load the increased current in the inductor causes elevated conduction loss in the inductor's parasitic resistance. Overall, the  $I^2R$  loss increases, because of the increase in current and because of the increase in resistance caused by that increase in current. For a high load we know that:

$$I_L \gg \Delta i$$

so the power loss in the buck converter using equation (1) of [3] takes the form of:

$$P_{Buck} = \alpha_1 I_L + \beta_1 I_L^2$$

The equation for efficiency can be written as:

$$\eta_{I_L} = VI_L / (VI_L + \alpha_1 I_L + \beta_1 I_L^2) \tag{9}$$

This expression shows that efficiency decreases as the load current increases. Using Taylor series expansion, this expression can be written as,

$$\eta_{I_L} = V / (V + \alpha_1) \{ 1 - \frac{\beta_1 I_L}{(V + \alpha_1)} + (\frac{\beta_1 I_L}{(V + \alpha_1)})^2 + \dots \} \tag{10}$$

In the proposed equation in this paper, Equation (2), the efficiency also decreases for the higher load. Expanding (2) using Taylor's series,

$$\eta_{I_L} = \eta_2 - (\eta_2 - \eta_1) / 4 * \{ k1 + k2 \frac{I_L}{I_O} + k3 \left( \frac{I_L}{I_O} \right)^2 + \dots \} \tag{11}$$

Equations (10) and (11) follow closely, with constants  $\eta_2$ ,  $\eta_1$ ,  $k_1$ , etc. in Equation (11) can be obtained by equating with respect to the powers of  $I_L$  in Equation (10). The proposed equation matches the trend of equation reported in literature [3].

While Equations (1), (4) or (10) can be more analytical versions of the DC-DC converter efficiency formulation, they are not very useful for early design space exploration or for studying system level power management techniques because of the unknown constants. In contrast, the compact model in Equation (2) can be expressed in terms of peak efficiency and minimum efficiency, making it easy to use.

### 2.1.2. Model for PFM Control Scheme

In the PFM control scheme with a constant peak inductor current, the switching and conduction loss scale with frequency, and the efficiency remains flat for higher loads. The power loss is given by

$$P_{Buck} = K * P_{Out} + C \tag{12}$$

where  $K$  and  $C$  are constants. The first term indicates switching and conduction loss that scales with frequency. The second term indicates the static loss that does not scale with frequency. Therefore:

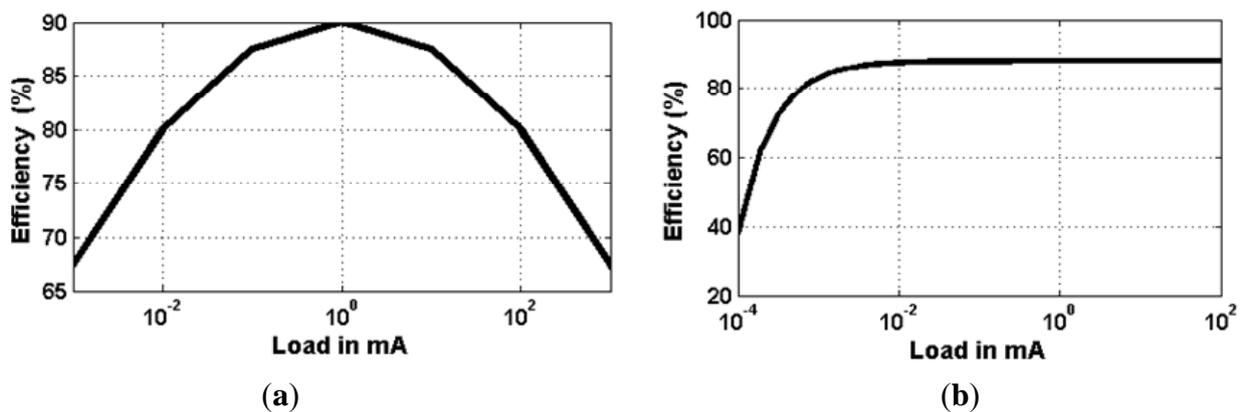
$$\eta_{I_L} = \frac{P_{Out}}{(P_{Out} + K * P_{Out} + C)} \tag{13}$$

Using  $P_{Out} = VI_L$  and expanding using Taylor series,

$$\eta_{I_L} = \eta_2 - \frac{a}{I_L} \tag{14}$$

Equation (14) shows that the efficiency increases and becomes constant as load increases. This happens because power loss in PFM schemes scales with the load. At light load condition, the static loss dominates reduces the efficiency.

**Figure 3.** Efficiency Variation with load current in (a) pulse width modulation (PWM) scheme with  $\eta_2 = 0.9$ ,  $\eta_1 = 0.68$  and  $I_L = 1$  mA; (b) pulse frequency modulation (PFM) scheme with  $\eta_2 = 0.88$  and  $a = 5 \times 10^{-5}$ .



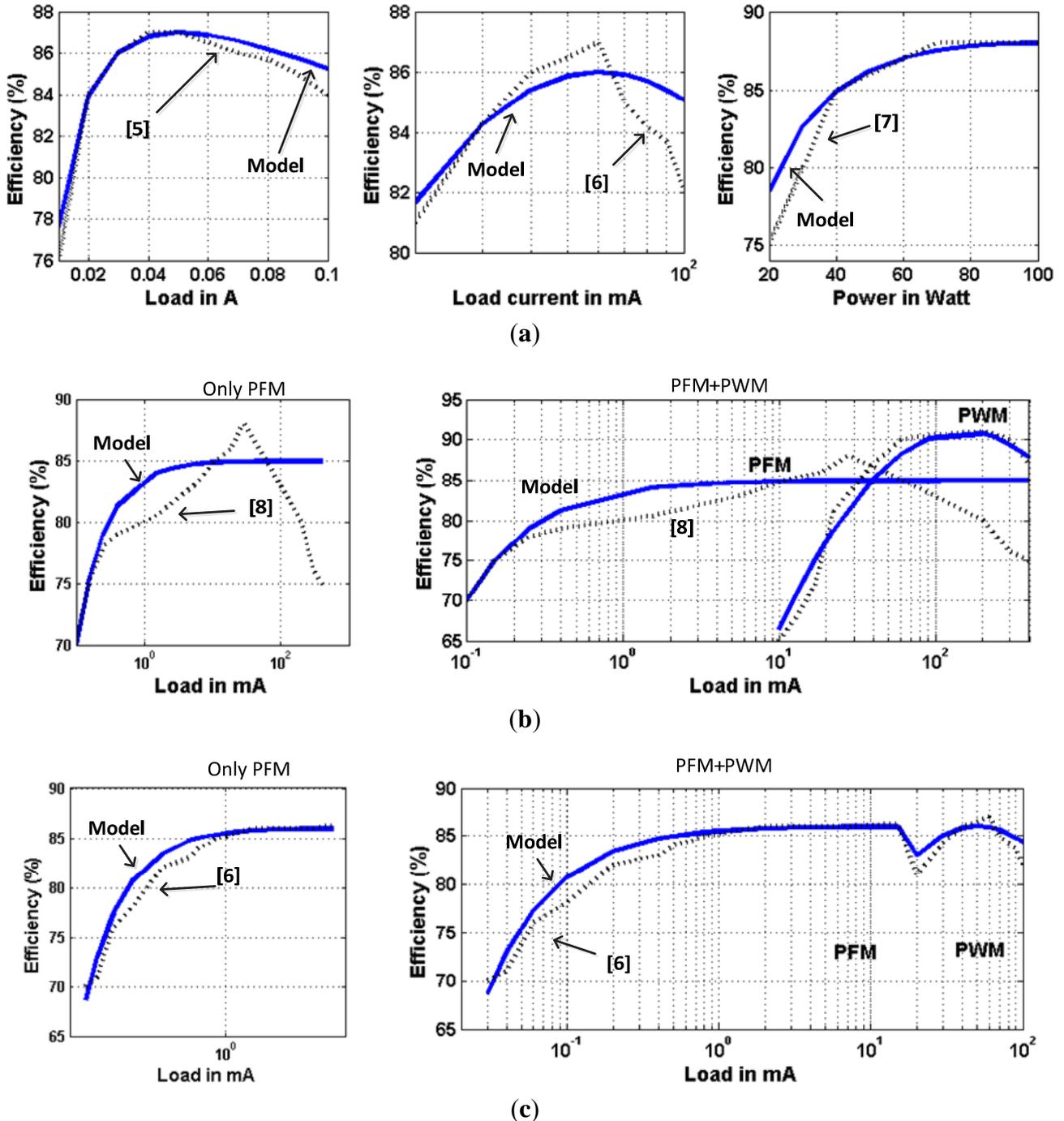
### 2.3. Verification of the Model

The equations we have provided accurately model the trends for PWM, PFM, and combinations of those control schemes. Figure 3 shows the variation of efficiency with respect to load when using dedicated PWM and PFM control schemes. In the PWM scheme, the efficiency degrades at high load and at light load conditions, while in the PFM scheme the efficiency remains flat as load increases and degrades at light load conditions.

Figure 4 shows the comparison of the model equations for PWM and PFM control schemes with the measured results reported in literature [5–8]. Figure 4a shows the results for the PWM scheme. For Equation (2), we have selected  $\eta_2$  as the peak efficiency reported in the corresponding paper and  $I_O$  as the load for that peak efficiency. The value of  $\eta_1$  is obtained experimentally based on [5–8], and we set  $\eta_1 = 10$  for all the papers ([5–8]) employing the PWM control scheme. The converters [5–7] and [8] in part implement PWM. We find that the model predicts the efficiency behavior of the converters very accurately (<5% error for these papers). For [5,7,8] the error is less than 3%.

We also compared the model with reported works that employ the PFM switching scheme. Figure 4b,c shows the results. For the PFM scheme, we used  $\eta_2$  as the peak efficiency reported in the corresponding paper. The constant  $a$  represents the static loss of the converter and will vary from one converter to another. It causes the degradation in efficiency at light load condition in a PFM control scheme. For this comparison, we set the value of constant  $a$  in Equation (14) to match the least efficiency reported in each paper. The model predicts the behavior of [6] correctly for the PFM scheme, while it deviates at higher load for [8]. This is because we assumed in our model that PFM scheme is used only for a light load condition, whereas [8] shows results for loads up to 400 mA.

**Figure 4.** Comparison of the load equation with measured work in literature. (a) Comparison of model with the measured PWM DC-DC converter reported in literature; (b) Comparison of model with [8], implementing both PFM and PWM; (c) Comparison of model with [6], schemes implementing both PFM and PWM.



To further illustrate the usefulness of the model, we also compared it with the schemes where both PFM and PWM schemes are employed. This is often done to increase the range of load a converter can support. Figure 4b,c shows the results of comparison of the model with efficiencies reported in [6] and [8]. The model accurately predicts the behavior of such converters. There can be several other combinations in which the model can be used. For example, the model can be used for a segmented

switch scheme if two or more curves for Equation (2) are used in conjunction, with each curve having a peak efficiency ( $\eta_2$ ) corresponding to a different value of  $I_O$ .

The proposed model is accurate in predicting the efficiency trend with respect to the load if the control scheme is PWM or PFM. Also, an approximate peak efficiency of a DC-DC converter can be obtained very early in the design cycle as it is dependent on the technology, size of the inductor, and ripple on rails. Therefore, the model can be employed for analyzing the DC-DC converter overheads early in design while implementing power management techniques.

#### 2.4. Efficiency with Output Voltage

The peak efficiency of an inductor based DC-DC converter decreases with a decreasing output voltage. For a given load current, the switching loss and conduction loss of the converter remain the same. The decreased output power level at lower voltages results in a decreased efficiency. The efficiency as a function of voltage can be modeled as:

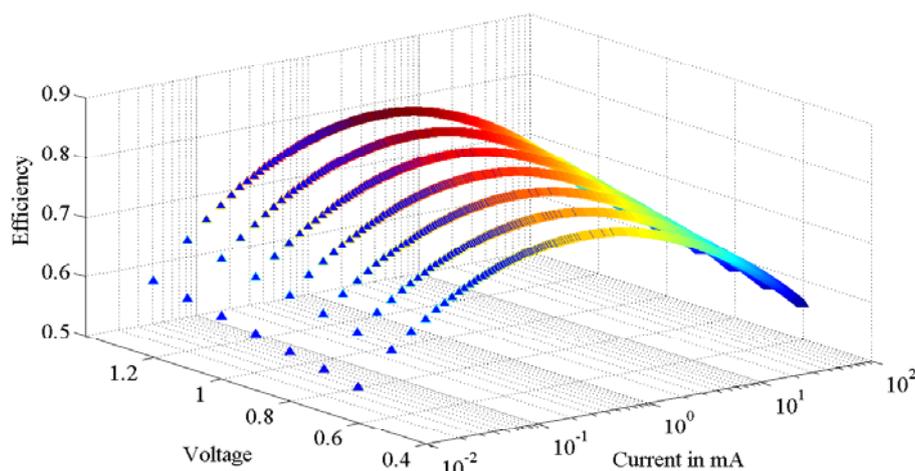
$$\eta_V = \eta_1 + m(V - V_{min}) \tag{15}$$

where  $m$  is the slope of the line given by  $m = (\eta_2 - \eta_1)/(V_{max} - V_{min})$ . This approximate linear behavior is reported in both [3] and [4]. Plugging Equation (2) for PWM or Equation (14) for PFM and using Equation (15) lets us write the combined voltage and load efficiency as:

$$\eta = \eta_V * \eta_{I_L} \tag{16}$$

Figure 5 shows the output of the proposed model with  $V_O$  and with load current assuming a PWM control scheme. A DC-DC converter designed for a specific voltage and load will follow this trend when its load current or output voltage changes.

**Figure 5.** Dynamic efficiency variation with current and voltage.



### 2.5. Settling Time

The settling time of a converter is the time it takes to reach the desired supply voltage. A typical converter has a large inductor and a large filter capacitor that makes the settling time very large (few  $\mu$ s to ms [9]). In a dynamic environment like DVFS or Ultra DVS (UDVS), the output voltage  $V_O$  is expected to change. The settling time of a converter to reach the desired voltage becomes an important overhead for these scenarios. The settling time  $\Delta T$  in our proposed model is approximated as,

$$\Delta T = \frac{T}{V} * \Delta V \tag{17}$$

when output voltage is charged to  $V$  from ground, where  $T$  is the settling time of the converter. We assume that the inductor carries the same amount of current for each cycle of charging. Consequently, the rate at which the output reaches a given voltage will be linear with time.  $T/V$  is the slope of this curve and is set by assuming that at each switching cycle the inductor carries the same amount of current even for the cases when the output voltage is rising from zero.

### 2.6. Supply Rail Switching Energy

The change in the output voltage of a converter results in a change of the stored energy on the capacitance of the supply voltage rail of the load blocks. Some of this stored energy is dissipated if the new voltage is lower than the previous voltage, whereas energy is consumed from the source supply,  $V_{in}$ , if the new voltage is higher than the previous voltage. The additional energy overhead  $E_C$  is given by Equation (18) where  $V_1$  and  $V_2$  are the new and previous voltages of the converter. If  $V_1$  is greater than  $V_2$ , work is to be done by the supply  $V_{in}$ . When  $V_1$  is less than  $V_2$ , no work is done by  $V_{in}$  hence energy overhead will be zero.

$$E_C = V_{in} C_L \max(V_1 - V_2, 0) \tag{18}$$

In some cases, the voltage on the capacitor is not immediately discharged to lower voltage. VDD slowly discharges from  $V_2$  to  $V_1$  while running workloads. In such cases  $E_C$  will be lower than given by Equation (18). Equation (16) helps us to predict the losses at a given load or voltage condition, while Equations (17) and (18) give the conversion energy and timing overhead. These equations enable a framework where overheads that originate from dynamic changes to the DC-DC converter output can be calculated for techniques like DVFS to accurately measure their energy benefits.

In summary, this section has derived models for inductor based DC-DC converter efficiency for both PWM and PFM control schemes at a fixed load and provided equations for modeling the overheads that arise when the loads change. In the next section, we examine an example of how to apply these models in the evaluation of power management schemes like DVS.

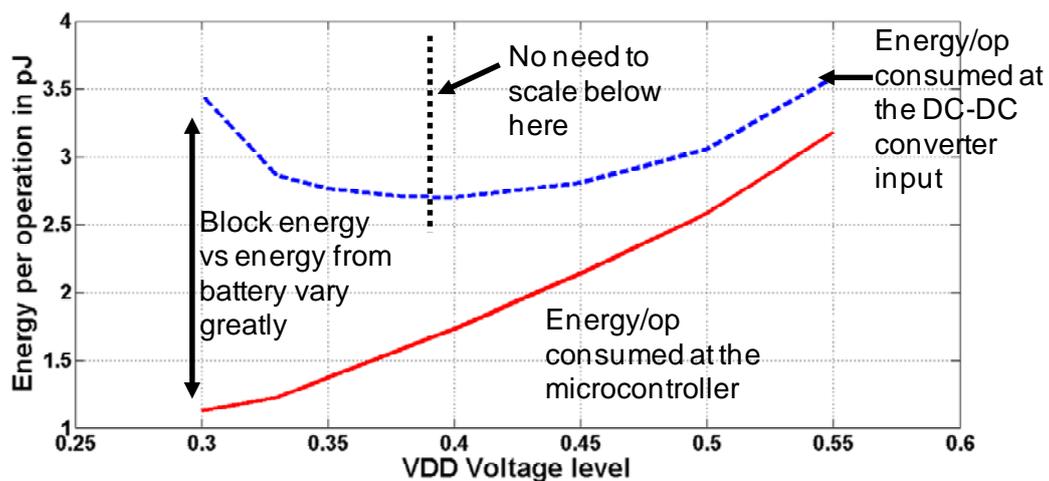
## 3. Evaluation of DVS Techniques Using the Proposed Model

The DC-DC converter model can be used for assessing a variety of block level power management techniques. Since the model captures both the efficiency of the converter for fixed loads and the cost of making dynamic changes to the converter output voltage and load, we can use it to model system level

implementations of varying complexity. In the most basic case, the model can provide additional insight into the system level cost of reducing the voltage delivered to a block or to a chip.

For example, Figure 6 shows the measured energy consumption of a microcontroller in a sub-threshold system on chip [13] across voltage. The minimum energy voltage occurs at below 0.3 V. However, when we consider the amount of energy drawn from the battery or energy storage node, including the overhead of loss in a DC-DC converter, the situation changes significantly. The top line in Figure 6 shows the energy consumed from the source (at the input to the DC-DC converter) using our model, which was fitted to low load DC-DC converter measurements from [14] to illustrate an example converter for this system. Since the output voltage and load current both vary for the block as VDD decreases, it is not accurate to assume a constant efficiency loss in the converter, and our model captures the changing efficiency across the space. This result shows that reporting block level consumption only can result in an inaccurate view of the total impact on the battery, and that the actual optimal voltage [19] for minimizing energy consumed at the battery may be higher than anticipated from block measurements alone.

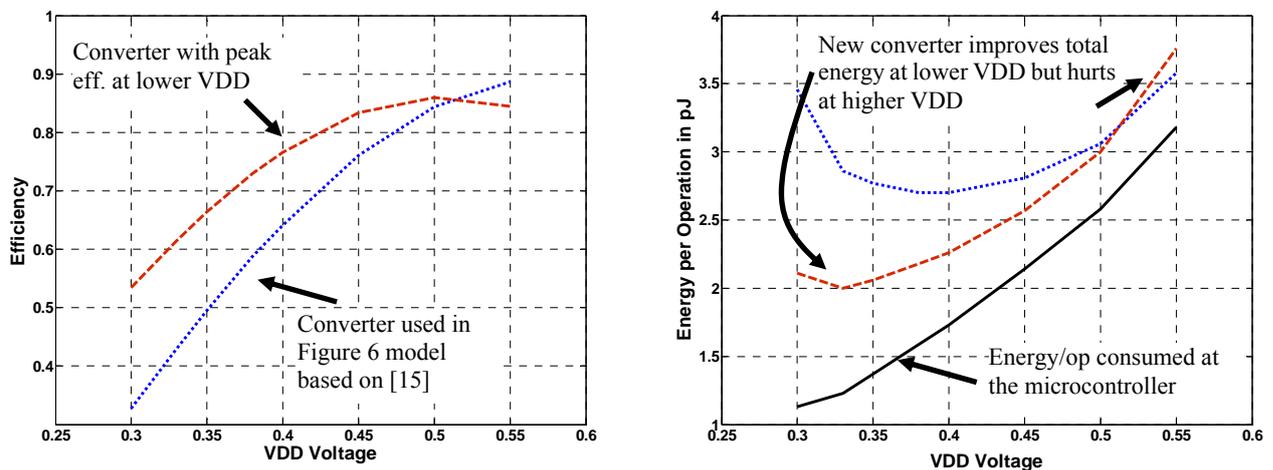
**Figure 6.** Energy consumption for a microcontroller across voltage with and without consideration of the DC-DC converter efficiency.



Further, the DC-DC model can help designers to choose the optimal specification for a converter to use for a given block or chip. This is especially important for embedded converters serving extremely low power systems like the one in [13], which operates from harvested energy. For example, we revisit the design in Figure 6 and consider a different converter design with lower overall peak efficiency, but whose peak efficiency occurs at a lower voltage. Figure 7a shows the efficiency versus VDD for two different converters: one is the converter used in Figure 6 and modeled on [14], and the other is a hypothetical converter. The new converter has a lower overall peak efficiency than the original design, which might lead to the misconception that it will hurt the overall energy consumption of any chip. However, its peak efficiency comes at a lower voltage, so its efficiency scales better across the lower range of voltage values. The impact of this is that, at lower voltage (and lower current) values, the second converter provides more efficient operation. Figure 7b shows the impact of using this converter alongside the curves from Figure 6. Not only is the total energy drawn from  $V_{in}$  much lower, the optimal voltage for minimizing energy occurs at a voltage much nearer to the optimal voltage of the

block. The flexibility of our model allows a designer to experiment with different converter specifications while co-designing an embedded converter with its loading system, providing for rapid design space exploration early in the system design process.

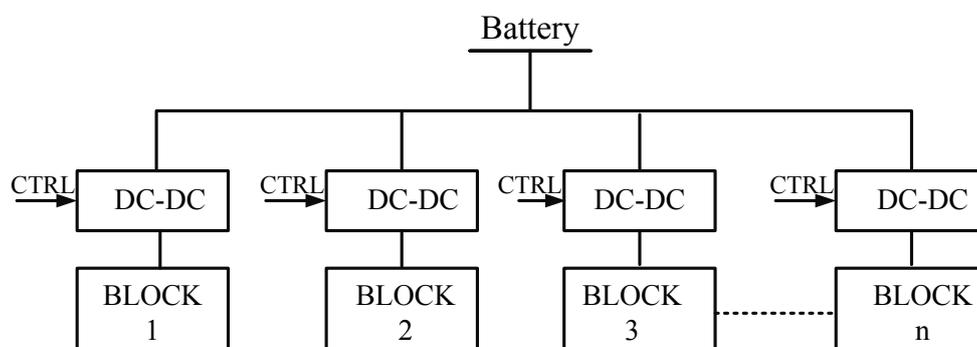
**Figure 7.** (a) Efficiency profiles for two different converters and (b) the impact of a converter change on the overall energy drawn from the battery.



In addition to supporting the co-design of embedded DC-DC converters, our model can enable higher level comparisons of power management techniques that apply to multiple blocks. The next example illustrates the application of our model to two different power management strategies.

DVFS is commonly used to save power in a SoC by changing the supply voltage at the full chip level. Even larger energy savings can be realized by implementing block level DVFS, so that each block can use a voltage that is best matched to its own workload. Figure 8 shows the idealized implementation in which each block has a dedicated DC-DC converter. However, it may not be practically possible to implement such a system because of the area and cost of replicating DC-DC converters for each block. We study this scheme using our model to analyze its benefits by taking into account the overheads discussed earlier in the paper. Later on, we compare this with a more practical implementation of block level power management.

**Figure 8.** Dedicated DC DC converter per block.



*3.1. Framework for Energy Calculation in DVFS*

In this section, we establish the framework for computing the system level energy consumption of a multiple block DVFS system, where individual DC-DC converters are modeled using the equations from Section 2. Figure 9 shows the operating condition of an example block that has a dedicated DC-DC converter. VDD and load will change with time. We have assumed a uniform random distribution for the power supply voltage setting in the range of 0.4 V to 1.2 V.  $\Delta T$  is the settling time of the converter, and we use  $T = 20 \mu s$  and  $V = 1 V$  in Equation (18) [3]. The load capacitor on each block is assumed to be 200 pF.

**Figure 9.** Operating condition for dedicated DC DC.

VDD	Load	Time of operation
V1	i1	T1+ $\Delta T$ 1
V2	i2	T2+ $\Delta T$ 1
.....	.....	.....

Optimal Condition for a Block

VDD	Load	Time of operation
0.9V	100 $\mu$ A	8 $\mu$ s
1.2V	900 $\mu$ A	8 $\mu$ s
.....	.....	.....

Example Table

$$E_{op} = \frac{V_1 i_1 (T_1 + \Delta T_1)}{\eta_1} + \frac{V_2 i_2 (T_2 + \Delta T_2)}{\eta_2} + \dots \tag{19}$$

$E_{op}$  is the operating energy and  $\eta$  is calculated using Equation (3).

$$E_C = V_{in} C_L (\max(V_1 - V_2, 0) + \max(V_2 - V_3, 0) + \dots) \tag{20}$$

$$E_{TOTAL} = E_{OP} + E_C$$

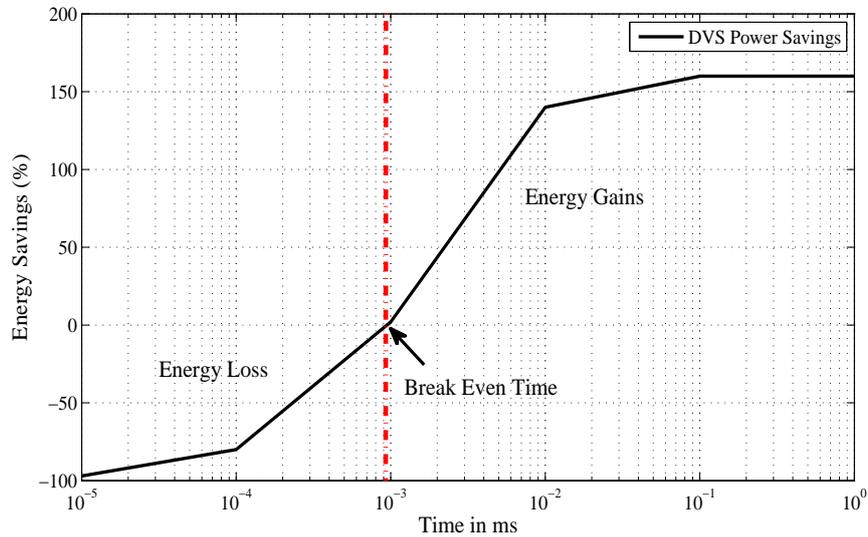
Each block is modeled as a chain of inverters with different depths. The delay of the block is calculated as its time of operation. The power supply level changes for 100 iterations. The rate at which the voltage changes to a new value is varied from 10 ns to 1 ms. The energy dissipation in each case is compared with a single VDD (always 1.2 V) block. Figure 10 shows the result of our experiment. We find that at fast rates of voltage scaling (a voltage transition every  $\sim 10$  ns), the overheads of a DC-DC converter dominate, and there is an energy loss. Energy benefits can be realized for  $T_{OP}$  greater than 1 $\mu$ s with a maximum benefit of more than 150% achievable at slower rates of VDD transitions. This implies that, for these assumptions, the 5 VDD system would save energy relative to the single VDD system when transitioning VDD to adapt to changes in the workload that are slower than  $\sim 1 \mu s$ .

*2.3. Panoptic Dynamic Voltage Scaling (PDVS)*

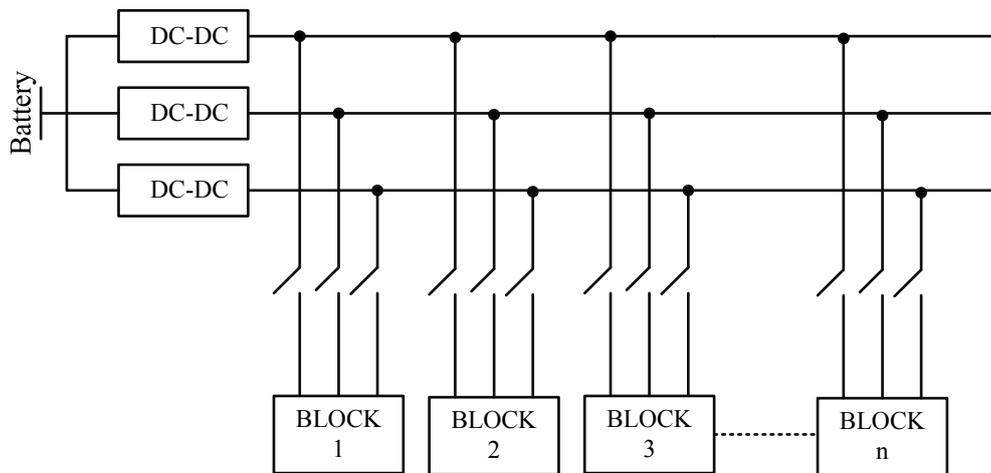
This section applies the DVFS modeling approach to a different DVS implementation. Figure 11 shows the block diagram of a block level voltage scaling technique called panoptic dynamic voltage scaling (PDVS) [15]. In the PDVS technique, a block can switch from one voltage to another by the use of headers as shown in Figure 11. The advantage of this technique is that it enables a much faster

switching. An equivalent DVFS voltage can be realized by dithering between the supplies. This scheme is more practical and has lower cost.

**Figure 10.** Energy Savings with rate of Voltage Scaling.



**Figure 11.** Panoptic dynamic voltage scaling (PDVS): Block level voltage scaling technique.



*2.4. Framework for Energy Calculation in PDVS*

We reproduce the operating condition of a block from Figure 9. This block operates at different voltages for different times to accomplish optimal energy operation. We break down operating condition of Figure 9 into Figure 12. If a block has to operate at  $V_1$  ( $0.4 \text{ V} < V_1 < 0.8 \text{ V}$ ) for  $T_1$  time, PDVS accomplishes it by connecting the block to  $0.4 \text{ V}$  for  $T_{11}$  and  $0.8 \text{ V}$  for  $T_{12}$ , such that  $T_{11} + T_{12} = T_1$  of Figure 9. This approach is called voltage dithering.  $T_{11}$  and  $T_{12}$  are such that the performance of the block does not change. A final operating condition is given by Figure 12b.

**Figure 12.** PDVS operating condition evaluation. (a) Operation condition; (b) Final load table.

VDD	Load			T <sub>OP</sub>
	0.4V	0.8V	1.2V	
v1 V	i11 μA	0	0	T11
v1 V	0	i12 μA	0	T12
v2 V	0	i21 μA	0	T21
v2 V	0	0	i22 μA	T22
.....	.....	.....	.....	.....

(a)

Load			dT <sub>OP</sub>
0.4V	0.8V	1.2V	
<i>i<sub>1</sub>(t)</i>	<i>i<sub>2</sub>(t)</i>	<i>i<sub>3</sub>(t)</i>	1e-9

(b)

The load on each supply will change depending on the blocks that are connected to it and results in a continuous time varying load on each supply. We include time to obtain the energy. Each supply has larger load variation which will have an impact on the overall efficiency. The total energy is given by,

$$E_{OP} = 0.4 \int i_1(t)/\eta_1(i_1)dt + 0.8 \int i_2(t)/\eta_2(i_2)dt + 1.2 \int i_3(t)/\eta_3(i_3)dt \tag{21}$$

$$E_C = 1.2C_L * 0.4(1 + 0 + 0 + 0 \dots) + 0.8C_L * 0.4(0 + 1 + 1 + 0 \dots)$$

$$E_{TOTAL} = E_{OP} + E_C$$

We keep the same system set-up as was used for the dedicated DC-DC converter case. It should be noted that there will be an insignificant overhead of settling time in this case. We assume a capacitive load of 20 pF on each block, since the local block virtual VDD rail switches instead of the total chip-wide VDD rail (with all of its decoupling capacitance).

#### 4. Comparison of DVFS and PDVS using the Proposed Model

Figure 13 compares the PDVS scheme with a dedicated DC-DC converter case using the system level model that incorporates the DC-DC converter equations. The PDVS scheme has a break-even time of 30 ns compared to 1 μs in the dedicated supply case. This is because of the very small settling time in PDVS as the block is charged to the rail almost instantly. It also has lower conversion energy. The total energy benefits from the PDVS scheme is, however, lower than the dedicated DC-DC converter case, because it sees much wider load variation. The PDVS scheme though is better suited for implementing block level DVFS owing to its much smaller break-even time, allowing it to adjust to short changes in the workload. PDVS scales much better to larger numbers of blocks, since it requires only one DC-DC converter output per voltage rail rather than per block, as in the dedicated DVFS

scheme. These results are of course influenced by the values of the parameters in the model, and the model makes it very easy to investigate how the results will vary when the assumptions change.

**Figure 13.** Energy Benefits of PDVS and Dedicated DVFS.

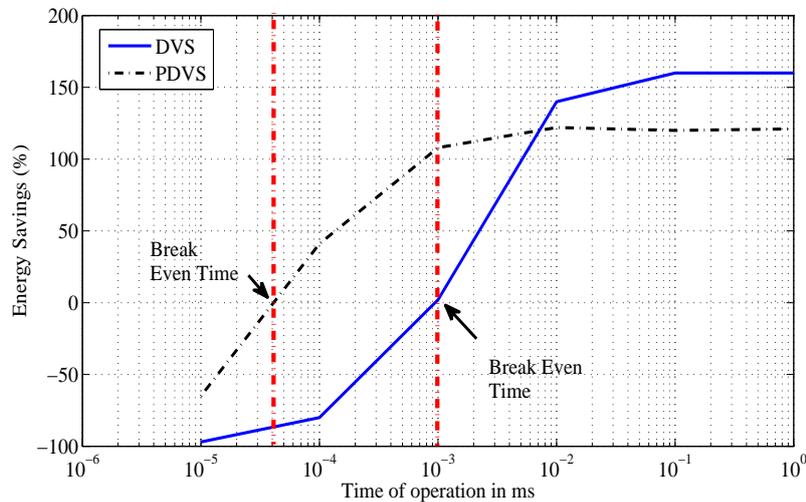
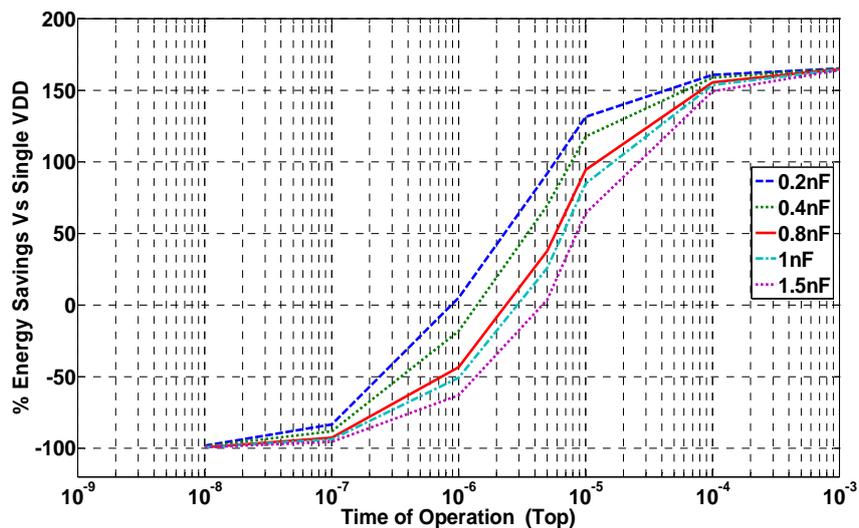


Figure 14 shows how the PDVS savings for the same scenario as before will change as a function of the capacitance of the virtual VDD rail of each PDVS block. As the capacitance of the block increases, the breakeven time moves to larger times, meaning that the workload needs to remain at a new value for a longer time to make it worthwhile to switch the voltage of that block.

**Figure 14.** Energy Benefits of PDVS for different values of the virtual VDD capacitance of the block.



**5. Conclusions**

A model that can accurately capture the behavior of inductor based DC-DC converters in a dynamic environment has been presented. The converter model has been validated and compared with measured results from a variety of DC-DC converter topologies in existing literature. We use this model to study

block level power management techniques for a SoC by incorporating it into a higher level model of the multiple block system. The system model predicts that there is a break-even time before the benefit of voltage scaling becomes positive, and our proposed modeling framework provides a quantitative means for comparing multiple power management techniques in a given use case scenario.

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