Combined SRAM Read/Write Assist Techniques for Near/Sub-Threshold Voltage Operation

Farah B. Yahya[1], Harsh N. Patel[1], Vikas Chandra[2], Benton H. Calhoun[1]
[1]University of Virginia, Charlottesville, VA USA
[2]ARM Inc., San Jose, CA USA
[1]Email: fby5bb@virginia.edu

Abstract

This paper investigates the use of combined read and write assist techniques to reduce the minimum operating voltage (V_{MIN}) of the 6T SRAM bit-cell. While write failures initially limit V_{MIN}, applying write assist introduces row and column half-select failures. Thus, read and write assist must be combined to allow scaling V_{MIN} down to near/sub threshold voltages. We find that combining negative bitline (BL) for write assist with array V_{DD} boosting for read assist is most effective for reducing the array V_{MIN} and eliminating half-select failures for commercial 130nm and sub-20nm FinFET technologies across different process corners and temperatures. The proposed combination results in the highest reduction in SRAM V_{MIN} (to 300mV for FinFET and to 600mV for 130nm CMOS). This paper also shows that controlling the degree of applied assist based on the chip corner will allow further reductions in V_{MIN} for the 130nm CMOS (to 450mV) and the required assist needed to achieve V_{MIN} for both the FinFET and the 130nm bit-cells.

Keywords

SRAM V_{MIN}, near/sub-threshold operation, read assist, write assist.

1. Introduction

With the growing demand for mobile and wearable devices and the rising focus on the internet of things (IoT), developing ultra-low power (ULP) circuits that can operate on a limited battery supply or harvested energy has become essential [1]. For devices that do not require high performance such as bio-sensors, speed can be sacrificed for lower power. Thus, these devices usually use older technologies with lower performance but much reduced leakage currents (such as 130nm CMOS). However, for many devices (such as smart phones/tablets), performance cannot be traded off for energy efficiency. These devices are usually fabricated in state-of-the-art technologies (such as FinFET) and have both high performance (HP) and low power (LP) cores that can be used interchangeably based on the system requirements [2].

Scaling the supply voltage (V_{DD}) to near or below the threshold voltage (V_T) of the transistor is one of the most effective ways to reduce the power and energy consumption of the system [3]. However, operating at a near/sub-V_T voltage reduces the performance of the system and the reliability of some of its circuits, especially Static Random Access Memories (SRAMs). The performance concern can be addressed by dynamic voltage scaling between the nominal voltage and near/sub-V_T voltages to enable both high speed and ULP operation. The reliability of SRAMs, on the other hand, faces significant challenges at near/sub-V_T voltages due to the increased impact of process variations in that region. SRAM bit-cells depend on the relative strength of their transistors for correct operation, thus variations in V_T causes read, write, and access failures. Without applying any assist, write failures set the array V_{MIN}. Introducing write assist techniques allows us to reduce the write V_{MIN} but causes row and column half selected (HS) bit-cell failures that then become the limiting factor on V_{MIN} as we will show in later sections.

Conventional methods to avoid HS instability include operating the SRAM array at higher supply voltages, using a read-before-write approach [4], using alternative bit-cell topologies, and implementing banks with one word per row [5]. However, all these approaches have a significant impact on the power consumed and/or area occupied by the SRAM array. Different combinations of read and write assist techniques were also used to address this problem [6][7]. The authors in [6] suggested combining either negative BL (NegBL) or lowered column V_{DD} (LCV_{DD}) with under-driving WL (UDWL) to eliminate HS failures while maintaining write stability and speed. In [7], NegBL was combined with UDWL to improve both read and write stability. Both these approaches aim at improving the overall performance of the SRAM array.

In this paper, we study the use of assist techniques to reduce the array V_{MIN} and thus to lower power. We evaluate different read and write assist techniques and then propose a new combination (NegBL with array V_{DD} boosting) that allows reduction of the overall array V_{MIN} down to near/ sub-V_T voltages. The proposed combination is compared to the combinations presented in [6] and [7] for two technology nodes (commercial 130nm CMOS and sub-20nm FinFET technologies). These technologies are chosen since they are commonly used for low power [1] and high performance applications [7], respectively.

The rest of the paper is organized as follows: Sections 2 and 3 present the evaluation of write and read assist techniques, respectively. Even though this evaluation has been performed in the literature [8][9], we will study the effects of assist on both the write stability of a selected cell and the read/hold stability of row and column HS cells for a wider supply voltage range and use sensitivity analysis [10] to explain the unique results observed at lower supply voltages. Then, Section 4 introduces our proposed combined read/write assist technique used to reduce V_{MIN}, evaluates

and compares it to different combinations available in the literature. Section 5 presents the advantages of using the data from a process monitor to control the applied assist. Finally, Section 6 concludes the paper.

2. Write Assist Evaluation

In this section, the different write assist techniques – WL boosting (BWL), LCV_{DD}, and NegBL – are evaluated individually for 130nm and FinFET bit-cells. For the FinFET bit-cell, nominal V_T transistors are used to allow high performance; whereas, for the 130nm bit-cell, high V_T transistors are used to reduce power consumption. Since performance is not a priority at lower supply voltages, we chose the static write margin (WM) as the evaluation metric. To measure the WM, we swept WL from 0 to V_{DD} and recorded the WL voltage (WL_{switch}) at which the internal nodes switch their data. The WM is then defined as the difference between V_{DD} and WL_{switch} [11]. Then, Monte-Carlo simulations were used to measure the worst case WM at the Slow N, Fast P (SF) corner with a temperature (T) of 25^0C since that corresponds to the worst case write corner. The assist voltages are chosen as different percentages of the applied V_{DD}. After evaluating the impact of write assist techniques on WM, we study their impact on the RSNM and HSNM [12] of row and column HS bit-cells at the worst case HS corner (Fast N, Fast P (FS) corner, T=100^0C).

2.1 Write Stability

Figure 1 shows the impact of different write assist techniques on the write V_{MIN}. For the 130nm bit-cell, high percentages of assist (40%) are required to reduce V_{MIN} of the accessed cells only down to sub-V_T voltages. Introducing (40%) NegBL lowers the write V_{MIN} down to 450mV, while BWL and LCV_{DD} reduce V_{MIN} further down to 400mV. On the other hand, for the FinFET bit-cell, applying 10% BWL or LCV_{DD} is enough to drive the write V_{MIN} to 350mV, while NegBL reduces V_{MIN} down to 400mV only.

For the 130nm bit-cell, BWL shows the most improvement in WM at V_{DD} higher than 500mV, whereas LCV_{DD} shows the most improvement at lower V_{DD}s. To explain the change in the most effective assist with V_{DD}, Figure 2 shows the sensitivity of the WM to changes in the V_T of each of the six transistors. The WM is very sensitive to changes in the V_T of device PGR (Figure 3). Devices PUR, PDL, and PGL also impact the WM, while PUL and PDR

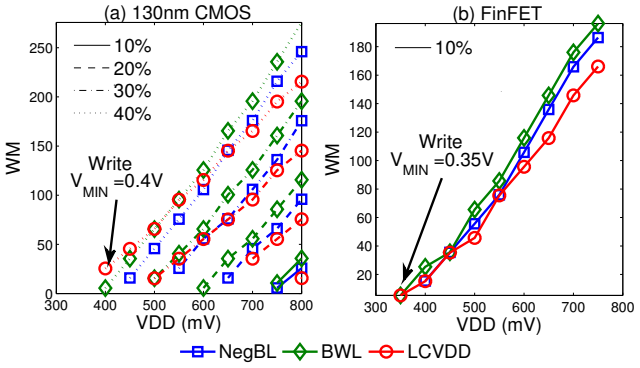

Figure 1: Impact of write assist on WM at the worst case write corner (SF 25^0C).

have negligible impact on WM. Since BWL improves the strength of both PGR and PGL, it gives the highest WM at high V_{DD}s. NegBL improves the strength of PGR only and thus gives a lower WM than BWL. Even though LCV_{DD} reduces the strength of PUR, at high V_{DD}s, WM is more sensitive to changes in PGR, and thus LCV_{DD} gives lower WM than BWL and NegBL. As V_{DD} is scaled however, the sensitivity of WM to changes in PUR and PDL increases, and thus LCV_{DD} becomes more effective at lower V_{DD}s, since it reduces the strength of both PUR and PDL. Similarly for the FinFET bit-cell, BWL shows the most improvement in WM, and LCV_{DD} becomes more effective at V_{DD}s lower than 450mV.

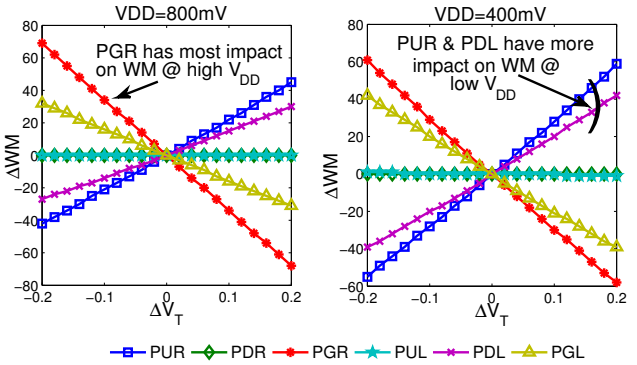

Figure 2: Sensitivity of WM to changes in V_T of the SRAM transistors at different V_{DD} values.

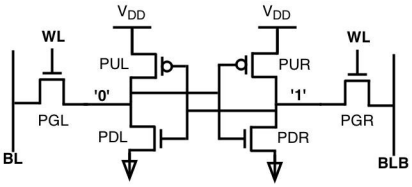

Figure 3: The 6T SRAM bit-cell.

2.2 Half Select Stability

Even though the different assist techniques reduce the write V_{MIN} (Section 2.1), they negatively impact the SNM of row and column HS bit-cells, which share the WL and BLs of the selected cells, respectively. Both LCV_{DD} and NegBL reduce the HSNM of column HS bit-cells but have no impact on the RSNM of the row HS bit-cells. BWL, on the other hand, has no impact on the HSNM of column HS bit-cells but lowers the RSNM of row HS bit-cells, causing the HS V_{MIN} to increase as shown in Figure 4. For the 130nm bit-cell, applying 40% BWL increases the row HS read limited V_{MIN} from 700mV to above 800mV, while applying 40% LCV_{DD} or NegBL degrades the HSNM and raises the column HS V_{MIN} from 350mV to 750mV and above 800mV, respectively. Similarly, for the FinFET bit-cell, applying 10% BWL increases the HS V_{MIN} from 400mV to 550mV. Applying 10% LCV_{DD} or NegBL degrades the HSNM but does not raise the column HS V_{MIN}.

To understand the impact of write assist on the RSNM and HSNM, Figure 5 and Figure 6 show the sensitivity of these margins to changes in the V_T of the SRAM transistors. At high V_{DD}s, the RSNM is most sensitive to PGL and PDR (Figure 3). PUR and PDL also impact RSNM while PUL and PGR have negligible impact. At lower V_{DD}s, PUR and

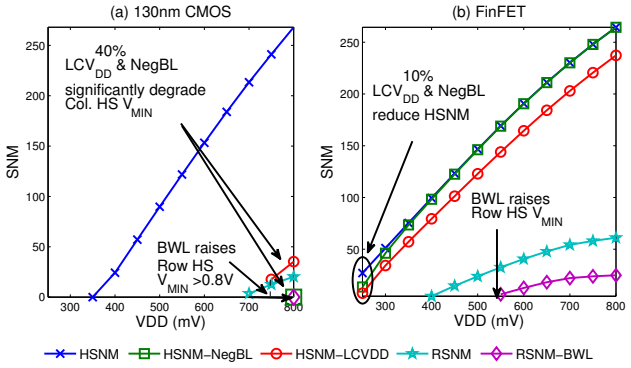

Figure 4: Impact of write assist techniques on HS bit-cells ((a) 40% for 130nm, (b)10% for FinFET) at the worst case HS corner (FS 100^{0}C).

PDL have a higher impact on RSNM. However, when the V_T of PUR is above a certain limit, its impact on RSNM becomes fixed. When PGR is strong (lower V_T), it helps improve RSNM since BLB is high and leakage currents through PGR help retain the data. This trend is more obvious at lower V_{DD}s since the I_{ON}/I_{OFF} is lower and thus leakage current through PGR is comparable to current through PUR. BWL improves the strength of PGL, causing the node holding '0' to rise and reduce the strength of PUR and improve the strength of PDR. This effect reduces the RSNM, causing the number of failures and the HS V_{MIN} to increase.

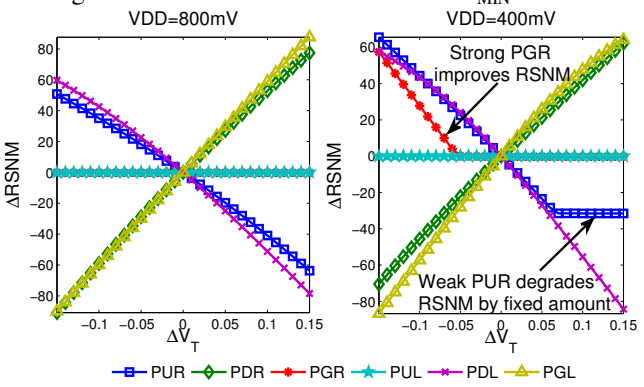

Figure 5: Sensitivity of RSNM to changes in V_T of the SRAM transistors at different V_{DD} values.

According to Figure 6, the HSNM is most sensitive to PUR and PDR at high V_{DD}s. However, at lower V_{DD}s, the impact of PUR increases. When PGR is strong, it negatively impacts the HSNM since the leakage current through it is comparable to the on current through PUR and the fight between the two transistors will determine the voltage at the node holding '1'. Applying 40% NegBL on BLB will increase the strength of PGR, turning it partially on and causing the bit-cell to lose its data even at high V_{DD} values. Applying 40% LCV_{DD} degrades the strength of PUR and thus increases the HS V_{MIN} up to 750mV. At higher V_{DD}s, the HSNM is less sensitive to PUR changes. This causes the HSNM to reduce significantly but remain positive.

To reduce the write V_{MIN} down to sub-V_T voltages, the 130nm and FinFET bit-cells require 40% and 10% applied write assist, respectively. Table 1 summarizes the impact of applying these percentages of write assist on the write and HS V_{MIN}. Even though write assist techniques reduce the

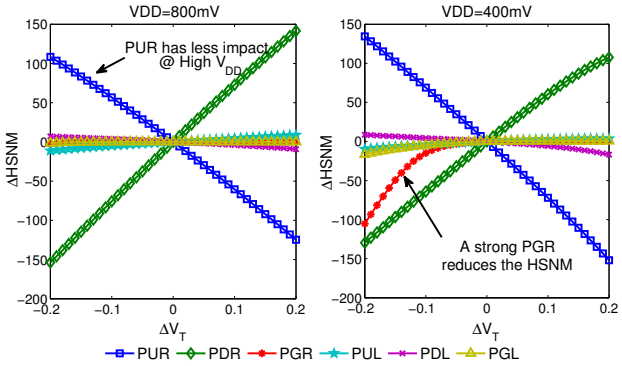

Figure 6: Sensitivity of HSNM to changes in V_T of the SRAM transistors at different V_{DD} values.

write V_{MIN}, they increase the HS V_{MIN}, thus limiting the array level V_{MIN}. Column based write assist techniques (LCV_{DD} and NegBL) degrade the hold stability (HSNM) of column HS bit-cells and have no impact on the row HS bit-cells. On the other hand, row based write assist techniques (BWL) have no impact on the hold stability of column HS bit-cells but significantly degrade the read stability (RSNM) of row HS bit-cells. In both cases, write assist techniques reduce the write V_{MIN} below the HS V_{MIN} making HS failures the limiting factor on the array V_{MIN}.

Table 1: Write and HS V_{MIN} for 130nm & FinFET bit-cells with 40% & 10% applied write assist (WA).

	130nm (40% WA)		*FinFET (10% WA)*	
(in mV)→	*Write V_{MIN}*	*HS V_{MIN}*	*Write V_{MIN}*	*HS V_{MIN}*
No Assist	>800	700	500	400
NegBL	450	>800	350	400
LCV_{DD}	400	750	400	400
BWL	400	>800	350	550

3. Read Assist Evaluation

In the previous section, we determined that HS failures will limit the array V_{MIN} when write assist techniques are employed. In this section, we evaluate the impact of read assist techniques – boosting V_{DD} (RV_{DD}) and UDWL – on the write and HS V_{MIN}. Monte-Carlo simulations at different process corners showed that the FS corner is the worst case corner for the HS bit-cells. Thus, the FS corner with T=100^{0}C was used to measure the worst case RSNM.

3.1. Half Select Stability

Figure 7 shows the impact of read assist techniques on the worst case RSNM at different V_{DD}s. Without any read assist, the 130nm row HS bit-cells experience a read upset for V_{DD}s below 700mV. Applying 20% UDWL improves the RSNM of these bit-cells and enables correct functionality down to 500mV. Applying 20% RV_{DD} provides additional improvements in the RSNM and lowers the HS V_{MIN} further down to 450mV. Similarly, for the FinFET bit-cell, both UDWL and RV_{DD} improve the RSNM and reduce HS V_{MIN} down to 300mV.

RV_{DD} shows more improvement in the RSNM than UDWL. Referring back to Figure 5, UDWL reduces the strength of PGL, which means that the voltage on node '0'

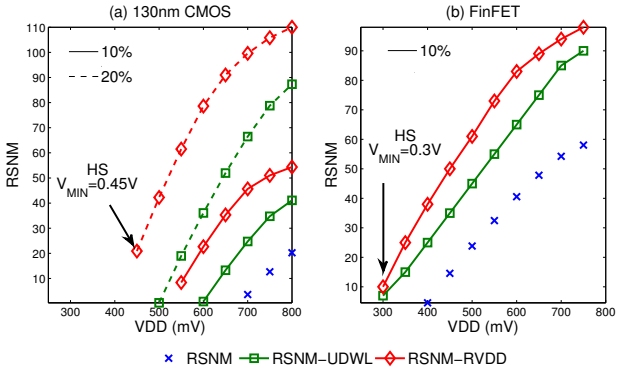

Figure 7: RSNM vs. V_{DD} for different read assist techniques in (a) 130nm & (b) FinFET at FS 100^{0}C.

does not rise significantly, and thus PDR is kept firmly off. On the other hand, RV_{DD} improves the strength of PUR and PDL (since the gate of PDL is driven by a higher bias). A stronger PDL also means node '0' remains low keeping PDR firmly off. At lower V_{DD}s, the sensitivity of RSNM to changes in PUR and PDL increases making RV_{DD} more effective at improving the RSNM and reducing the HS V_{MIN}.

3.2. Write Stability

Read assist techniques improve the read stability of row HS bit-cells at the cost of degraded write stability in selected bit-cells. The 130nm bit-cell fails to write without write assist techniques; applying read assist techniques will only increase the number of failing bit-cells within the array at a particular voltage. Figure 8 shows the impact of read assist techniques on the WM of the FinFET bit-cell. UDWL degrades the strength of PGR and PGL. Since those transistors have a high impact on WM (Figure 2), UDWL raises the write V_{MIN} of the FinFET up to 650mV. On the other hand, RV_{DD} improves the strength of PUR and PUL but since these transistors have less impact on WM, RV_{DD} raises the write V_{MIN} only to 550mV.

To reduce the HS V_{MIN} to near/sub-V_T voltages, the 130nm and FinFET bit-cells need 20% and 10% read assist applied, respectively. Table 2 shows the impact of applying these percentages of assist on the write and HS V_{MIN}.

4. Proposed Read/Write Assist Combination

Using read and write assist techniques independently does not reduce the overall array V_{MIN}. Thus, we propose combining NegBL (write assist) and array RV_{DD} (read assist)

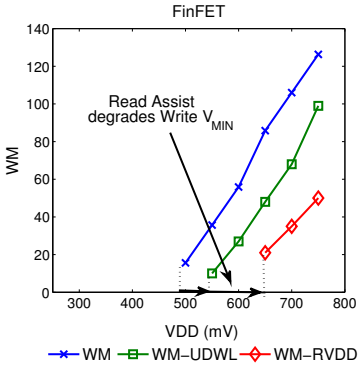

Figure 8: Impact of read assist techniques on WM for FinFET bit-cells at FS 100^{0}C.

Table 2: Write & HS V_{MIN} for 130nm & FinFET bit-cells with 20% & 10% applied read assist (RA).

	130nm (20% RA)		*FinFET (10% RA)*	
(in mV) →	*Write V_{MIN}*	*HS V_{MIN}*	*Write V_{MIN}*	*HS V_{MIN}*
No Assist	>800	700	500	400
RV_{DD}	>800	450	550	300
UDWL	>800	500	650	300

to achieve a lower array V_{MIN}. Array V_{DD} is defined as the V_{DD} of the SRAM bit-cell array only, excluding drivers and peripherals. In this section, we evaluate the proposed technique of RV_{DD}-NegBL and compare it to the two previously proposed combinations [6][7]. We define UDWL–NegBL as the combination of UDWL (read assist) and NegBL (write assist) proposed in [6][7], and UDWL–LCV_{DD} as the combination of UDWL (read assist) and LCV_{DD} (write assist) proposed in [6]. Table 3 summarizes the changes to the WL, BL and V_{DD} for each combination as compared to the no assist case.

Table 3: WL, BL & V_{DD} conditions for the studied combinations.

	RV_{DD}-NegBL	UDWL-NegBL	UDWL-LCV_{DD}
WL	No change	*Under-driven*	*Under-driven*
BL	*Negative bias*	*Negative bias*	No change
V_{DD}	*Boosted for Array*	No change	*Lowered for column*

Since the RSNM and HSNM are pessimistic measures of HS failure, in this section, we look at dynamic HS failures by running transient simulations with a relaxed WL pulse width. Figure 9 shows the impact of applying different percentages of NegBL on the write delay of the 130nm and FinFET bit-cells. For the 130nm bit-cell, column HS failures limit the percentage of NegBL that could be applied to below 40%. Applying 30% NegBL reduces the write V_{MIN} from above 800mV to 550mV, however, row HS failures limit the array V_{MIN} to 650mV. For the FinFET bit-cell, introducing 30% NegBL reduces the write V_{MIN} from 500mV to 250mV. However, row HS bit-cells fail at 350mV limiting the array V_{MIN}.

To address the row HS failures, 10% or 20% UDWL is applied simultaneously with 30% NegBL. Since UDWL does not reduce the column HS failures, a higher percentage of NegBL cannot be used for the 130nm bit-cell. Figure 10

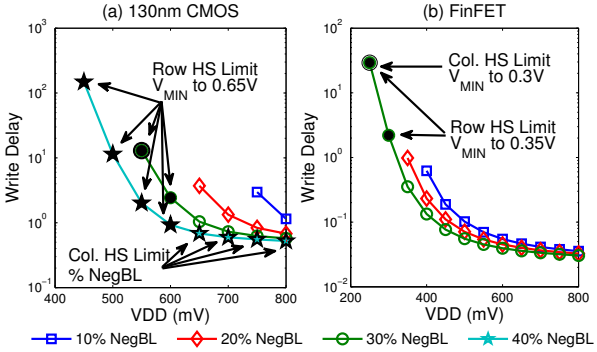

Figure 9: Impact of NegBL on the write delay of (a) 130nm & (b) FinFET bit-cells – black filled markers indicate HS failures.

shows the impact of combining 30% NegBL with different percentages of UDWL for the 130nm and FinFET bit-cells. Even though UDWL reduces the row HS V_{MIN}, it increases the number of write failures and raises the write V_{MIN}. Combining 10% UDWL with 30% NegBL does not change the array V_{MIN}. Reducing the WL further (20% UDWL) will significantly degrade the write V_{MIN} resulting in an overall degradation in the array V_{MIN}. For the FinFET bit-cell, applying 10% and 20% UDWL reduces the number of row HS failures but does not eliminate them completely. UDWL (20%) also increases the number of write failures resulting in an overall array V_{MIN} degradation. Thus, UDWL-NegBL does not provide any advantages in V_{MIN} over using only NegBL.

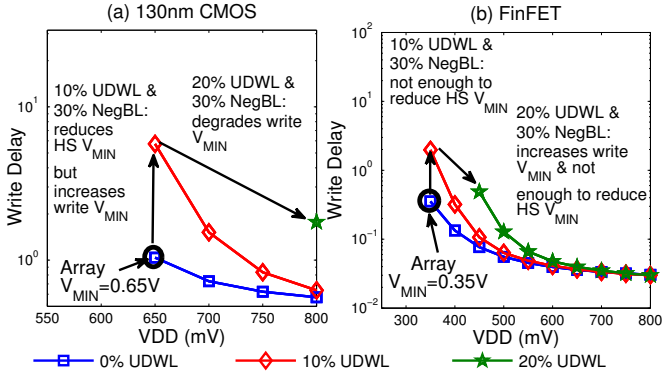

Figure 10: Impact of UDWL-NegBL [6][7] on the write delay for (a) 130nm & (b) FinFET bit-cells.

UDWL can also be combined with LCV_{DD} to reduce the overall array V_{MIN}. Figure 11 shows the impact of applying 30% LCV_{DD} with UDWL. While this combination reduces the HS and write V_{MIN}, developing enough BL/BLB differential to perform a correct read operation is not possible with the UDWL (black marker in Figure 11). Thus, differential read V_{MIN} limits the overall 130nm array V_{DD} to 650mV. For the FinFET bit-cell, 10% UDWL is not enough to reduce the HS V_{MIN} and further under-driving will degrade the write V_{MIN}.

RV_{DD}–NegBL improves V_{MIN} most effectively. Boosting the array V_{DD} helps address both row and column HS failures allowing a lower NegBL to be used if needed. It also improves the read capabilities of the bit-cell and ensures

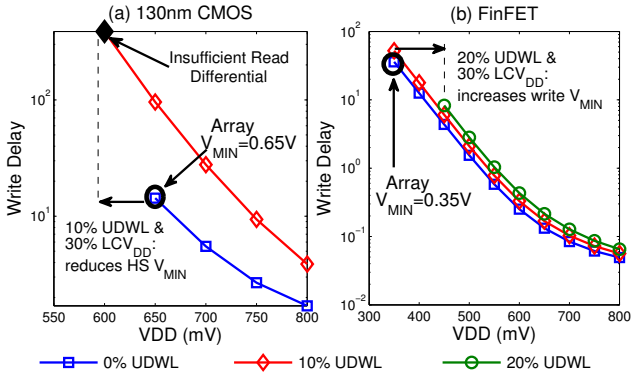

Figure 11: Impact of UDWL-LCV_{DD}[6] on the write delay for (a) 130nm & (b) FinFET bit-cells – black filled marker indicates read failure.

enough BL/BLB differential is developed for a correct read operation. **Figure 12** shows the impact of combining 30% NegBL with different percentages of array RV_{DD} for the 130nm and FinFET bit-cells. 10% RV_{DD} is enough to reduce the row HS failures and V_{MIN} down to 600mV. 20% RV_{DD} increases the write V_{MIN} (to 700mV) and reduces the HS failures but does not allow a higher percentage of NegBL assist. 30% RV_{DD} improves the column HS V_{MIN} allowing 40% NegBL to be used. However, this combination does not reduce the array V_{MIN} below 650mV. Similarly for the FinFET bit-cell, 15% RV_{DD} allows 40% NegBL to be used and reduces the array V_{MIN} down to 300mV. Even though a large percentage of NegBL is required to push V_{MIN}, the drive voltage across the access transistors and within the NegBL generation circuit does not exceed the V_{MAX} of the technology, thus oxide breakdown is not a concern.

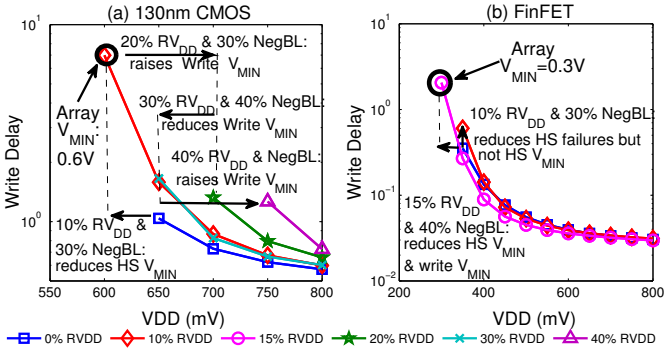

Figure 12: Impact of RV_{DD}-NegBL on the write delay for (a) 130nm & (b) FinFET bit-cells.

Table 4 summarizes the comparison between the proposed combination (RV_{DD}-NegBL) and the combinations in [6] and [7]. RV_{DD}-NegBL is the most effective combination for reducing the array V_{MIN} to near/sub-V_T voltages. The combination of read and write assist techniques provide significant improvement in V_{MIN} compared to the V_{MIN} achieved by applying no assist techniques. The proposed combination provides more than 25% improvement in V_{MIN} for the 130nm array and 40% for the FinFET array over the no assist case. Compared to the most effective write assist technique (BWL from Table 1), the proposed combination provides more than 20% improvement in the V_{MIN} for the 130nm array and 25% improvement for the FinFET array.

Table 4: V_{MIN} comparison between the proposed assist combination, [6], [6][7] and the no assist (NA) and best write assist (WA) V_{MIN} (Table 1).

		Array V_{MIN} (mV)	*% lower V_{MIN} vs. NA*	*% lower V_{MIN} vs. WA*
130nm CMOS	Proposed	600	>25%	>20%
	[6][7]	650	>19%	>13%
	[6]	650	>19%	>13%
FinFET	Proposed	300	40%	25%
	[6][7]	350	30%	13%
	[6]	350	30%	13%

5. Assist Control by Process Corner

If a process monitor is available within the system, knowledge of the process corner can help in reducing V_{MIN} and the degree of assist needed to achieve this V_{MIN}. Since the worst case write corner (SF) is different than the worst case HS corner (FS), the required assist at any particular process corner will be relaxed. Thus, we ran Monte-Carlo simulations for the proposed combination of read/write assist (RV_{DD}-NegBL) at each process corner at two temperatures (25^0C and 100^0C) to determine the required assist percentages to reduce V_{MIN}.

Table 5 shows the percentages of NegBL and array RV_{DD} required for the 130nm array to achieve a V_{MIN} of 450mV. For the Typical N, Typical P (TT) and Slow N, Slow P (SS) corners, applying 10% NegBL is enough to guarantee correct write operation without disturbing row and column HS cells down to 450mV. At the Fast N, Fast P (FF) corner, write assist is not required down to 450mV but 10% RV_{DD} is needed to address HS failures at this V_{MIN}. For the worst case write corner (SF), only 40% NegBL is needed since at this corner row and column HS are not disturbed. At the worst case HS corner (FS), 20% RV_{DD} will eliminate HS disturbances and no write assist is required.

Table 5: Required assist per corner to reduce the 130nm array V_{MIN} to 450mV.

Corner	*NegBL*	*RV_{DD}*	*V_{MIN} (mV)*
TT	10%	0%	450
SS	10%	0%	450
FF	0%	10%	450
SF	40%	0%	450
FS	0%	20%	450

For the FinFET bit-cell, controlling the assist through a process monitor does not allow further reduction in V_{MIN} but will allow us to obtain this low V_{MIN} with less aggressive applied assist (Table 6). For the SF corner, 30% NegBL is enough to ensure correct write and no read assist is required. Similarly for the FS corner, 15% array RV_{DD} along with 10% NegBL will eliminate write and HS failures. For the TT, SS and FF corners, applying 10% NegBL only is enough to achieve V_{MIN}=300mV without the need for array RV_{DD}.

Table 6: Required assist per corner to reduce the FinFET array V_{MIN} to 300mV.

Corner	*NegBL*	*RV_{DD}*	*V_{MIN} (mV)*
TT	10%	0%	300
SS	10%	0%	300
FF	10%	0%	300
SF	30%	0%	300
FS	10%	15%	300

6. Conclusion

In this paper, we proposed simultaneously boosting the array V_{DD} (bit-cells only) and applying a negative BL to reduce the V_{MIN} of SRAM arrays down to near/sub-V_T voltages while addressing row and column half select failures. We also presented a detailed evaluation of the read and write assist techniques for a wide range of supply voltages for a commercial 130nm and sub-20nm FinFET bit-cells. The proposed combination of read and write assist techniques will allow maximum reduction in the array V_{MIN} (to 600mV for the 130nm bit-cell and to 300mV for the FinFET bit-cell) when compared to other combinations available in the literature [6][7]. We also presented the advantages of employing a process monitor to control the percentages of assist applied in order to reduce the overall array V_{MIN}. For the 130nm array, controlling the applied assist per corner will allow us to reduce the array V_{MIN} to 450mV while only applying one type of assist at each corner (NegBL for TT, SS and SF and RV_{DD} for FF and FS). For the FinFET array, controlling the applied assist per corner does not reduce the achievable array V_{MIN} but it will reduce the required percentage of assist needed to achieve this V_{MIN}. The combination of read and write assist techniques is only needed for the FS corner (10% NegBL, 15% RV_{DD}). For all other corners different percentages of NegBL will allow a V_{MIN} of 300mV.

8. Acknowledgement

This work was funded in part by ARM Inc. The authors would like to thank Rob Aitken, Cezary Pietrzyk and Azeez Bhavnagarwala for their valuable input.

7. References

[1] Klinefelter, A.; et al., "A 6.45µW self-powered IoT SoC with integrated energy-harvesting power management and ULP asymmetric radios," *ISSCC,* Feb 2015

[2] *Big.LITTLE Technology: The Future of Mobile*, white paper, ARM Inc., September 2013.

[3] Wang, A.; et al. "Optimal supply and threshold scaling for subthreshold CMOS circuits," *IEEE Computer Society Annual Symposium on VLSI*, pp.5,9, 2002.

[4] Tae-Hyoung Kim; et al. "A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual Ground Replica Scheme," *ISSCC*, Feb. 2007

[5] Ik Joon Chang; et al., "A 32 kb 10T Sub-Threshold SRAM Array With Bit-Interleaving and Differential Read Scheme in 90 nm CMOS," *JSSC*, vol.44, no.2, Feb. 2009

[6] E. Karl et al, "The impact of assist-circuit design for 22nm SRAM and beyond," *IEDM,* Dec. 2012.

[7] Taejoong Song; et al. "A 14nm FinFET 128Mb 6T SRAM with VMIN-enhancement techniques for low-power applications," *ISSCC*, pp.232,233, Feb. 2014

[8] V. Chandra, et al., "On the Efficacy of Write Assist Techniques in Low Voltage Nanoscale SRAMs", *DATE,* 2010.

[9] R. W. Mann, et al., "Impact of circuit assist methods on margin and performance in 6T SRAM" *JSSC*, vol.54, no.11, Nov 2010.

[10] Boley, J.; et al., "Leveraging sensitivity analysis for fast, accurate estimation of SRAM dynamic write VMIN", *DATE*, 2013

[11] Z. Guo; et al. "Large-scale read/write margin measurement in 45nm CMOS SRAM arrays," *IEEE Symposium on VLSI Circuits,* 18-20 June 2008.

[12] Seevinck, E.; List, F.J.; Lohstroh, J., "Static-noise margin analysis of MOS SRAM cells," *JSSC*, vol.22, no.5, Oct 1987.