
# Combined SRAM Read/Write Assist Techniques for Near/Sub-Threshold Voltage Operation

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Robust Low Power VLSI

# Internet of Things

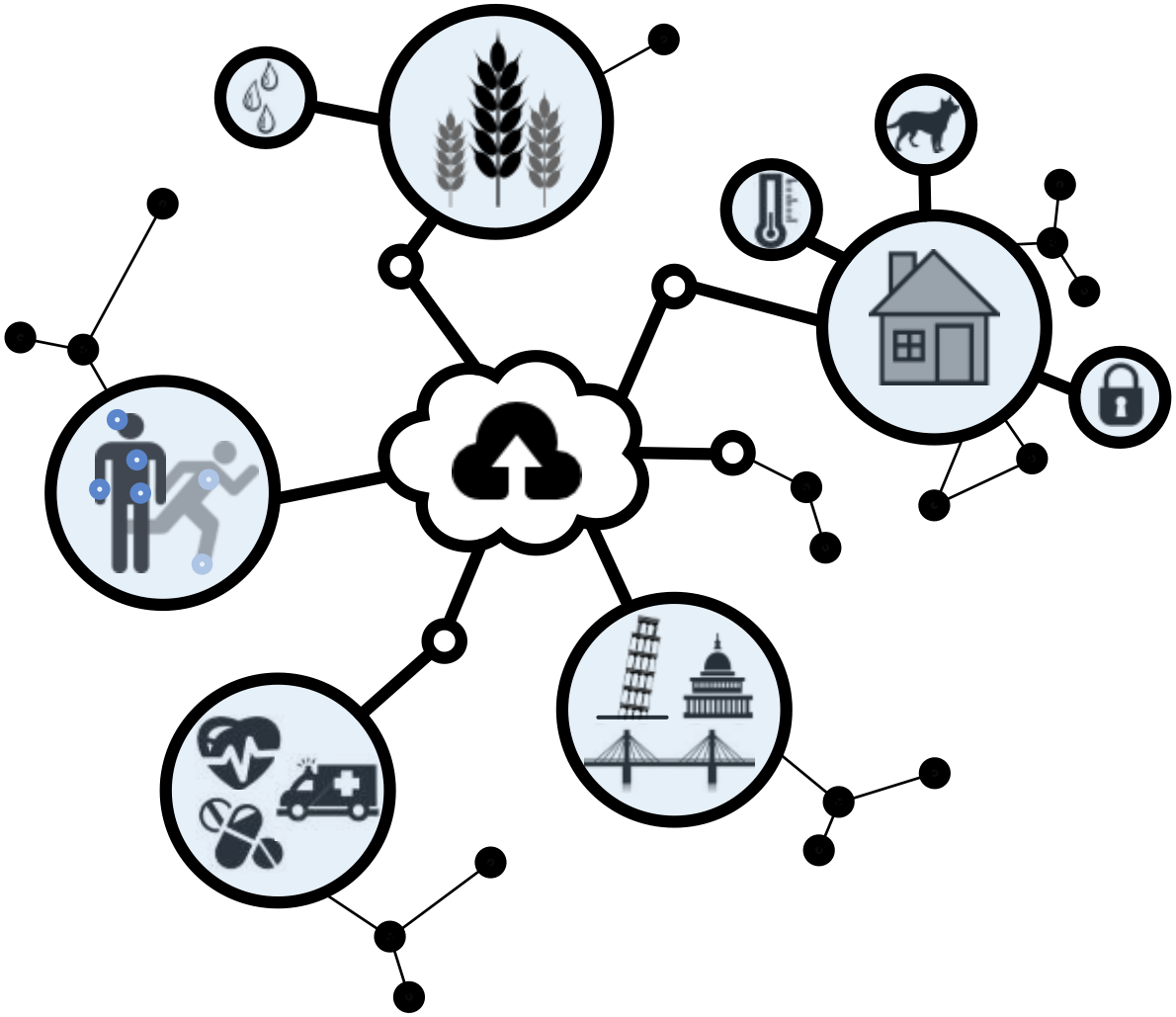
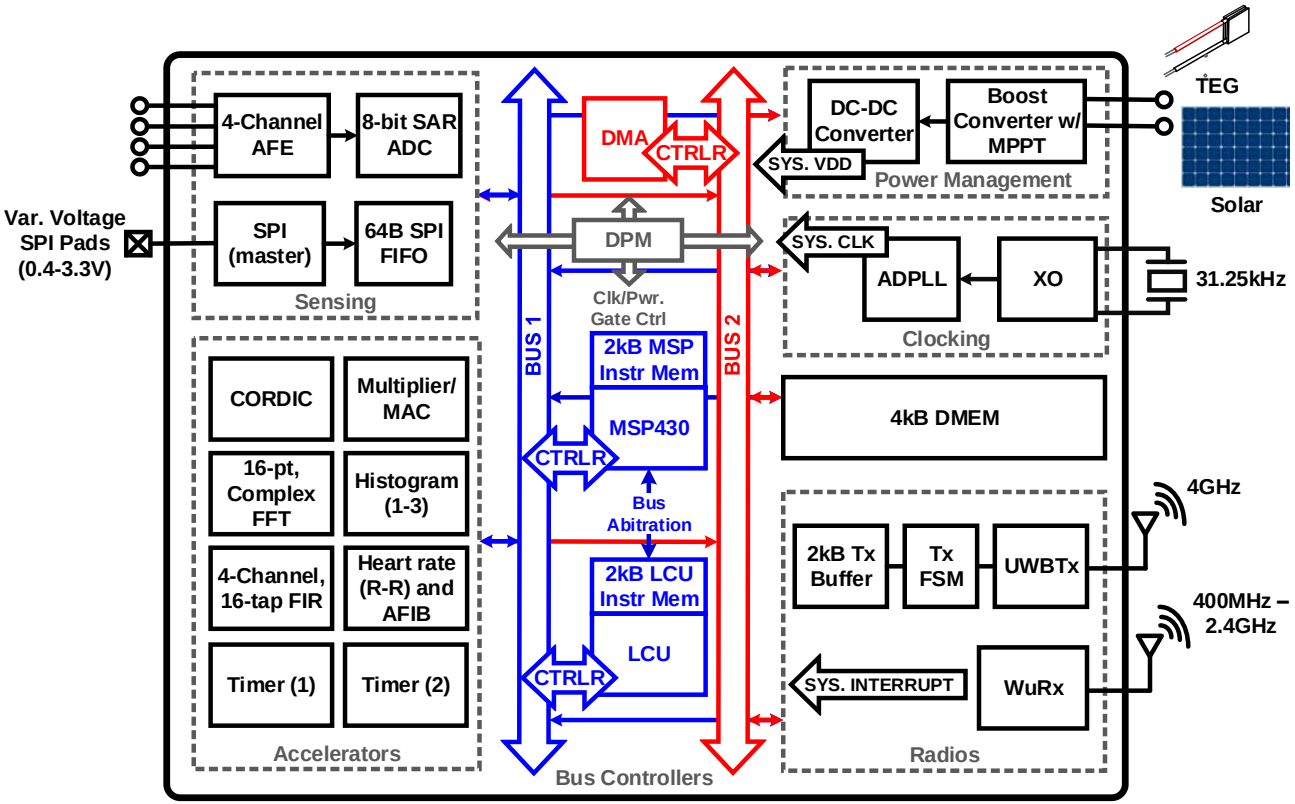


Image by Alicia Klinefelter

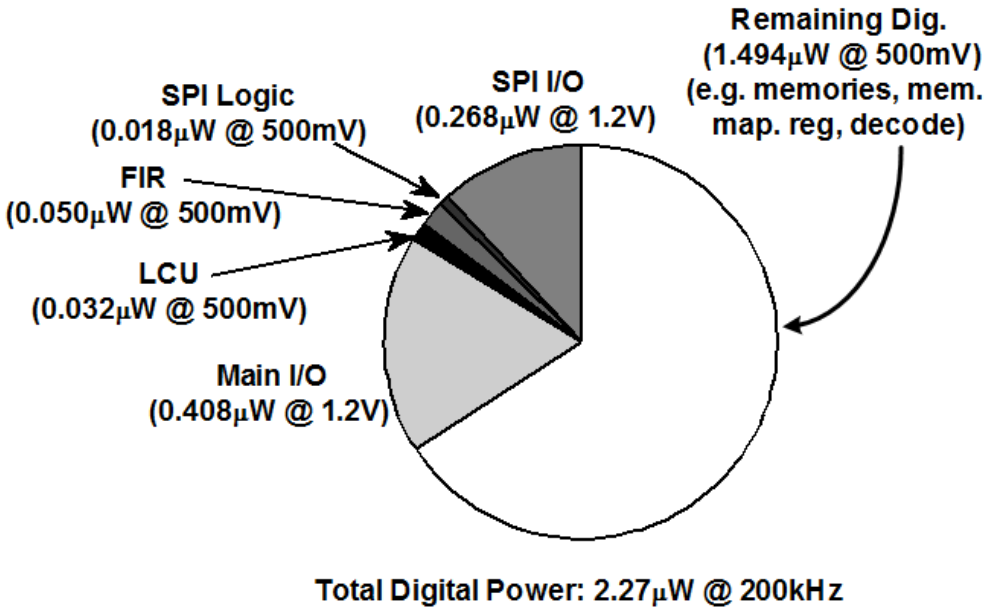
# Internet of Things




**Source:** A. Klinefelter, ISSCC 2015

**IoT specific SoCs harvest energy and operate in sub-threshold to reduce energy/power consumption**

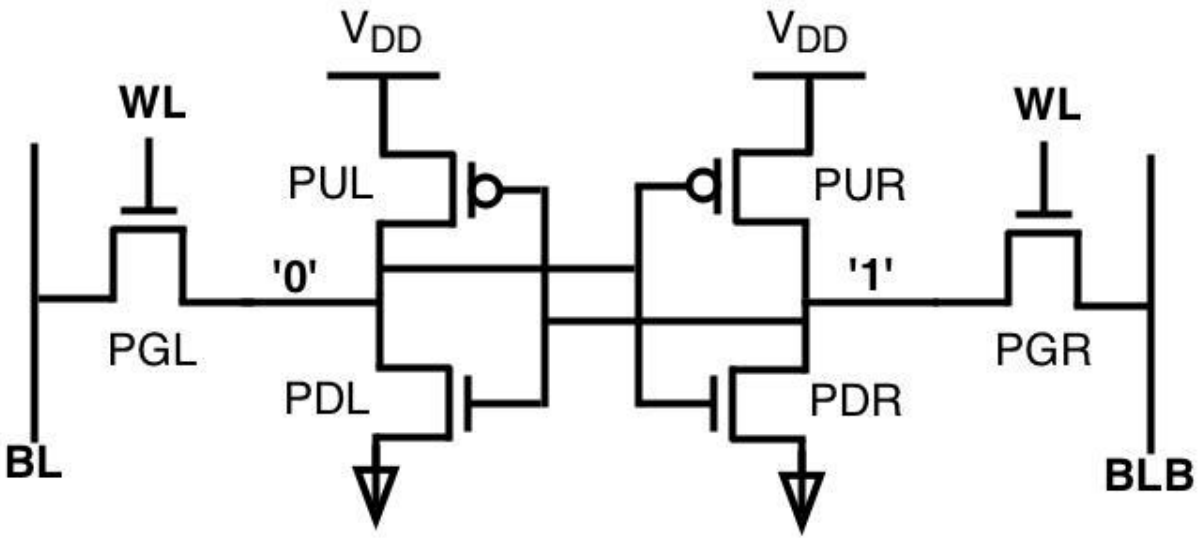
# Internet of Things




**Source:** A. Klinefelter, ISSCC 2015

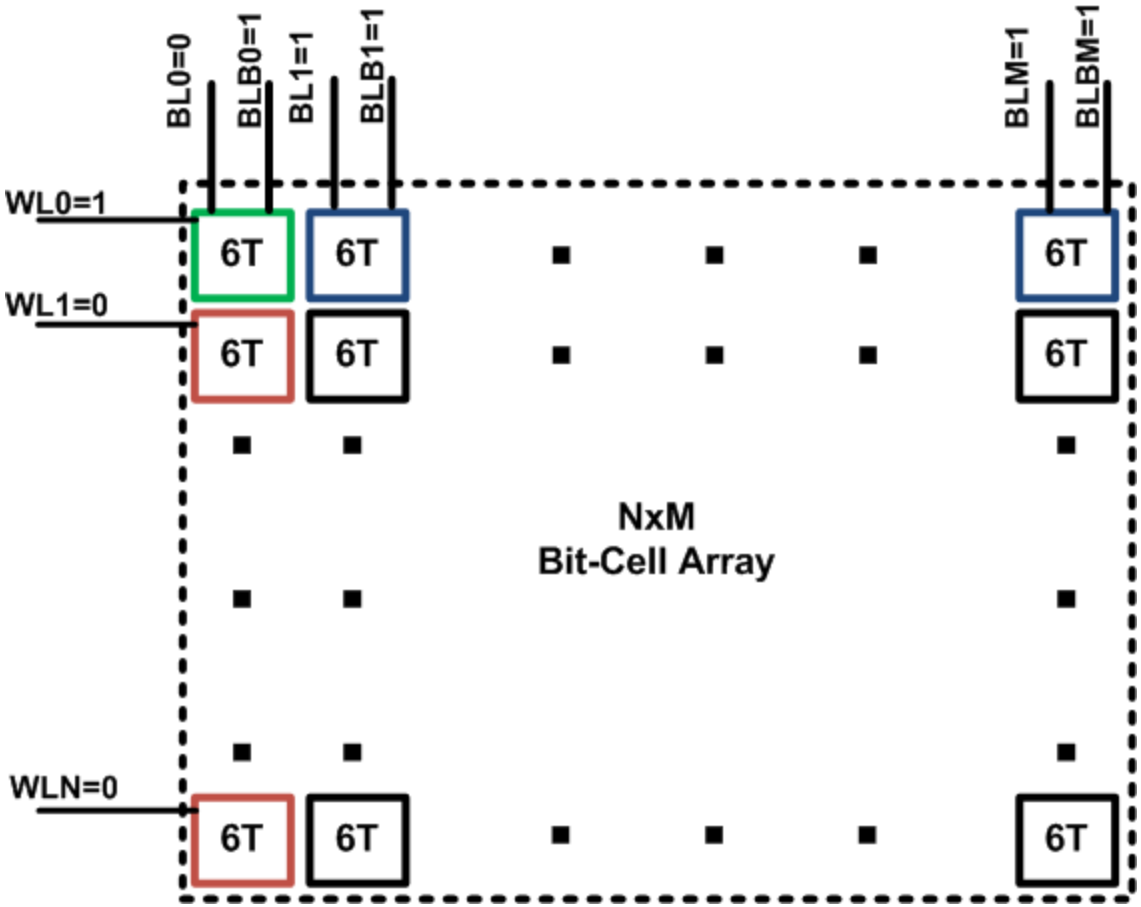
**Memory consumes a significant portion of the digital power.**

# SRAM Challenges




- Large impact of variations in subthreshold causes read and write failures.

# SRAM Challenges

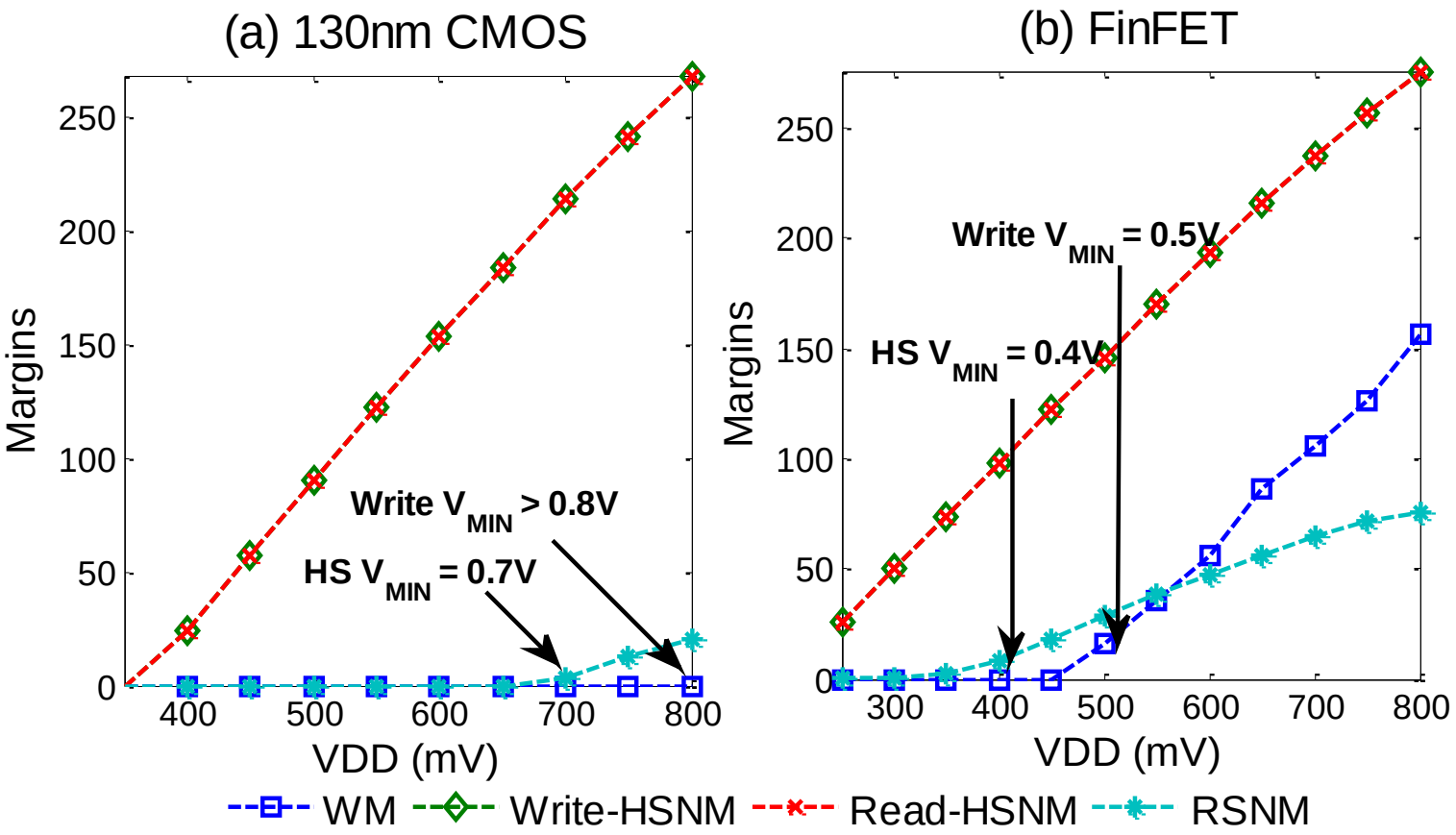



Half selected cells also experience disturb during a read/write operation which might corrupt their data

# SRAM Challenges

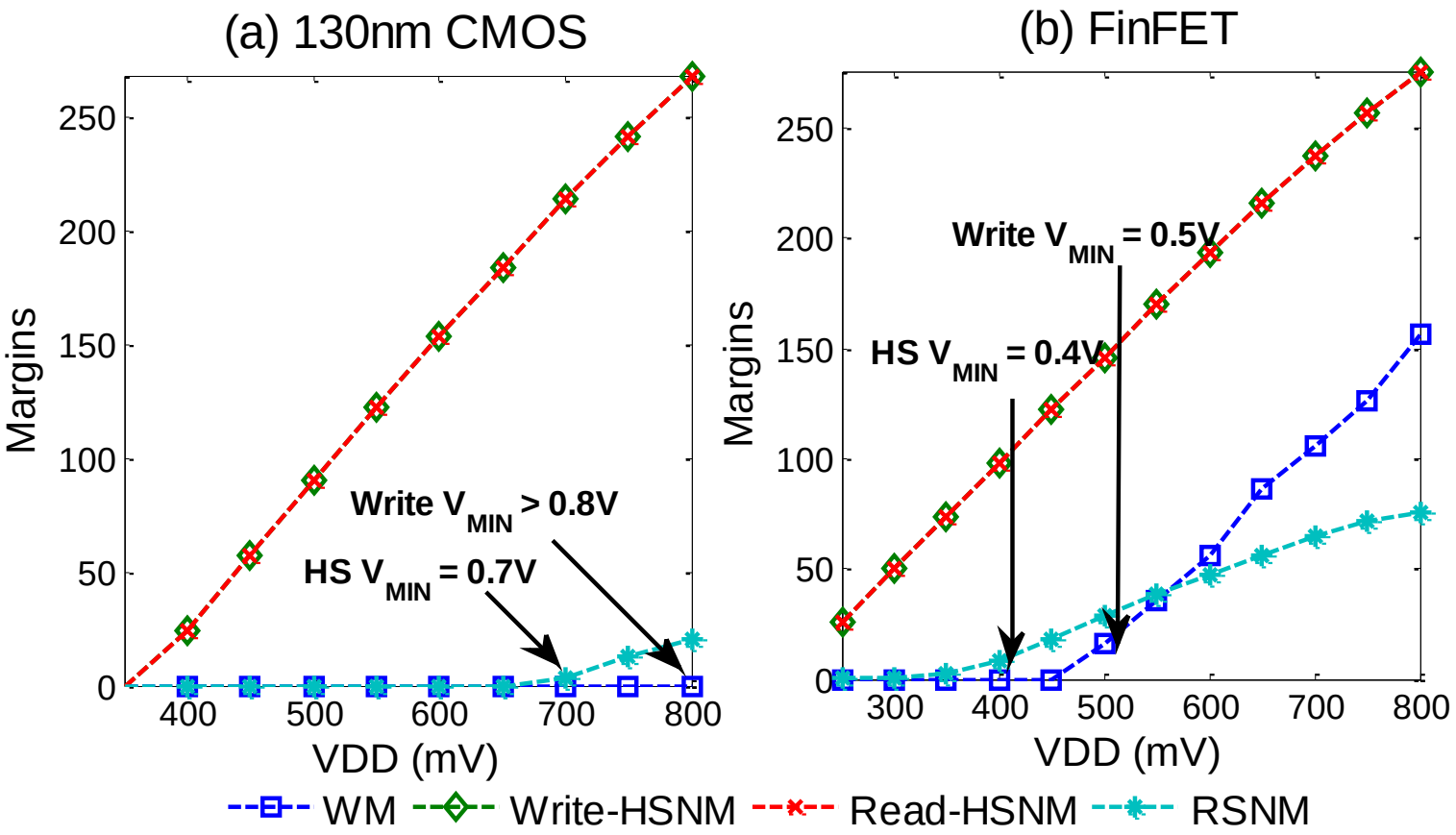
- Static margins are used as metrics
  - Performance is not a constraint for most IoT SoCs.
  - For high performance platforms, we are assuming DVFS .
- Two technologies were studied: Commercial 130nm and sub-20nm FinFET.
  - High-$V_T$ devices were used in the 130nm bit-cell.
- Monte-Carlo simulations at the worst case corner for each operation was performed.

# SRAM Challenges



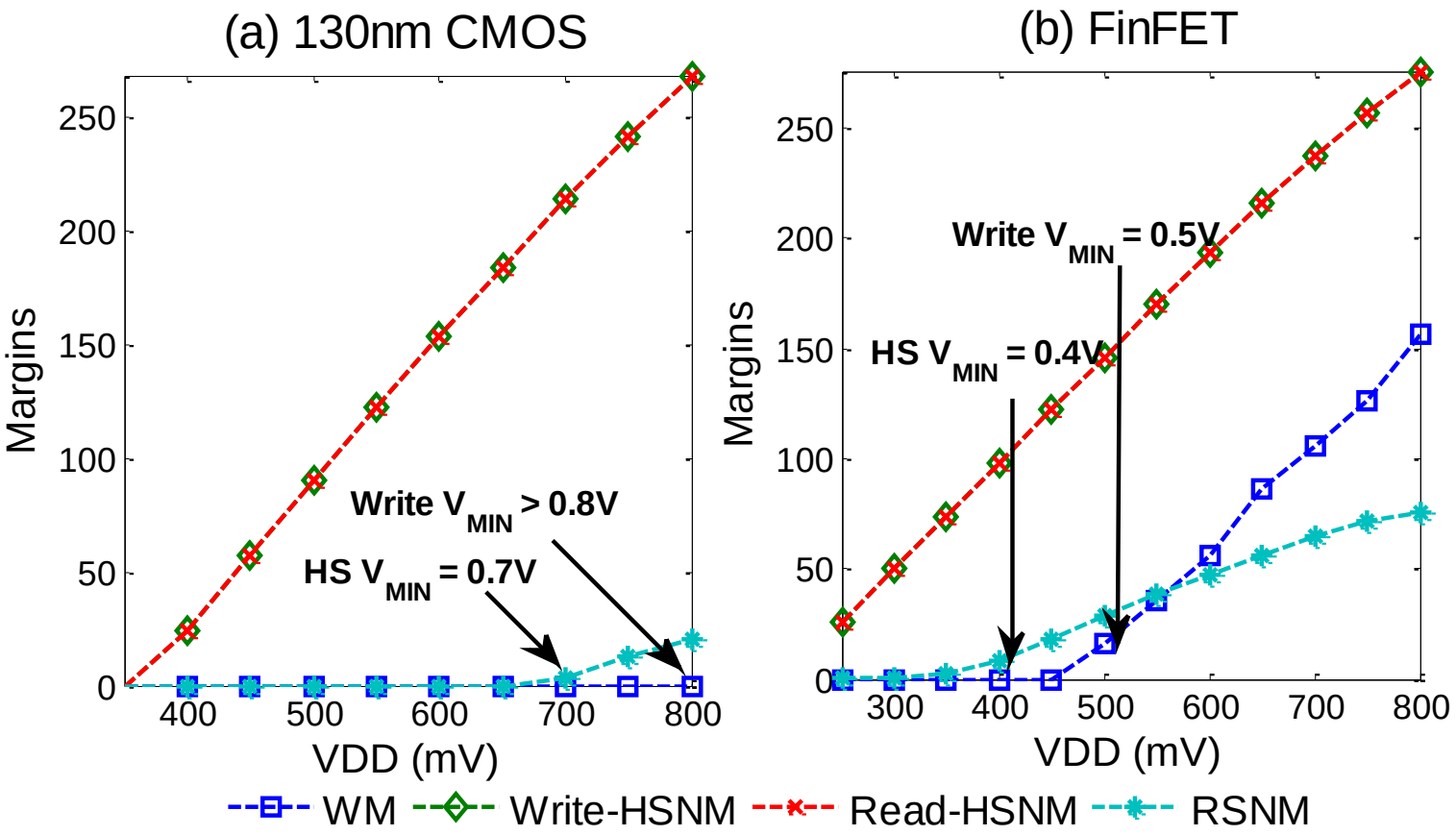

For 130nm bit-cell, write cannot be guaranteed below 0.8V and half select disturbs will occur below 0.8V

# SRAM Challenges




For FinFET bit-cell, write cannot be guaranteed below 0.5V and half select disturbs will occur below 0.4V

# SRAM Challenges




Applying a write assist technique improves the write $V_{MIN}$ but not the HS $_{VMIN}$

# Current Approaches

- Using higher $V_{DD}$ for SRAMs,
- Using alternative bit-cell topologies,
- Using a read-before-write approach,
- Implementing banks with one word per row,
- Simultaneously applying a read assist technique with a write assist technique.

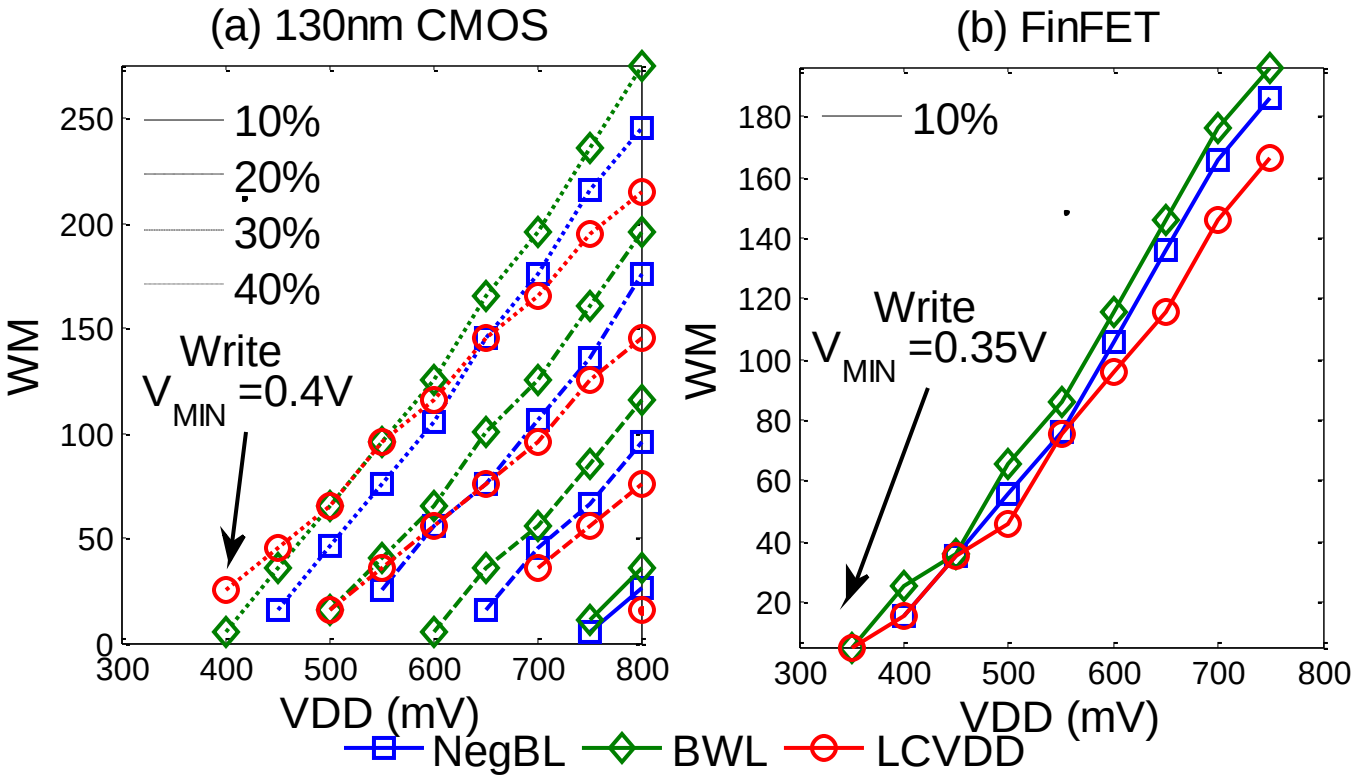
# This talk…

- Write Assist Techniques
- Read Assist Techniques
- Combined Read/Write

# Write Assist Techniques

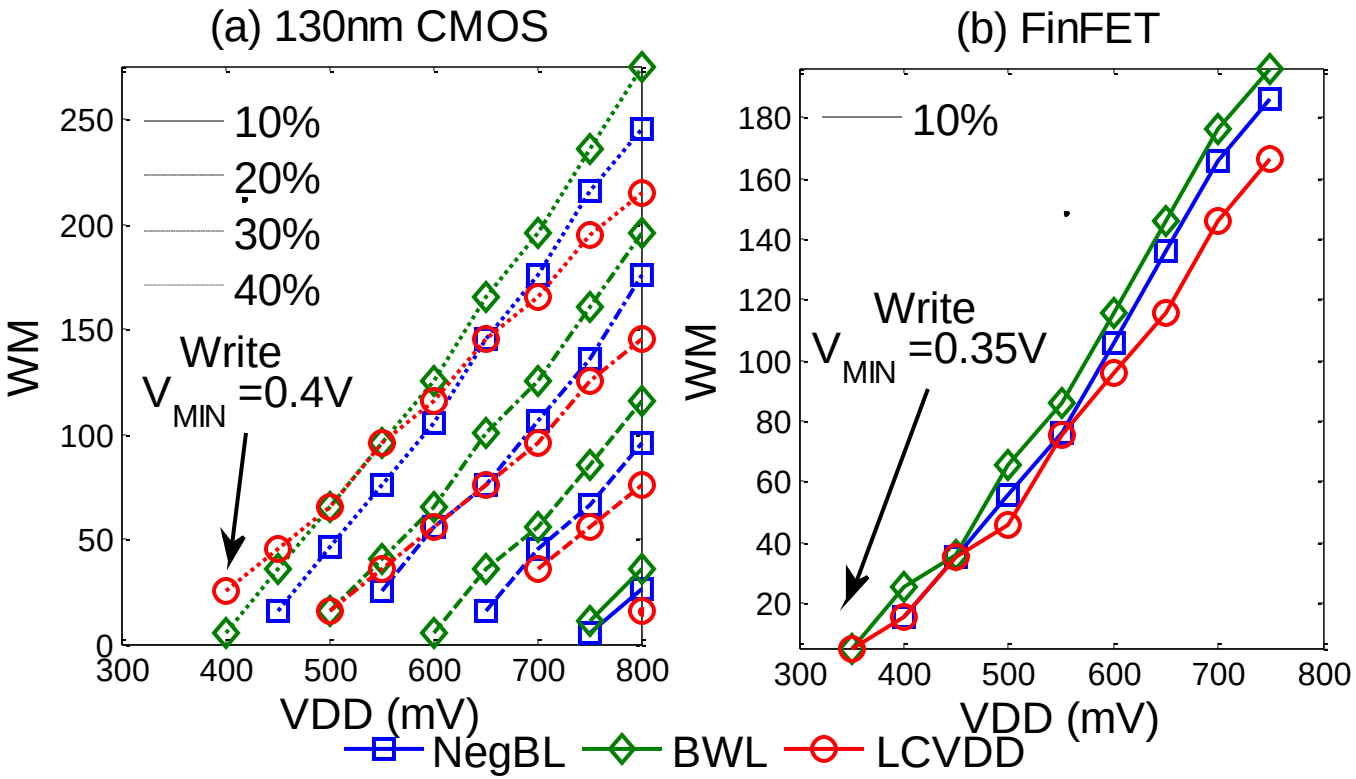
- Assist techniques: WL boosting (BWL), NegBL, and Lowering Column $V_{DD}$ ($LCV_{DD}$)
- Assist was applied as a percentage of the $V_{DD.}$
- Impact on the Write Margin across $V_{DD}$.
- Impact on the Half Select Margins across $V_{DD}$.

# Write Assist - WM



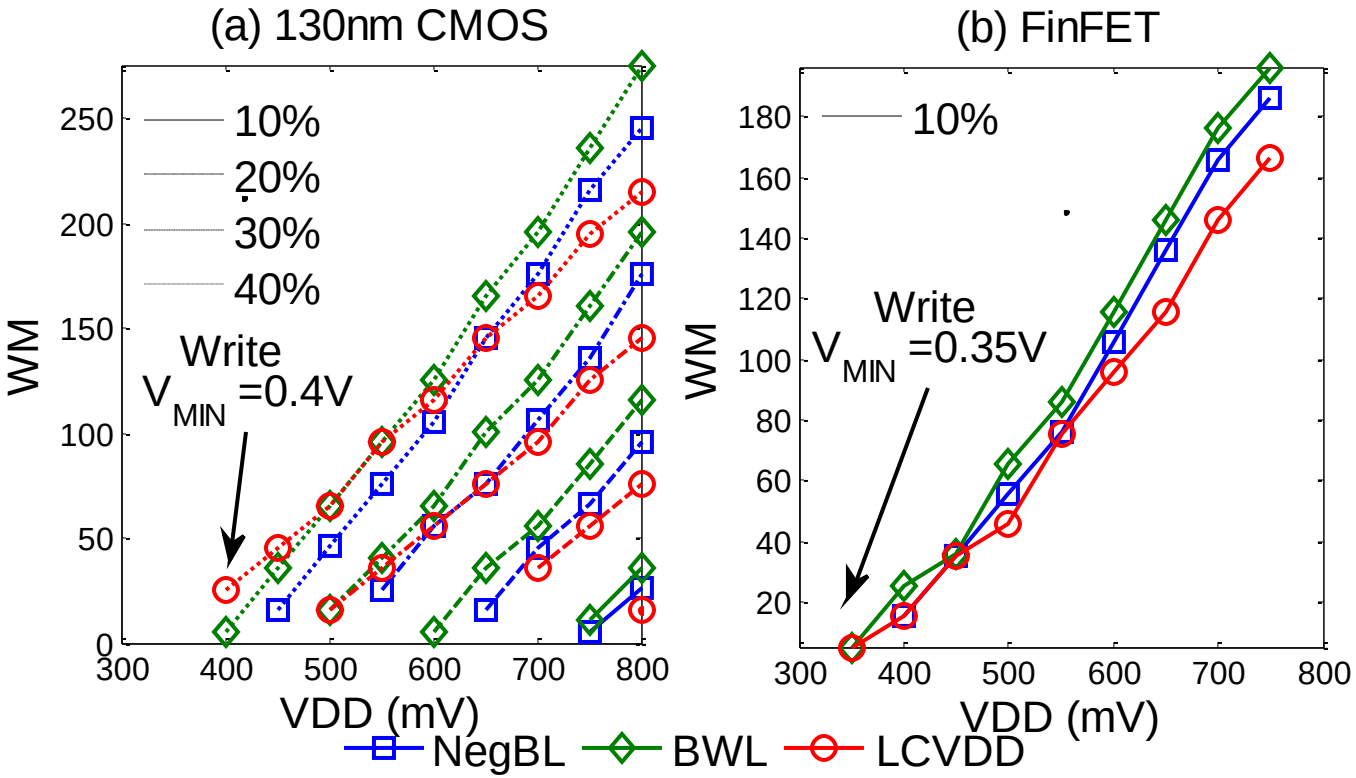

For the 130nm bit-cell, high percentages of assist are needed to lower the write $V_{MIN}$ down to 0.4V

# Write Assist - WM



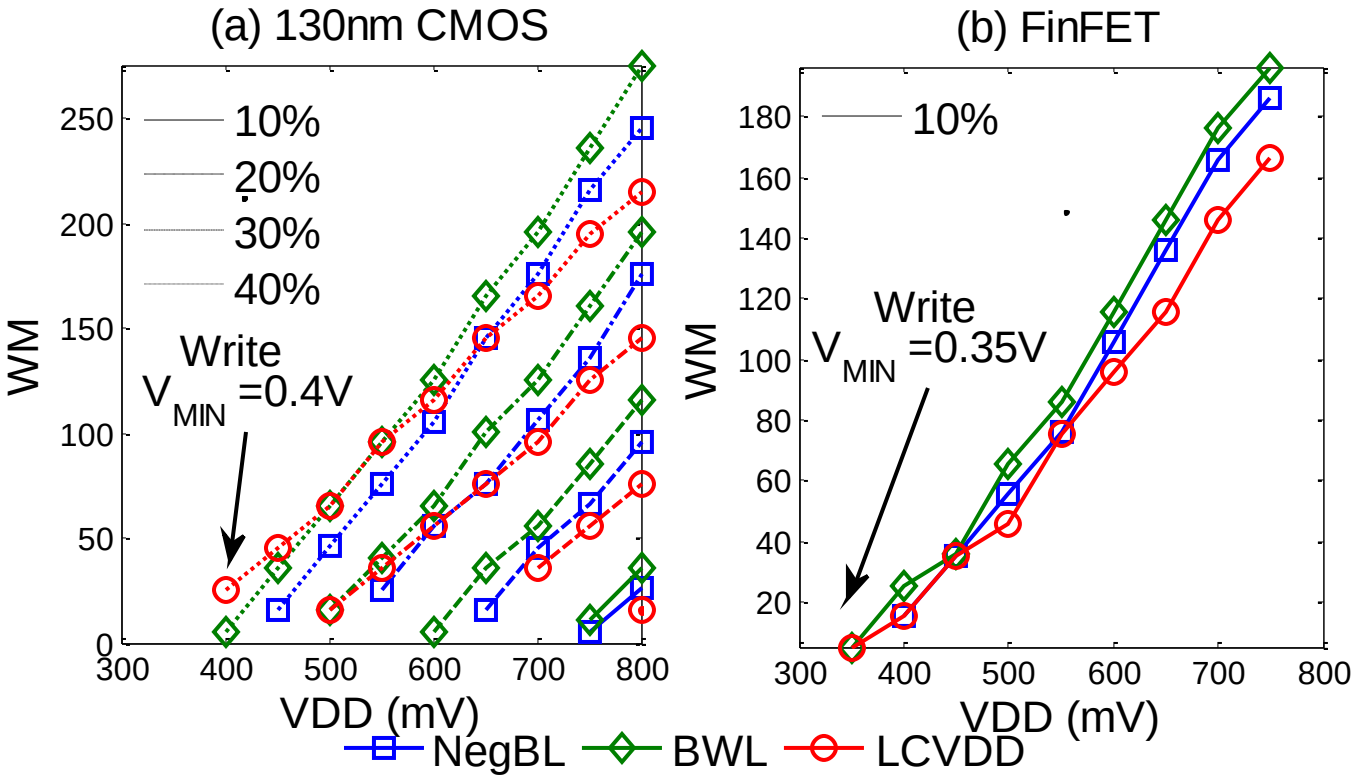

BWL provides the highest improvement in write margin at $V_{DD}$ > 550mV

# Write Assist - WM



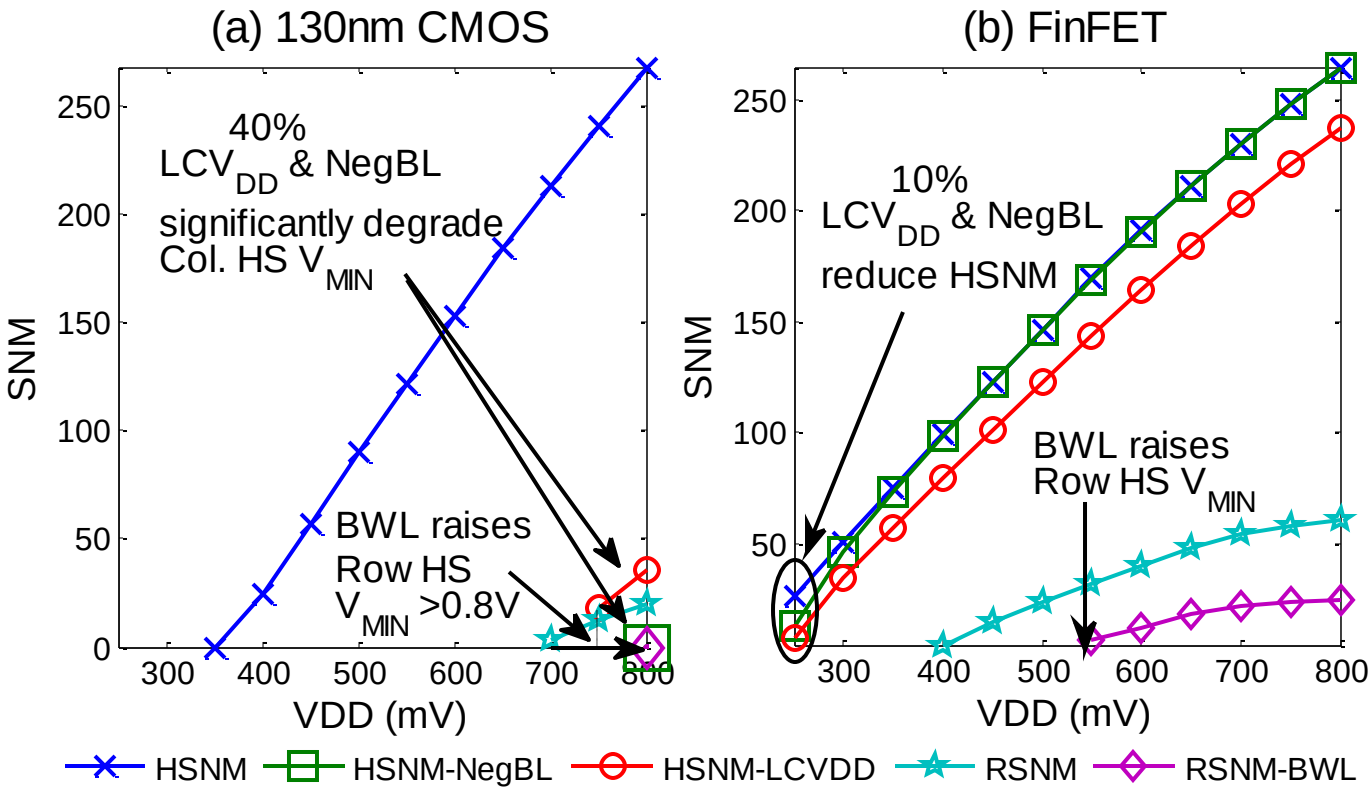

$LCV_{DD}$ provides the highest improvement in write margin at $V_{DD} < 550mV$

# Write Assist - WM



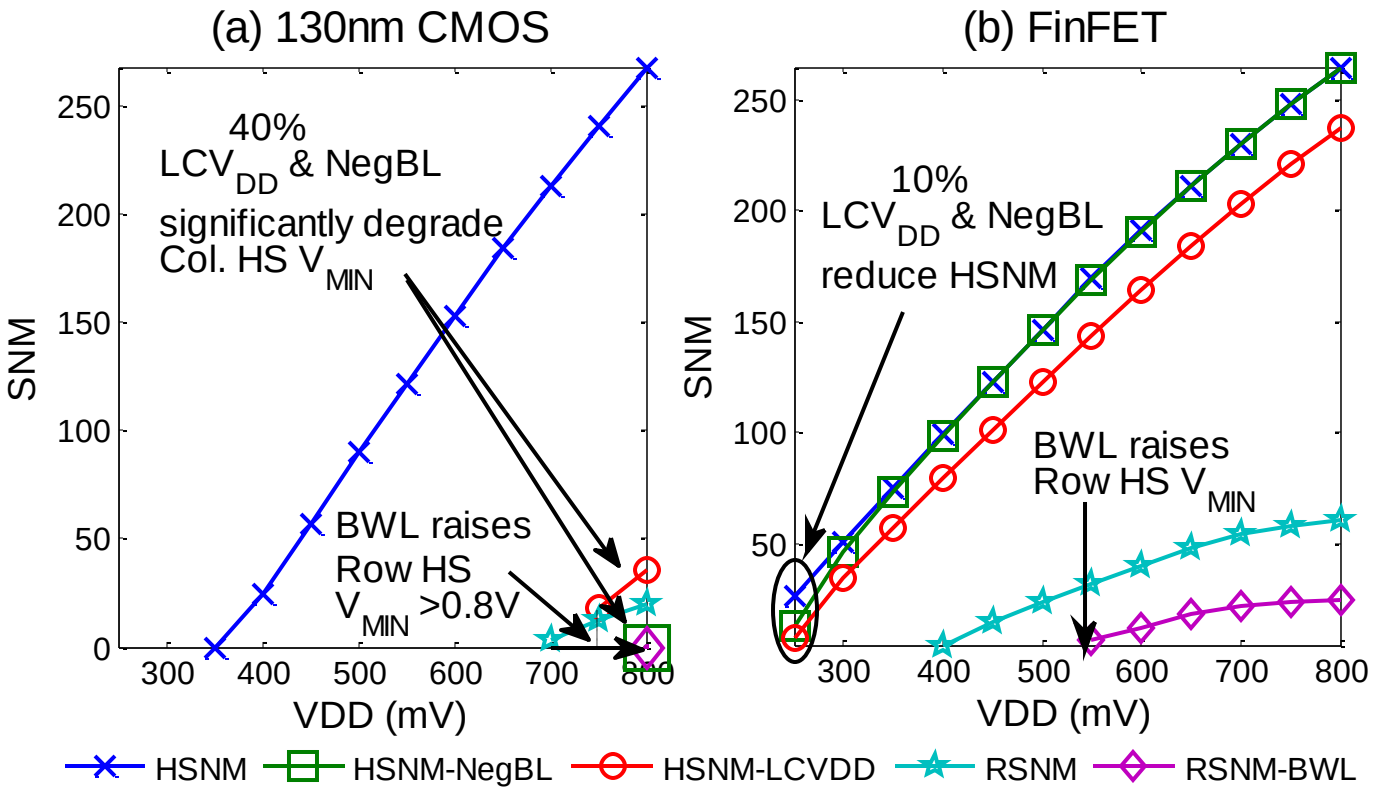

The FinFET bitcell exhibits similar behavior but only 10% of assist is needed to reduce the write $V_{MIN}$ to 0.35V

# Write Assist - SNM



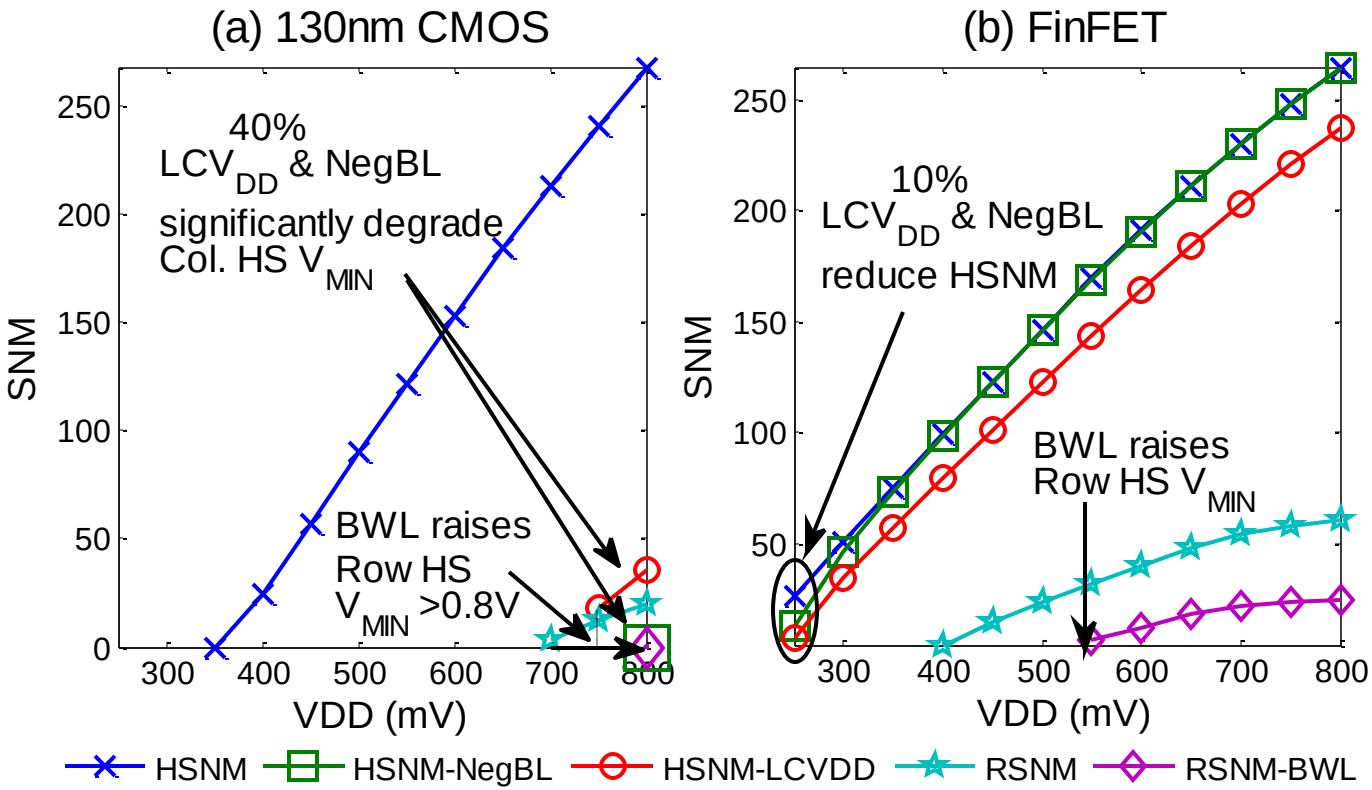

For 130nm bitcell, row HS $V_{MIN}$ is raised by BWL from 700mV to above 800mV.

# Write Assist - SNM



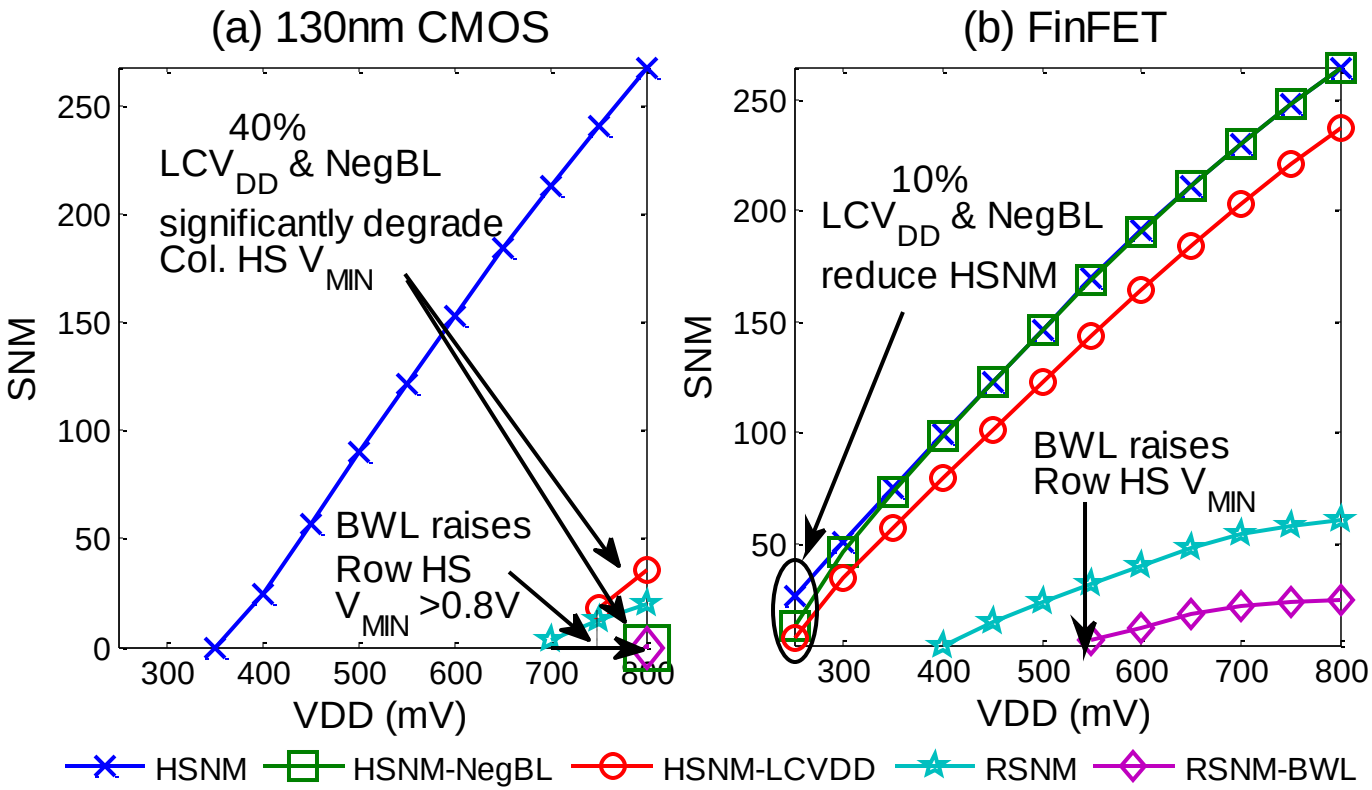

For FinFET, BWL increases the row HS $V_{MIN}$ to 0.55V

# Write Assist - SNM



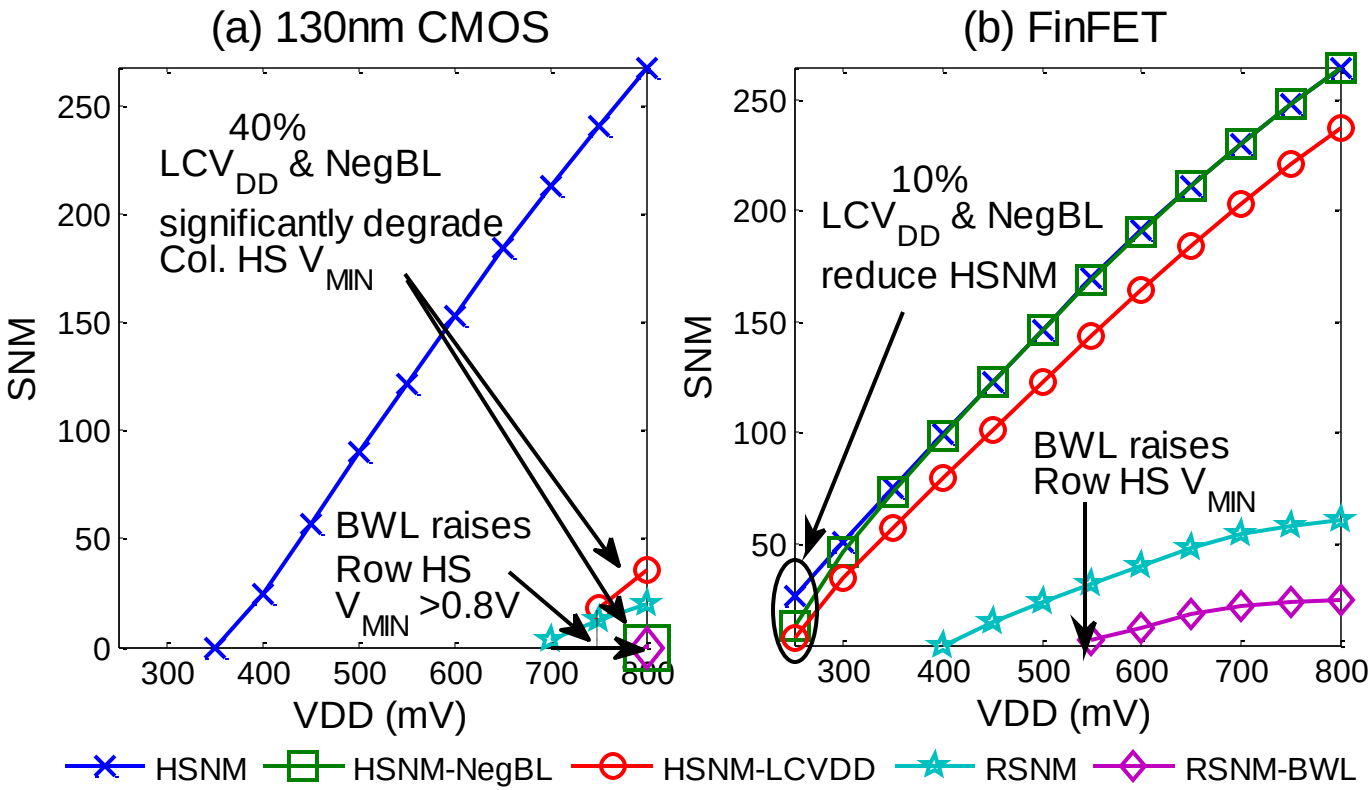

For 130nm bitcell, applying 40% $LCV_{DD}$ increases the column HS $V_{MIN}$ to 0.75V.

# Write Assist - SNM




For 130nm bitcell, applying 40% NegBL increases the column HS $V_{MIN}$ above 0.8V.

# Write Assist - SNM




For FinFET bitcell, applying 10% NegBL or $LCV_{DD}$ degrades the margins but does not raise the $V_{MIN}$

# Write Assist Summary

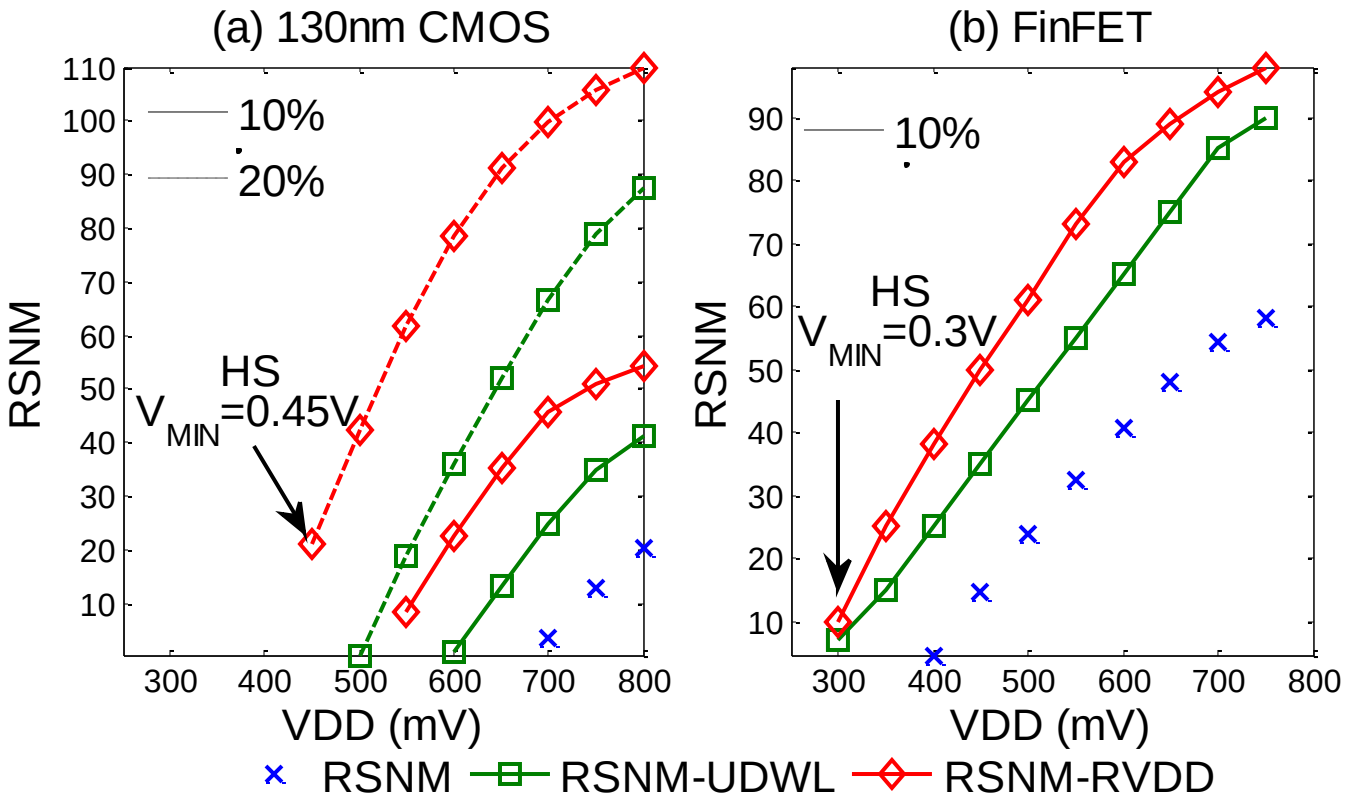
| | 130nm (40% WA) | | FinFET (10% WA) | |
|---|---|---|---|---|
| (in mV)→ | Write $V_{MIN}$ | HS $V_{MIN}$ | Write $V_{MIN}$ | HS $V_{MIN}$ |
| No Assist | >800 | 700 | 500 | 400 |
| NegBL | 450 | >800 | 400 | 400 |
| $LCV_{DD}$ | 400 | 750 | 350 | 400 |
| BWL | 400 | >800 | 350 | 550 |

- Write assist improves the write $V_{MIN}$ at the cost of HS $V_{MIN}$
- At low $V_{DD}$s, $LCV_{DD}$ provides the highest improvement in the WM.

# Read Assist Techniques

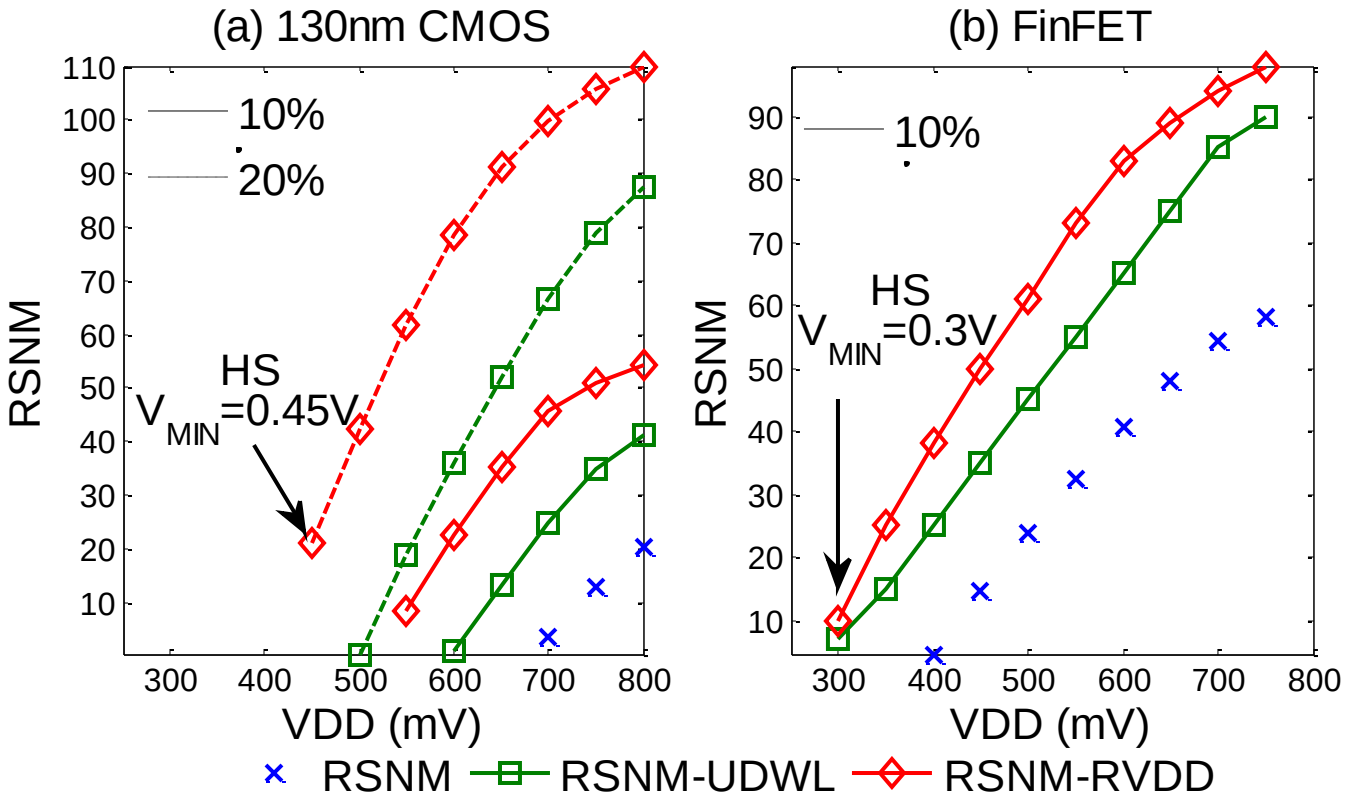
- Assist techniques: WL Underdrive (UDWL), NegBL, and Raising $V_{DD}$ ($RV_{DD}$)
- Assist was applied as a percentage of the $V_{DD.}$
- Impact on the Half Select Margins across $V_{DD}$.
- Impact on the Write Margin across $V_{DD}$.

# Read Assist - RSNM




For the 130nm bit-cell, high percentages of assist are needed to reduce the HS $V_{MIN}$ to 450mV.

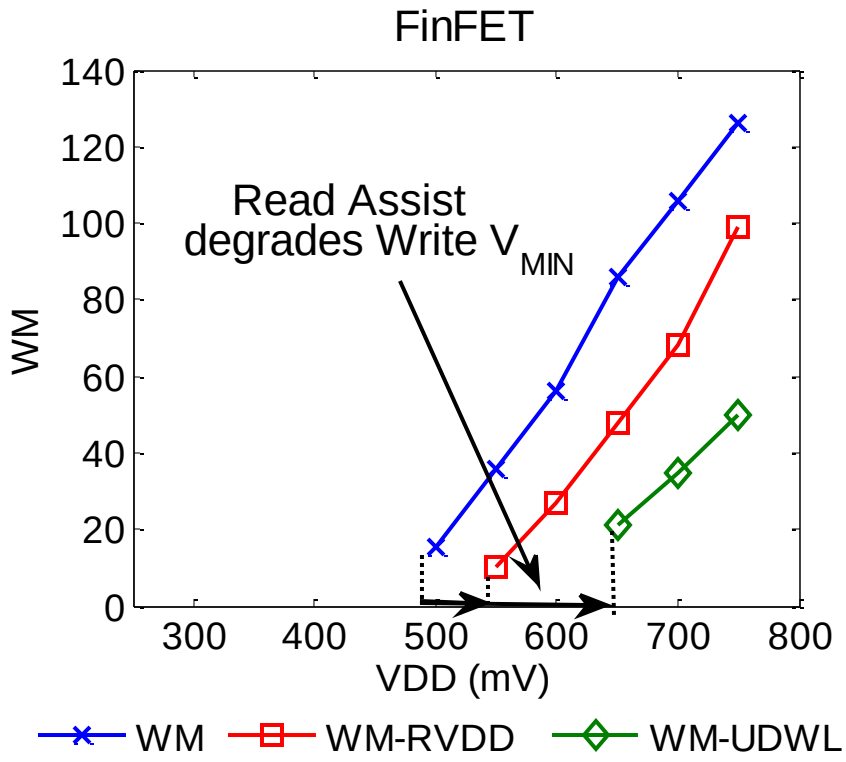
# Read Assist - RSNM




For both bit-cells, $RV_{DD}$ shows the most improvement in the row HS $V_{MIN}$.

# Read Assist - WM

- For 130nm bitcell, Write $V_{MIN}$ is already above 0.8V.
- For FinFET bitcell, both read assist tech. degrades the write $V_{MIN}$, but UDWL shows more degradation



# Read Assist Summary

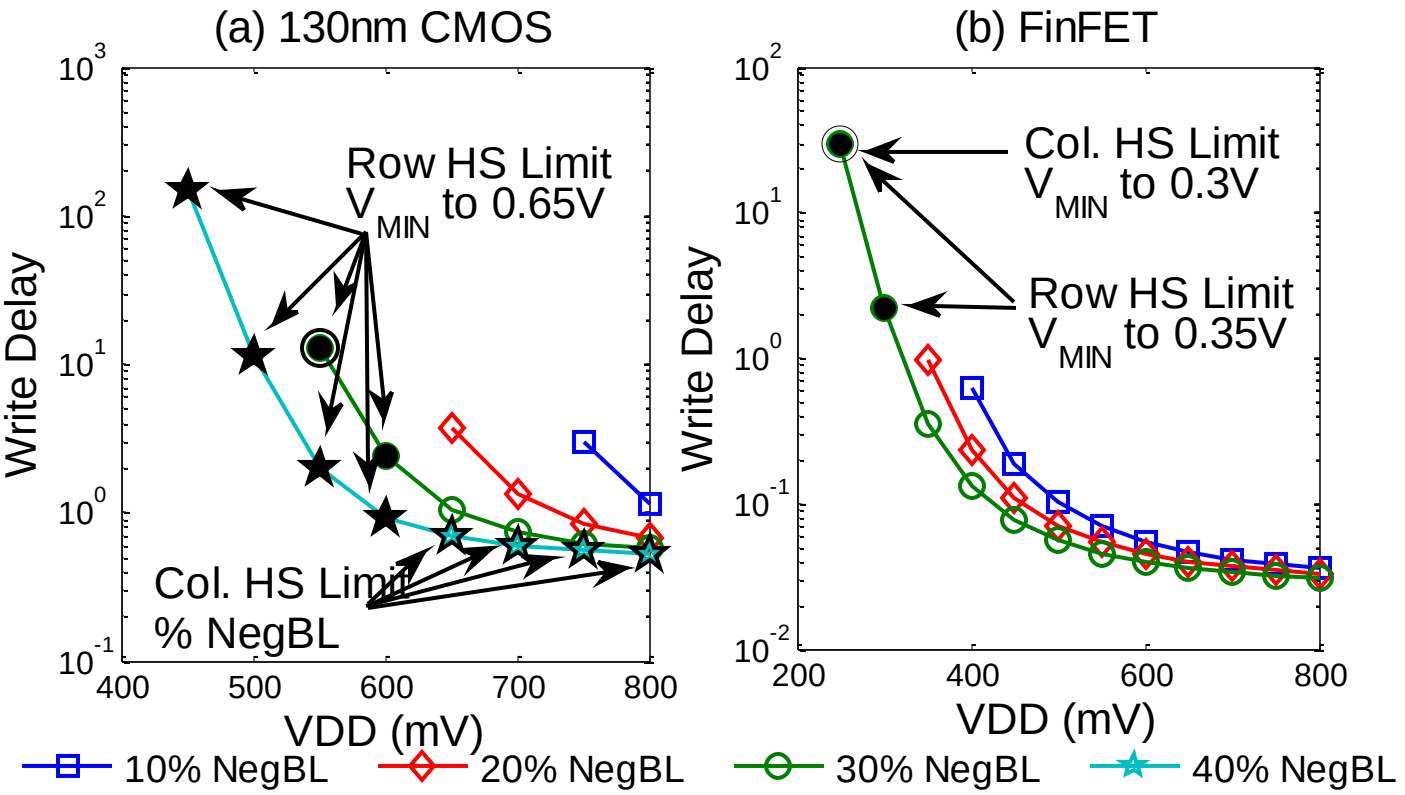
| | 130nm (20% RA) | | FinFET (10% RA) | |
|---|---|---|---|---|
| (in mV)→ | Write $V_{MIN}$ | HS $V_{MIN}$ | Write $V_{MIN}$ | HS $V_{MIN}$ |
| No Assist | >800 | 700 | 500 | 400 |
| $RV_{DD}$ | >800 | 450 | 550 | 300 |
| UDWL | >800 | 500 | 650 | 300 |

- Read assist improves the HS $V_{MIN}$ at the cost of write $V_{MIN}$
- At low $V_{DD}$s, $RV_{DD}$ provides the highest improvement in the RSNM.

# Proposed Solution

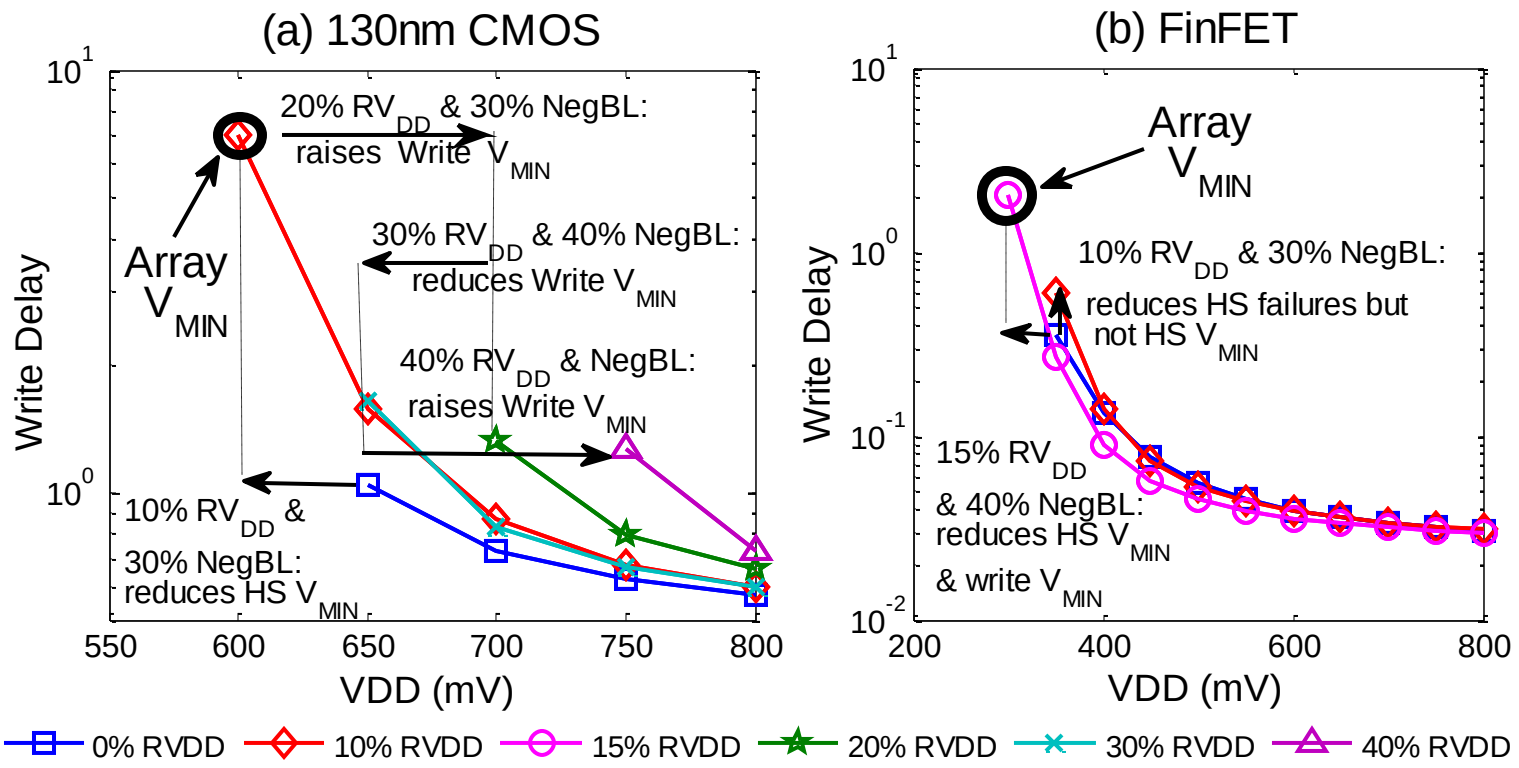
| | $RV_{DD}$-NegBL | UDWL-NegBL | UDWL-$LCV_{DD}$ |
|---|---|---|---|
| **WL** | No change | Under-driven | Under-driven |
| **BL** | Negative bias | Negative bias | No change |
| **$V_{DD}$** | Boosted for Array | No change | Lowered for column |

# Write Delay



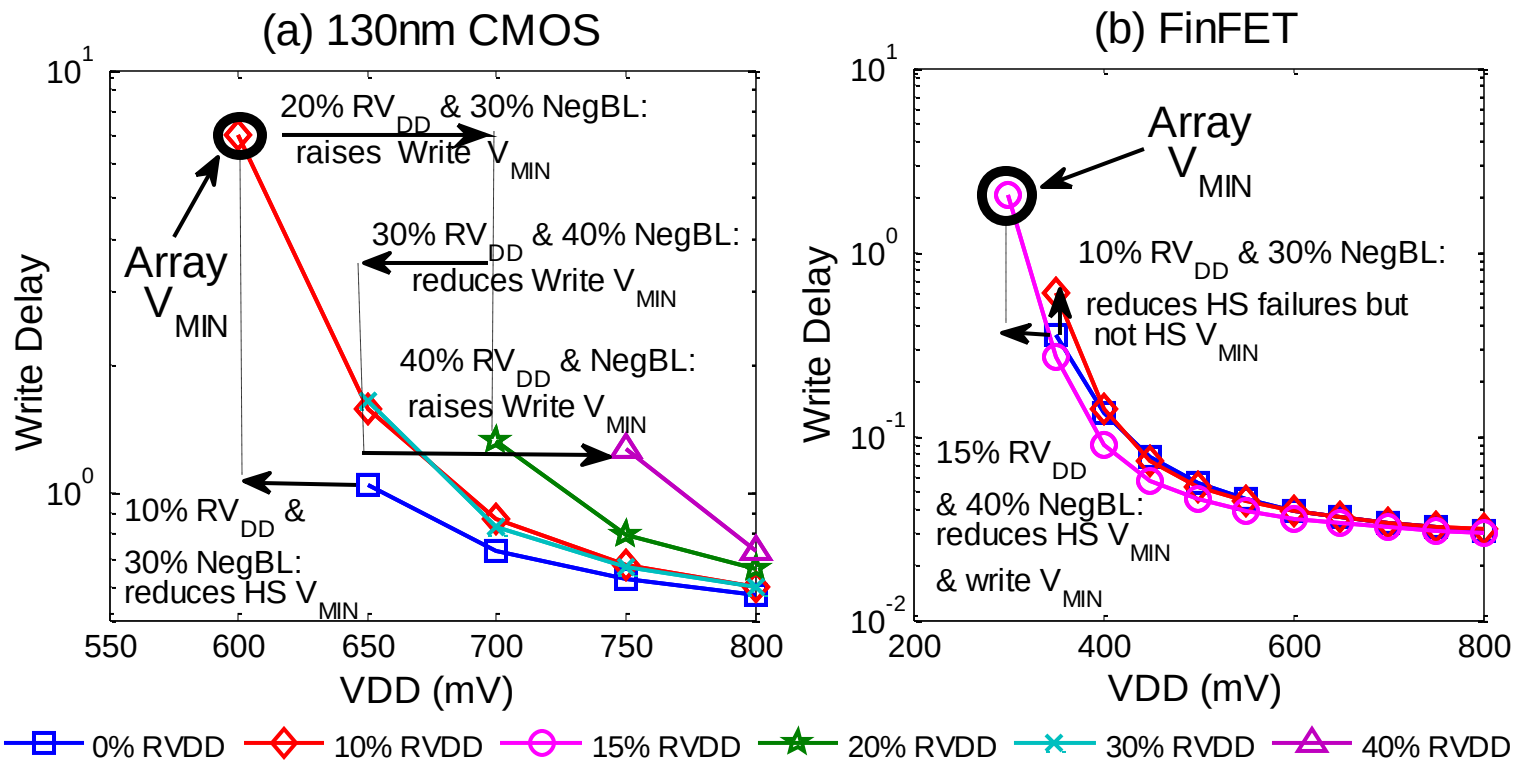

NegBL improves the write delay but when high percentages of assist are used Row & Col. HS limit $V_{MIN}$

# Proposed - $RV_{DD}$-NegBL



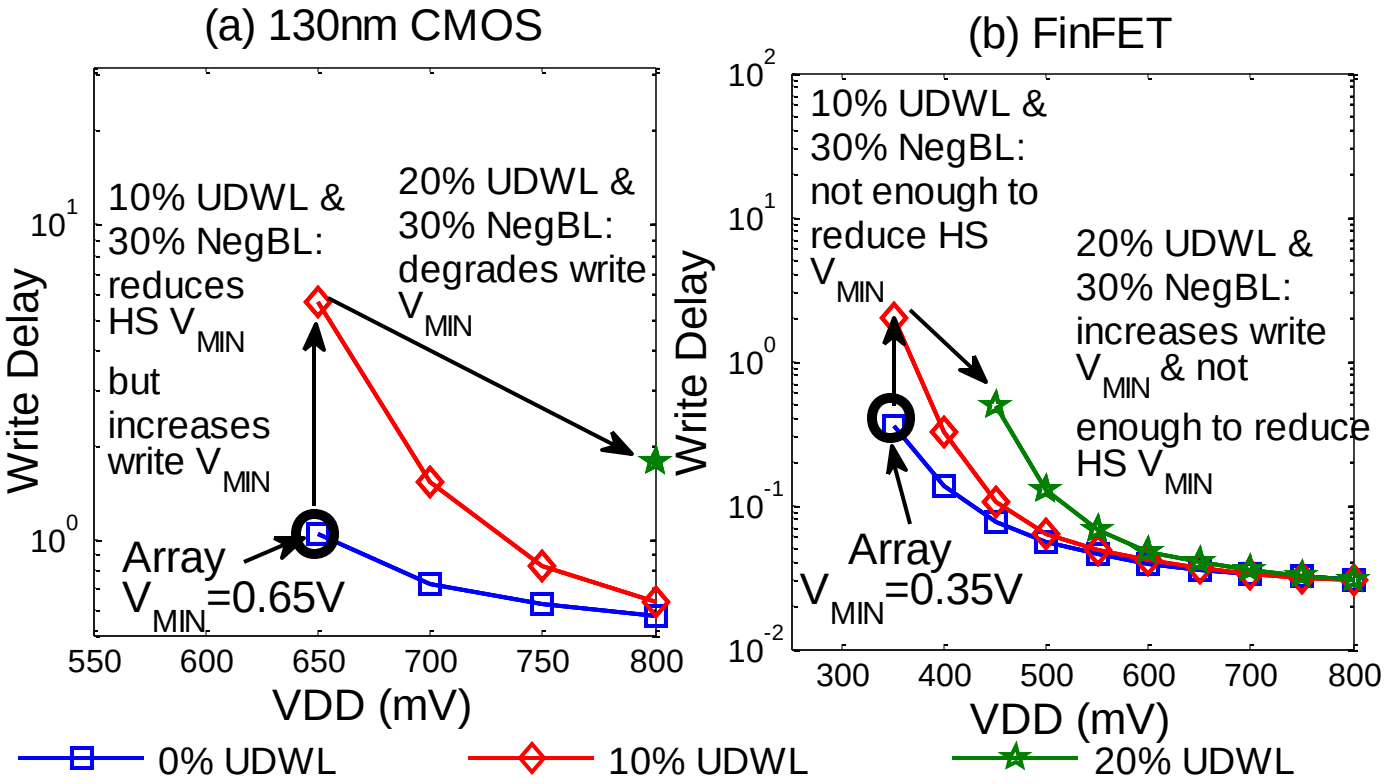

For 130nm bitcell, applying 10% $RV_{DD}$ with 30% NegBL reduces the array $V_{MIN}$ to 600mV.

# Proposed - $RV_{DD}$-NegBL




For the FinFET bitcell, applying 15% RVDD with 40% NegBL reduce the $V_{MIN}$ down to 300mV.

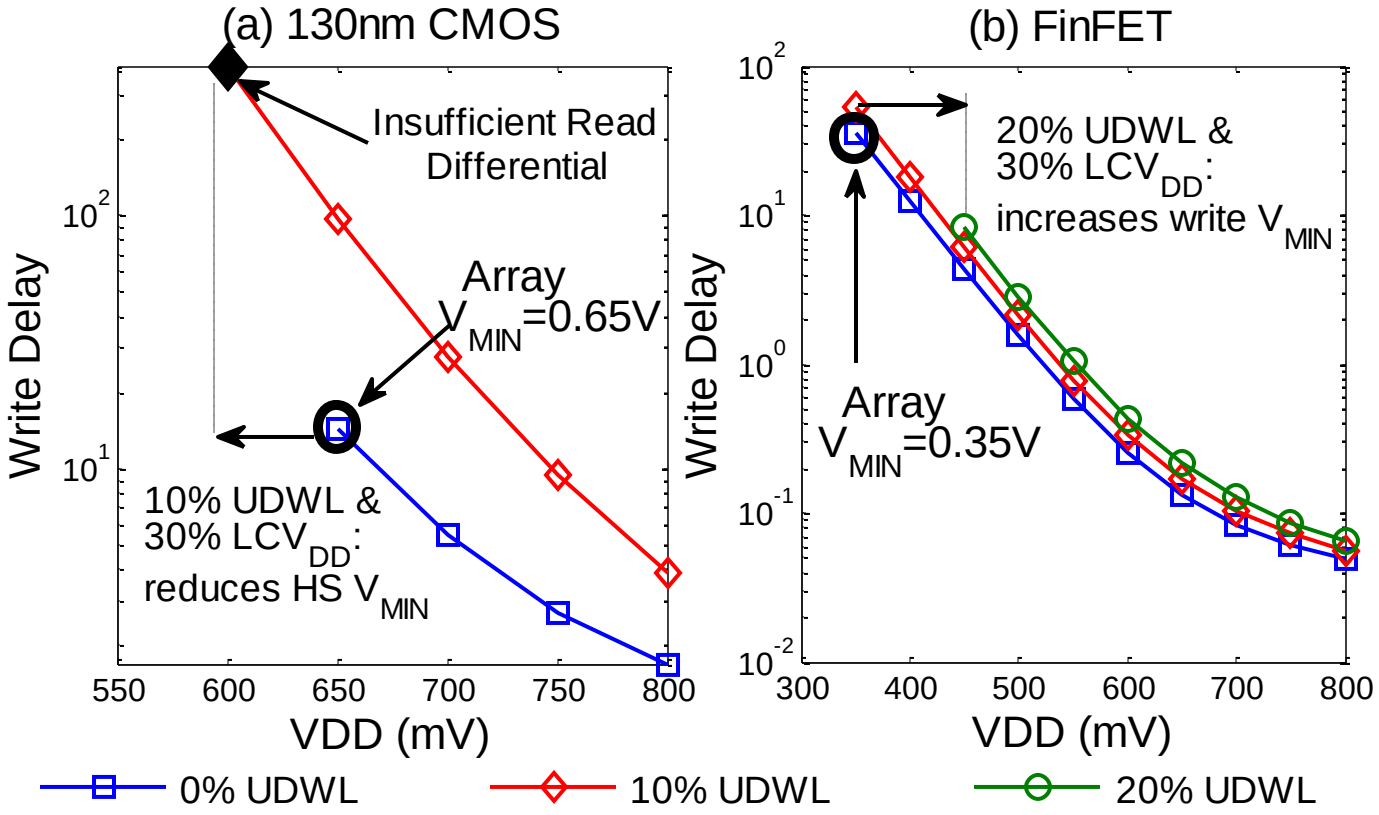
# UDWL-NegBL




Applying 10% UDWL will not reduce $V_{MIN}$.

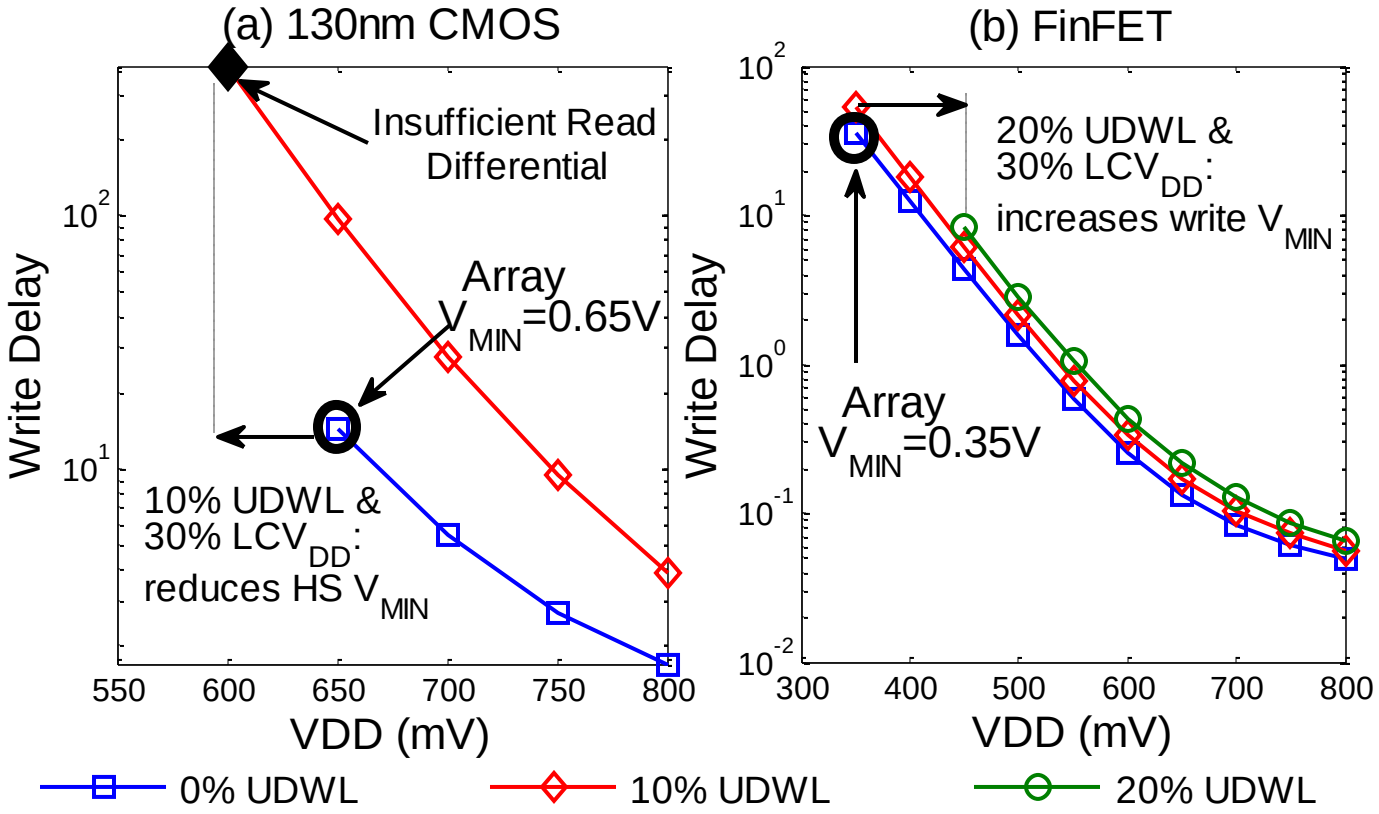
Applying 20% UDWL will increase the $V_{MIN}$.

# UDWL-LCV$_{DD}$




For 130nm bitcell, starting with 30% LCV$_{DD}$ applying 10% UDWL will reduce the write & HS V$_{MIN}$ but degrade the read V$_{MIN}$

# UDWL-LCV$_{DD}$




For FinFET bitcell, applying 10% UDWL will not reduce the write & HS $V_{MIN}$ .

Applying 20% UDWL degrades the write $V_{MIN}$ .

# Summary

| | | Array $V_{MIN}$ (mV) | % lower $V_{MIN}$ vs. NA | % lower $V_{MIN}$ vs. WA |
|---|---|---|---|---|
| **130nm CMOS** | Proposed | 600 | >25% | >20% |
| | [6][7] | 650 | >19% | >13% |
| | [6] | 650 | >19% | >13% |
| **FinFET** | Proposed | 300 | 40% | 25% |
| | [6][7] | 350 | 30% | 13% |
| | [6] | 350 | 30% | 13% |

The proposed combination allows the most reduction in array $V_{MIN}$.

# Assist per Corner

- The worst case write corner is different than the worst case HS corner.
- Thus controlling the assist percentage by corner allows more improvement in $V_{MIN}$.

130nm bitcell

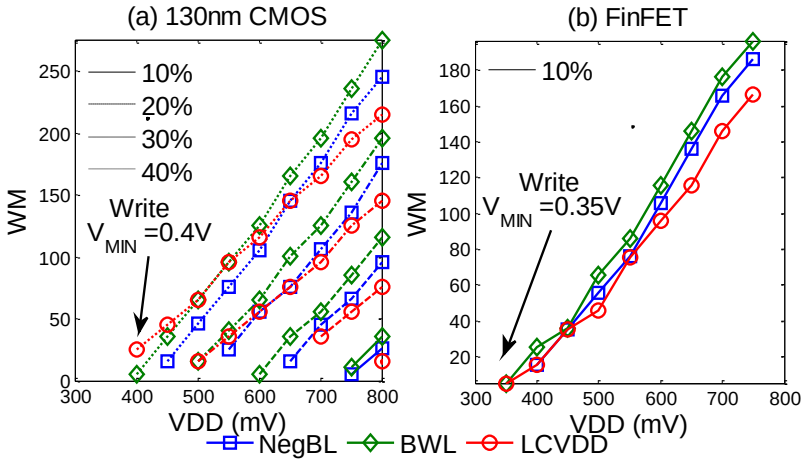
| Corner | NegBL | $RV_{DD}$ | $V_{MIN}$ (mV) |
|---|---|---|---|
| TT | 10% | 0% | 450 |
| SS | 10% | 0% | 450 |
| FF | 0% | 10% | 450 |
| SF | 40% | 0% | 450 |
| FS | 0% | 20% | 450 |

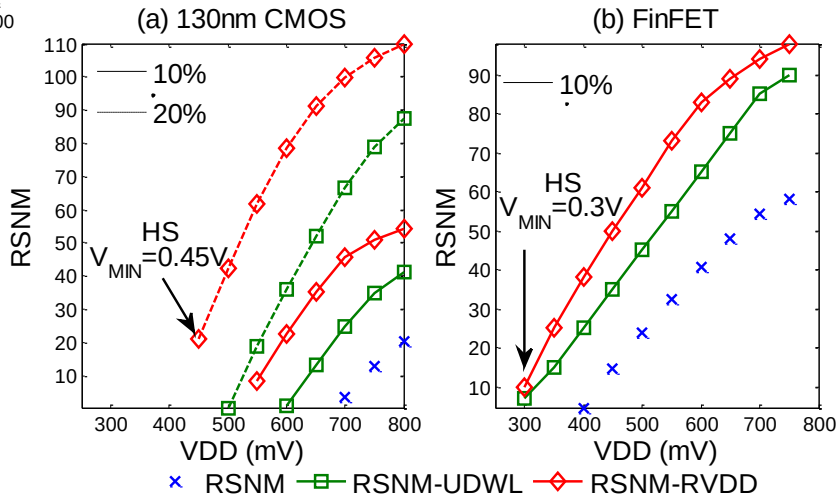
# Assist per Corner

- The worst case write corner is different than the worst case HS corner.
- Thus controlling the assist percentage by corner allows more improvement in $V_{MIN}$.

FinFET bitcell

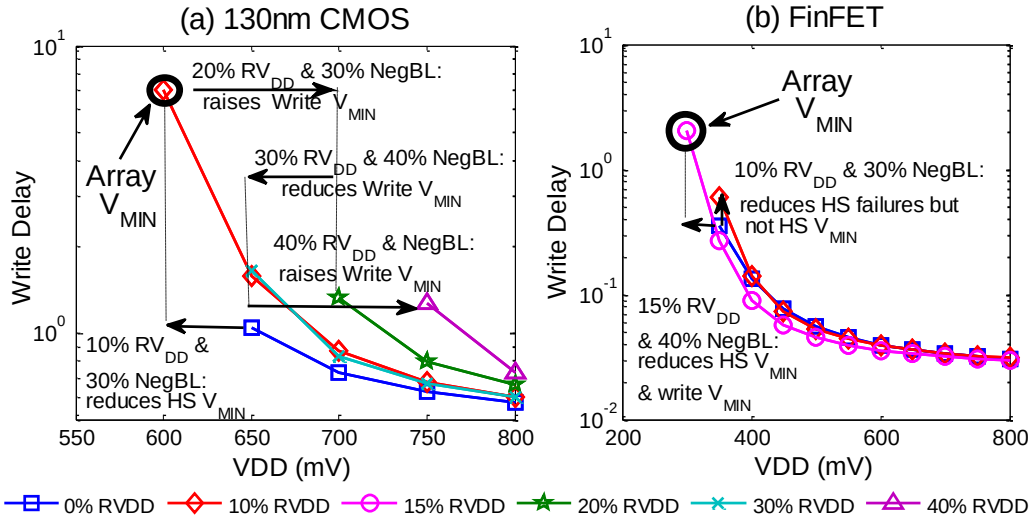
| Corner | NegBL | $RV_{DD}$ | $V_{MIN}$ (mV) |
|---|---|---|---|
| **TT** | 10% | 0% | 300 |
| **SS** | 10% | 0% | 300 |
| **FF** | 10% | 0% | 300 |
| **SF** | 30% | 0% | 300 |
| **FS** | 10% | 15% | 300 |

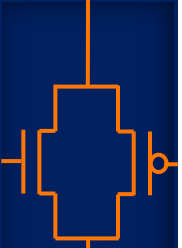



# Thank You!

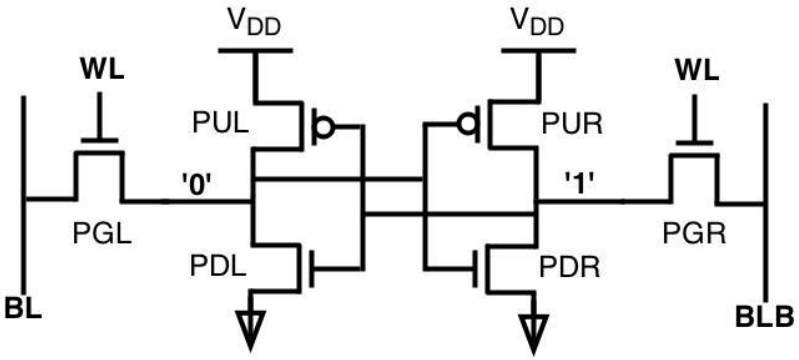
# Questions?

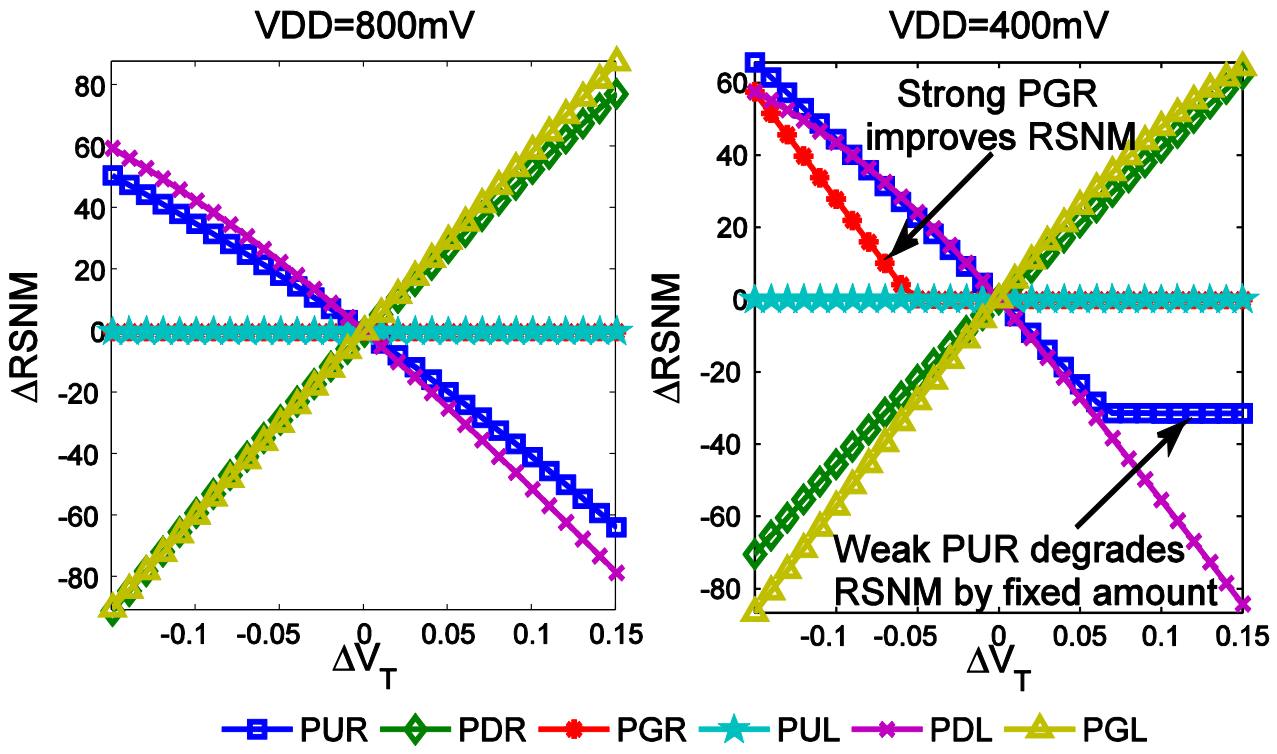




# Backup Slides

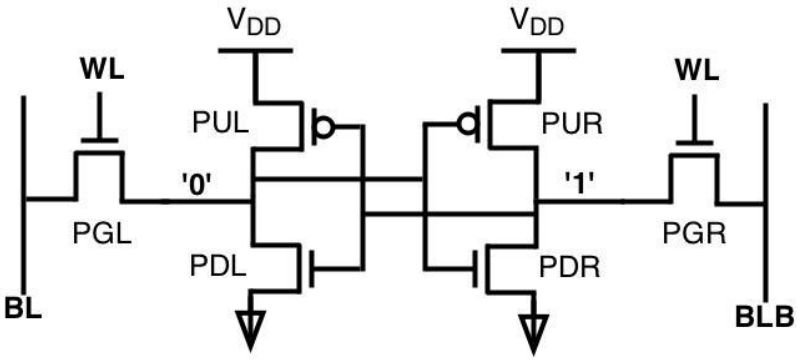
# SNM Sensitivity

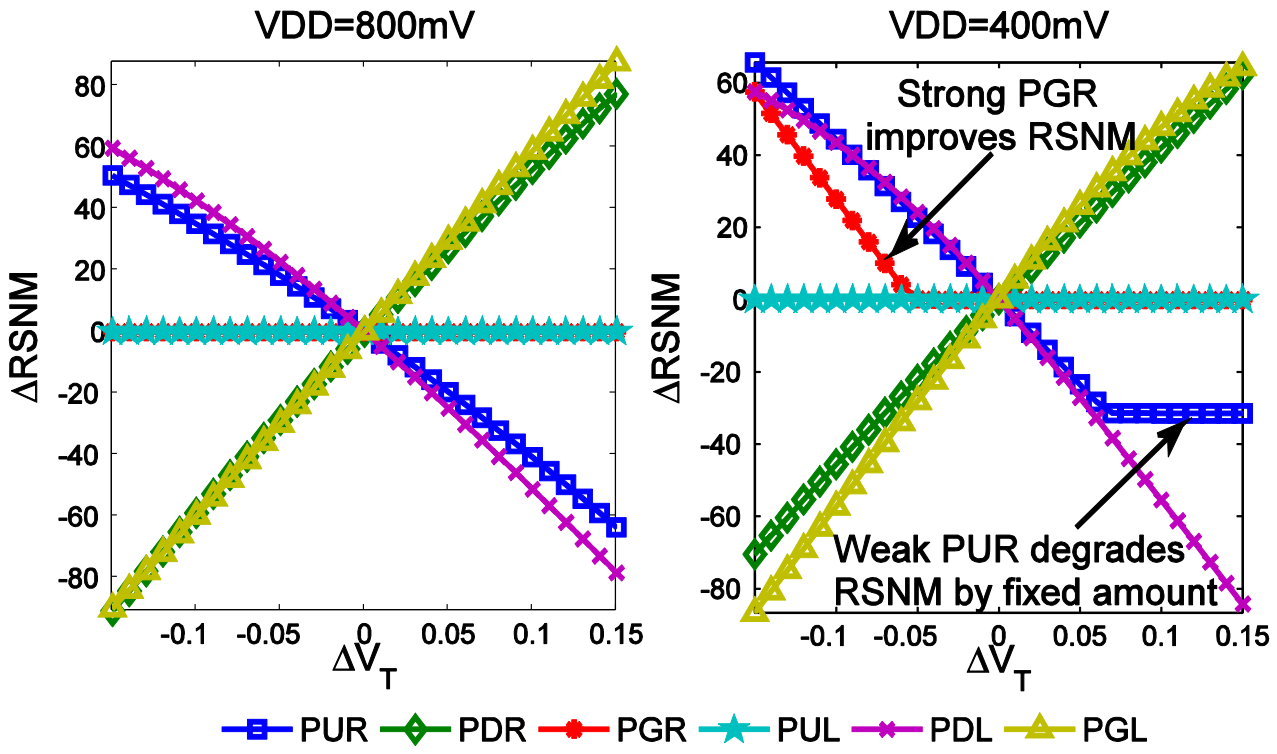



At high $V_{DD}$s, the RSNM is most sensitive to PGL and PDR

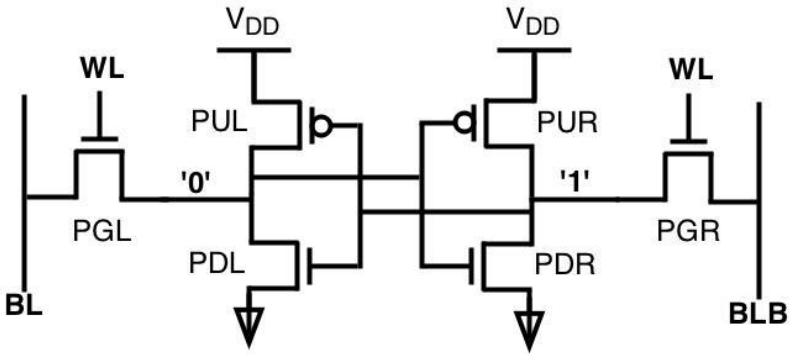
# SNM Sensitivity

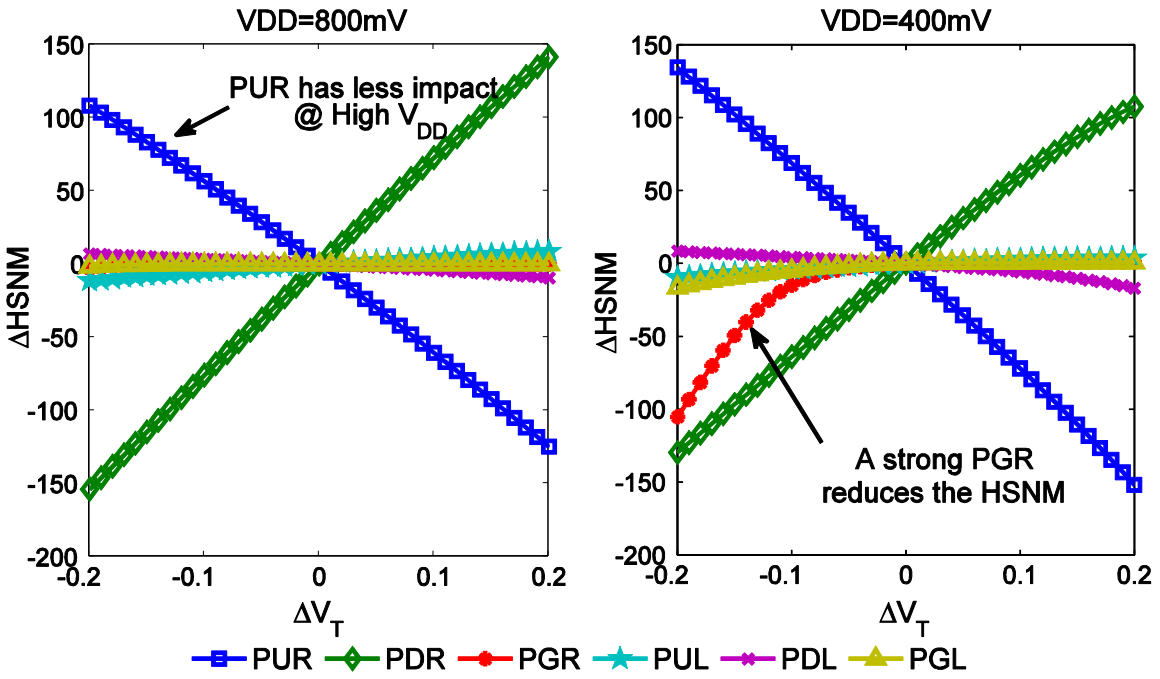



The RSNM is most sensitive to PGL and PDR at all voltages → BWL will negatively impact the RSNM.

# SNM Sensitivity




The HSNM is most sensitive to changes in PDR and PUR at high $V_{DD}$s, but at low $V_{DD}$s PGR starts to play an important role.