

# An Energy-Efficient Subthreshold Level Converter in 130-nm CMOS

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**Abstract**—This brief presents a fast energy-efficient level converter capable of converting an input signal from subthreshold voltages up to the nominal supply voltage. Measured results from a 130-nm test chip show robust conversion from 188 mV to 1.2 V with no intermediate supplies required. A combination of circuit methods makes the converter robust to the large variations in the current characteristics of subthreshold circuits. To support dynamic voltage scaling, the level converter can upconvert an input at any voltage within this range to 1.2 V.

**Index Terms**—Level converter, level-up shifter, subthreshold.

## I. INTRODUCTION

**B**IOLGICAL and environmental real-time monitoring systems that interact with both our surroundings and our own bodies are emerging. Examples include hearing aids, pacemakers, cochlear implants, electrocardiograms, thermal monitors, and environmental sensors. These devices require ultralow power to allow long operational lifetimes from small-form-factor constrained batteries. One method for reducing power is using a supply voltage below the device voltage threshold  $V_T$ , which is referred to as subthreshold  $V_{Sub-V_T}$  operation [1], [2]. Reducing the supply voltage can have up to a quadratic reduction of energy ( $CV_{DD}^2$ ). A required cost of supply reduction is slowing the clock frequency to match an increased delay caused by lower transistor current. The requirements of some real-time systems allow for lower speeds, thus making subthreshold operation an ideal solution for ultralow energy consumption. Because subthreshold devices operate at voltages well below the nominal  $V_{DD}$  for most processes, level converters are necessary to interface subthreshold circuits to core voltage levels. Fig. 1(a) and (b) are examples of conventional level-converter topologies.

Due, in part, to the proliferation of multiple voltage domains on a chip, numerous level converters exist for strong inversion operation, but subthreshold conversion differs from the conventional scenario. In the subthreshold, the substantially larger voltage differential between local supplies causes most conventional level converters to fail. Strong-inversion designs that interface with chip I/O must often cope with  $V_{DS}$  or  $V_{GS}$  that exceed the breakdown voltage of core transistors.

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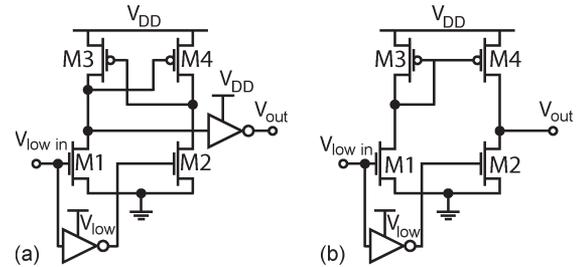


Fig. 1. Circuit-level schematic of the two conventional level converters (a) Type I and (b) Type II.

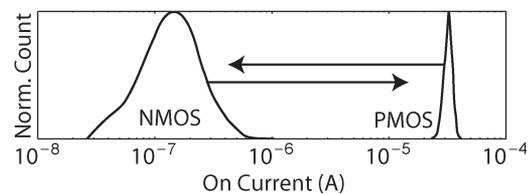


Fig. 2. Proximity of  $I_{on,N} - I_{on,P}$  current where the NMOS is in subthreshold and the PMOS is in superthreshold. The left curve is an NMOS (M1) device turned on with  $V_{GS,N} = 220$  mV, and the right curve is an “on” ( $V_{SG,P} = V_{DD}$ ) PMOS (M3) device. These distributions need to swap positions in order to convert a subthreshold input using a conventional topology.

Subthreshold designs typically operate well within device reliability requirements. A “high” output of a subthreshold block is too low for blocks operating with a nominal  $V_{DD}$  to typically recognize. Fig. 2 shows a Monte Carlo simulation for a 130-nm bulk CMOS process of both NMOS and PMOS currents for transistors that are “on.” The NMOS is “on” in subthreshold ( $V_{GS,N} = 220$  mV), and the PMOS is in strong inversion ( $V_{SG,P} = 1.2$  V). A conventional level-converter topology would require that the NMOS current exceed the PMOS current, but the NMOS’s “on” current needs to increase by several orders of magnitude to overcome this imbalance. In addition, the exponential relationship between the current and  $V_T$  in subthreshold leads to a larger variation in current at low voltage. These phenomena require more careful design for subthreshold operations than for traditional strong-inversion level converters. The subthreshold level converter would ideally be compatible with dynamic voltage scaling (DVS) circuits. This correlates to convertible input “high” voltages anywhere in the range from  $V_{Sub-V_T}$  to  $V_{high}$ .

Many level-converter topologies exist for circuit designers to implement. The types of level converters discussed in this brief convert between signals from a  $V_{low}$  supply domain to a higher nominal  $V_{DD}$ . Fig. 1 shows two of the most traditional topologies [3]. The cross-coupled PMOS devices of Fig. 1(a),

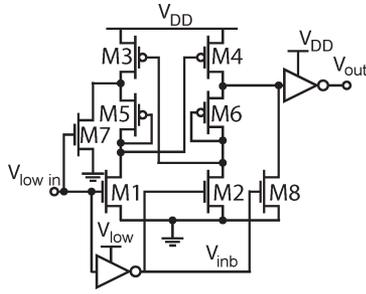


Fig. 3. Schematic of a modified Type-I level converter [8] using a PMOS diode to assist subthreshold conversions.

which are of Type I, take advantage of a positive feedback network to create a full output swing. The inverter provides a differential input for the conversion stage. Fig. 1(b), which is of Type II, uses a current mirror to level shift before the final inverter. This topology's main drawback is the static current with a "high" input. Each of these designs is typically used for converting between two superthreshold domains. Zhai *et al.* used a topology similar to Fig. 1(a) to convert from 200 mV to 1.2 V [4]. They used a cascaded design with three intermediate conversion stages, each of which requires its own supply voltage value, i.e., 300, 400, and 600 mV. In addition, they change the size of each stage that operates in subthreshold to increase their robustness. The major drawback to this design is the three intermediate supply voltages, which increase the power management overhead.

Another technique is to modify either a Type-I or -II level converter by using a reduced swing inverter (RSI) to reduce leakage and weaken the pull-up circuit [5], [6]. Chang *et al.* used the RSI to essentially lower the  $V_{SG}$  of each PMOS, on a Type-I converter, by raising  $V_G$  to operate between  $V_{high}$  and  $V_{high} - 2 * V_{TP}$ . This weakens each PMOS to operate around the subthreshold region and helps facilitate a low-to-high transition. In addition, they add a voltage doubler before the input of the level converter to boost the low voltage and increase  $V_{GSN}$ . This design complicates the topology by at least 18 transistors (not including the voltage doubler), augmenting its susceptibility to variation. The topology in [5] does not also easily support scalable voltage inputs. It cannot track the delay of a DVS circuit, because the cross-coupled PMOS devices are constantly weakened by the RSI, regardless of the input voltage level.

Another approach requires a process technology that supports dynamic threshold CMOS. Chavan *et al.* [7] used a silicon-on-insulator (SOI) technology to gain access to the bodies of each type of transistor. They proposed tying the body for M1 and M2 for both topologies in Fig. 1 to the gate. This method requires the manufacturing technology to allow each device's body to independently be set. This configuration shifts the  $V_T$  for each device, depending on the input, reducing it when the device is "on" and increasing it when the device is "off." In addition to requiring a technology-specific solution, this scheme cannot support a wide-range DVS input, because it would forward bias the diodes connected to the base once the input becomes larger than  $V_{T_{DIODE}}$ .

The topology in Fig. 3 uses diode-connected PMOS transistors between the drains of M1 and M2 in Fig. 1(a) and the

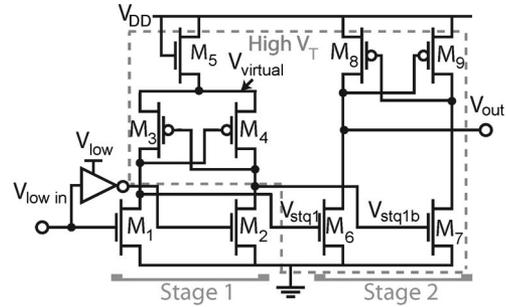


Fig. 4. Circuit-level schematic of the proposed level converter.

drains of M3 and M4 [8]. Each diode acts a current limiter to the PMOS pull-up devices. However, this design limits the output swing between  $V_{DD}$  and  $V_{TP}$ , without adding M7 and M8. The authors fix this by adding M7 and M8 at the drain of M3 and M4. M7 and M8 are controlled by  $V_{in}$  and  $V_{inb}$  to pull the output to ground. When the input is 0, M4 could have a  $V_{GS}$  other than 0 due to a voltage drop across M5. This could leave M4 in weak inversion, allowing a static current to pass through M8 and M4. The same is true when the input is high, but M5 and M7 are now creating a static current. Variation in the diode-connected devices has a strong impact on the reliability of the solution.

In this brief, we propose a new subthreshold level converter based on a two-stage Type-I design. Our design uses a combination of circuit methods to ensure reliable, fast, and energy-efficient operation. Specifically, we use sizing, threshold voltage selection, and diode-based voltage degradation to enable reliable conversion across variation and temperature. The succeeding sections cover the implementation and justification of our design, as well as hardware measurement results from a 130-nm bulk CMOS chip.

## II. IMPLEMENTATION

This section describes the functionality and specifics of the proposed level converter. This brief combines several techniques to reduce the number of power supplies and extend the conversion range relative to existing subthreshold level converters. Fig. 4 shows a schematic of the proposed topology. There are two main stages to this topology. The first stage uses a cross-coupled differential inverter stage with diode-connected NMOS. The second stage is a normal cross-coupled differential inverter whose only purpose is to restore the final output to full swing from its 0 to  $V_{DD} - V_T$  range at the output of stage one. For subthreshold inputs, the majority of the upconversion takes place in the first stage. Referring back to Fig. 2, stage one can only work if the NMOS input devices can overpower the PMOS pull-up devices. The succeeding sections describe the three primary methods used to ensure reliable operation in stage one.

### A. Multithreshold Devices

The exponential impact of  $V_T$  on subthreshold current makes  $V_T$  a powerful knob for modulating the current. The NMOS devices  $M_1$  and  $M_2$  in Fig. 4 must overpower  $M_3$  and  $M_4$  for

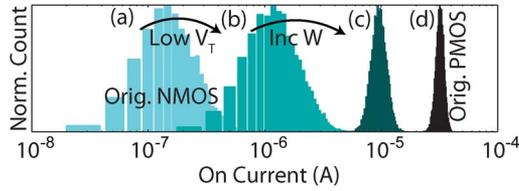


Fig. 5. Ten-thousand-iteration Monte Carlo simulation displaying the increase in NMOS “on” current at 220 mV as the NMOS is changed, compared with a nominal “on” PMOS. (a) Minimum-sized and nominal  $V_T$  device is used. (b) The device was changed to a low- $V_T$  device. (c) The width was increased. (d) PMOS with nominal voltage and minimum size.

correct conversion. Fig. 4 shows how we assign devices with different threshold voltages to start switching the balance of transistor strengths. Most modern processes provide both high  $V_T$  and low  $V_T$  devices. Each device introduces different advantages. The high  $V_T$  devices were chosen for  $M_3$ – $M_9$ . The higher  $V_T$  will reduce the energy used when transitioning. They also reduce the leakage current of off devices.  $M_3$  and  $M_4$  use the higher threshold devices, weakening them for transitions. This achieves a similar result as increasing the length of the devices by 35%–70% without sacrificing area.  $M_1$  and  $M_2$  use the lower threshold devices to increase their ability to pull the PMOS devices down. Fig. 5 shows the increase in current from (a) to (b) by switching to the lower threshold device, thus decreasing the disparity between the nominally “on” PMOS and the weak-inverted NMOS.

### B. Subthreshold Device Sizing

Ostensibly, sizing is a relatively weak knob in subthreshold since it only has a linear impact on current. However, changes to the length can modulate the  $V_T$  due to short-channel effects, heightening the impact of size on current. The second adjustment to the Type-I converter that we applied adjusts the PMOS and NMOS  $W/L$  ratios for subthreshold offsets.  $M_3$  and  $M_4$  have a  $W/L$  ratio that is substantially less than that of  $M_1$  and  $M_2$  to increase the NMOS’s ability to pull the output node low. The stronger NMOS device causes an increased gate capacitance with the increased width. Fig. 7 shows a simulation used to find the optimal width used to minimize the delay associated with charging the input gates by a standard inverter. Fig. 5(c) shows how much closer the current approaches the nominal PMOS’s current by increasing the width in addition to using different  $V_T$ s. Increasing the length of the PMOS devices increases the NMOS’s ability to transition from low to high. Fig. 6(b) shows the effect of increasing the length of the PMOS to help the current imbalance. Fig. 6(b) and (d) shows that changing the widths and lengths in addition with  $V_T$  nearly overcomes the current imbalance.

### C. Virtual Supply

The final circuit method to ensure reliable operation uses a diode-connected device to degrade the  $V_{DD}$  of the pull-up devices in stage one. Fig. 4 shows  $M_5$  of stage one as a diode-connected NMOS device. This creates a  $V_{TN}$  voltage drop for the supply of the cross-coupled latch. The supply is not static during transitions, and that drop is dependent on the current

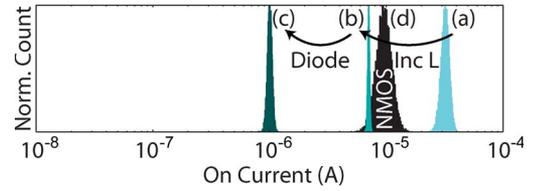


Fig. 6. Ten-thousand-iteration Monte Carlo simulation displaying the decrease in PMOS “on” current under nominal voltage as the PMOS is changed compared to an optimized subthreshold “on” NMOS. (a) Minimum-sized and nominal  $V_T$  device is used. (b) The device length was increased. (c) The diode-connected NMOS was added. (d) Optimized NMOS from Fig. 5.

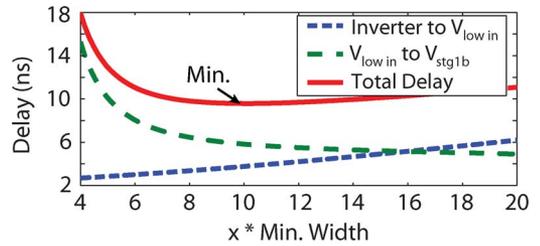


Fig. 7. Simulation of delay through two input buffers connected to the input of stage one and the delay of stage one from  $V_{low\ in}$  to  $V_{stg1b}$  while sweeping the widths of  $M_1$  and  $M_2$ , where  $V_{low} = 220$  mV.

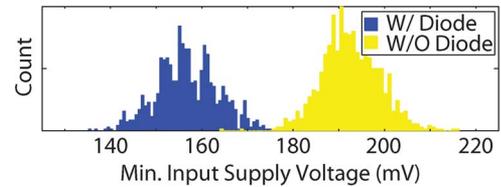


Fig. 8. Monte Carlo simulation, of 1000 iterations, showing the lowest input signal supply voltage that is convertible comparing two Type-I level converters. Both are in stage one of our proposed topology with or without  $M_5$ .

drawn at transition. The diode drop across  $M_5$  has an equivalent to further increasing  $V_{Tp}$ . The output range of this stage is forced to  $[0V, (V_{DD} - V_{TN_{high}})]$ . Fig. 6(c) demonstrates how the diode helps decrease the “on” PMOS below the optimized NMOS of Fig. 6(d). The large difference between Fig. 6(c) and (d) shows the circuit’s robustness to variation. The bulks of all the PMOS devices are tied to  $V_{DD}$ . This is helpful for weakening  $M_3$  and  $M_4$ , because it increases the threshold voltage of each device, due to the smaller  $V_{BS}$ . The virtual supply also reduces the  $V_{GS}$  for both  $M_3$  and  $M_4$ , further reducing their current. Increased  $V_T$  due to bulk effect is the reason that an NMOS diode was chosen. Fig. 8 shows how the convertible input decreases on average by 18.4% or 36 mV when using a virtual supply. Fig. 9 shows that the average power consumed by the diode-connected topology is less than a comparable Type-I level converter. Depending on the input supply voltage, the average power saved using the diode is between 25% and 85%. A combination of all these adjustments is used to optimize the speed and minimum input levels.

Stage two makes the final level conversion from  $(V_{DD} - V_T)$  to  $V_{DD}$ . We chose to continue using the Type-I level converter; however, most traditional level converters could be used in this stage since the conversion is only from  $(V_{DD} - V_T)$  to  $V_{DD}$ . The Type-I converter used was optimized for speed rather than a low voltage input.

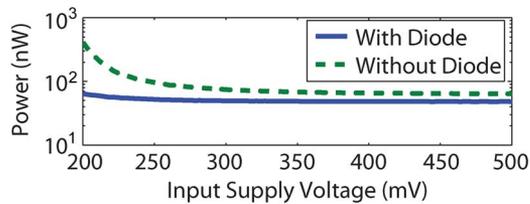


Fig. 9. Average power used by stage one of our topology during one cycle of a 1- $\mu$ s period, comparing our proposed topology with and without a diode, i.e.,  $M_5$ , virtual supply.

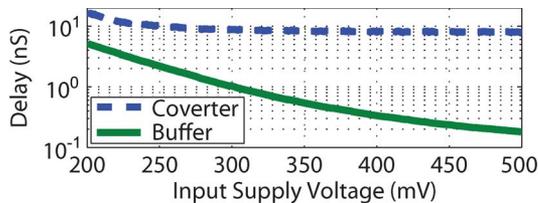


Fig. 10. Simulation of the delay through the level converter performing a conversion from a signal at  $V_{low\_in}$  up to  $V_{out}$  at 1.2 V versus a minimum-sized inverter driving three parallel inverters for reference. Both outputs drive a twice minimum-sized inverter.

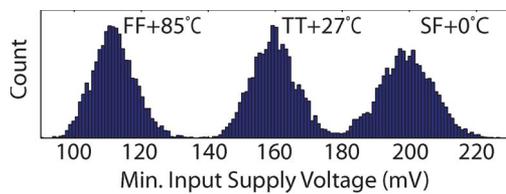


Fig. 11. Monte Carlo simulation, of 4000 iterations, taking into account how local and global variation changes minimum input signal supply voltage for upconverting to 1.2 V.

#### D. Level-Converter Delay

Fig. 10 shows a simulation of the level-converter delay for a conversion from  $V_{low\_in}$  to  $V_{out}$  along with the delay of a single minimum-sized standard cell inverter driving three parallel similar inverters. The level converter adds less than 25 ns of delay for an operating region of 200–500 mV. This limits off-chip communication frequencies; however, these delays are suitable for many subthreshold applications [4], [9]–[11]. The conversion delay is also better by 13.5 times than the fastest converter in [7], which uses a 0.25- $\mu$ m partially depleted SOI CMOS process to upconvert from 350 mV to 1.2 V.

#### E. Impact of Variation

Variation between devices can further complicate subthreshold conversion due to a heightened sensitivity to variation. Fig. 11 shows a Monte Carlo simulation that shows the minimum input supply voltage allowable for successful upconversion to 1.2 V. The level converter can convert any signal from a DVS voltage region between this minimum level and the full supply voltage. The simulation shows the results from three process corners and temperatures: 1) fast NMOS–fast PMOS (FF) at 85  $^{\circ}$ C; 2) typical–typical (TT) at 27  $^{\circ}$ C; and 3) slow–fast (SF) at 0  $^{\circ}$ C. Accounting for process, temperature, and voltage, our design supports conversion from a worst case of 227 mV up to 1.2 V. The extreme 3.645 $\sigma$ , i.e., SF at 0  $^{\circ}$ C, will permit

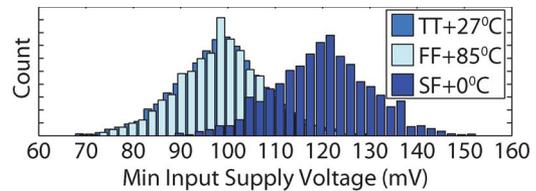


Fig. 12. Monte Carlo simulation of minimum input signal  $V_{low\_in}$  supply voltage when  $V_{Sub}-V_T$  is fixed at 220 mV. The plot shows 4000 iterations of all three global variations, i.e., SF, FF, and TT, at the respective temperatures: 0, 85, and 27.

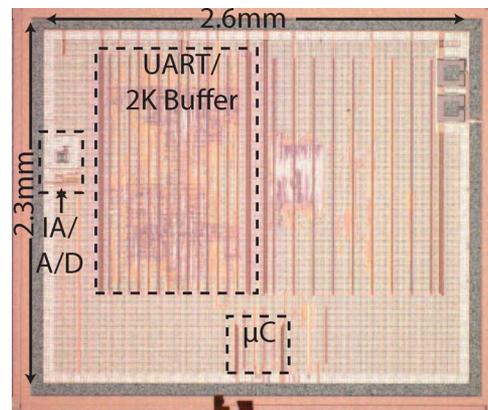


Fig. 13. Die picture of the larger SoC that used the level converter, showing the instrumentation amplifier, analog-to-digital converter, UART with 2K Buffer, and microcontroller ( $\mu$ C) [11].

an input supply of 227 mV. Even under extreme variation, the level converter can consistently convert from the subthreshold domain.

#### F. Extending Minimum Input Voltage

If the input supply voltage needs to be lowered further below 227 mV, two additional inverters can be added before the inputs of Fig. 4. By using a separate supply for these inverters and that of the input signal supply voltage, it is possible to lower the input signal supply voltage. Fig. 12 shows the minimum input supply voltage that would be usable by the inverters to be fully converted by stages one and two.  $V_{DD\_Inverters}$  is fixed at 220 mV, whereas the input signal supply voltage to the inverters is brought lower. Fig. 12 uses the same process corners and temperatures used in Fig. 11. The simulation shows a 32.7% or 74.4-mV drop of the input supply using this method. This technique is not typically needed, because the optimum energy point for subthreshold circuits is typically around or above 300 mV [4], [9], [12], [13].

### III. EXPERIMENTAL RESULTS

To verify its effectiveness and capabilities, we implemented the level converter in a bulk CMOS 130-nm test chip. The level converter was part of the interface between a SoC and other nominal voltage blocks [11]. Fig. 13 shows a die photo of the SoC that used the level converter. The size of the level converter is approximately 16 times the size of a minimum-sized standard cell inverter. In the context of the SoC, the

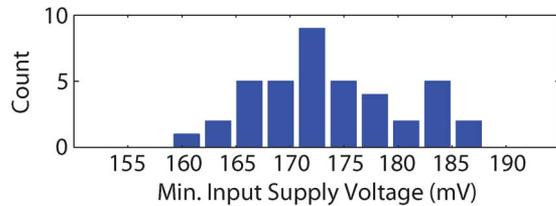


Fig. 14. Measured histogram of the minimum input signal supply that the level converter upconverts.

level converters reliably converted signals from a subthreshold processor running down to 280 mV (which is the optimum energy voltage) up to 1.2 V for the universal asynchronous receiver/transmitter (UART) and I/O.

#### A. Input Range

To verify the level converter's minimum input supply, we set  $V_{DD}$  to 1.2 V at room temperature, swept the input supply from 1.2 V down to 0, and measured the minimum input supply that produced a correct upconversion. Fig. 14 is a histogram of the minimum input supply converted for 40 level converters. Comparing Figs. 11 and 14 shows that the mean of the simulated TT, global variation, and measured level converters are within 15 mV of each other. The measured values are well within the upper bounds of simulation. The measured results also conclude that the level converter is able to convert  $V_{low}$ , in worse case, from 188 mV to 1.2 V. This demonstrates the level converter's effectiveness for interfacing between the subthreshold and higher voltage domains. It also shows the effectiveness of it operating in superthreshold mode as well since it correctly functioned across the full input range from this minimum value up to  $V_{DD}$ .

The optional operating method was found to decrease the convertible input supply voltage by 36% or 68 mV. The distribution is similar to Fig. 14, but the minimum input supply allowed is shifted down.

#### B. Measured Delay

It is important that the level-converter delay is small enough to not interfere with the device under test. Simulation results were used to allocate sections of the measured signal propagation path, which included I/O pads and other test-related circuits. The measured delay is larger than the 25-ns delay reported in Section II. This is due to process variation and differences between the parasitics of the particular testability path of the prototype and the parasitic environment of a typical application used in the simulations of Section II. Fig. 15 shows the experimental delay compared to the simulation results using the experimental signal path parasitic environment as a function of input supply voltage. The worst case measured delay is 57.9 ns when the input supply is 200 mV. As expected from the simulations in Section II, delay is relatively constant until the input supply voltage is less than 250 mV. The results show that the prototype circuit delay is within the range anticipated by the process variability, and our prototype process lies between the typical and slow process corners for the technology.

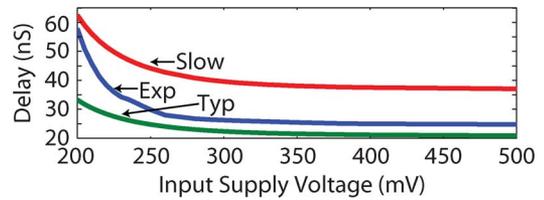


Fig. 15. Delay of the level converter. Typical and Slow are simulated from the two process corners TT and SS. The experimental delay is within the range of both the typical and slow simulations.

Our worst case experimental results show that the converter delay meets the clock frequency requirements of several published subthreshold applications [4], [9]–[11].

## IV. CONCLUSION

We have demonstrated a subthreshold level converter that is fabricated in a 130-nm process. The level converter successfully and reliably upconverts to 1.2 V a signal generated by a supply voltage ranging between 188 mV and 1.2 V, making it suitable for both subthreshold and DVS operation. Combining sizing, threshold voltage selection, and a diode-connected NMOS, our design overcomes the large  $I_{onP} - I_{onN}$  current imbalance. The level converter meets the requirements to interface subthreshold and nominal voltage circuits.

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