Canary Replica Feedback for Near-DRV Standby V_{DD} Scaling in a 90nm SRAM

- **Jiajing Wang and Benton H. Calhoun**
- *University of Virginia*
- *Charlottesville, Virginia*

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Outline

- Motivation
- Canary Feedback Scheme
- Canary Circuits Design
- Near-DRV V_{DD} Scaling
- Test Chip Implementation & Measurement
- Conclusion

Motivation – Leakage Power Reduction

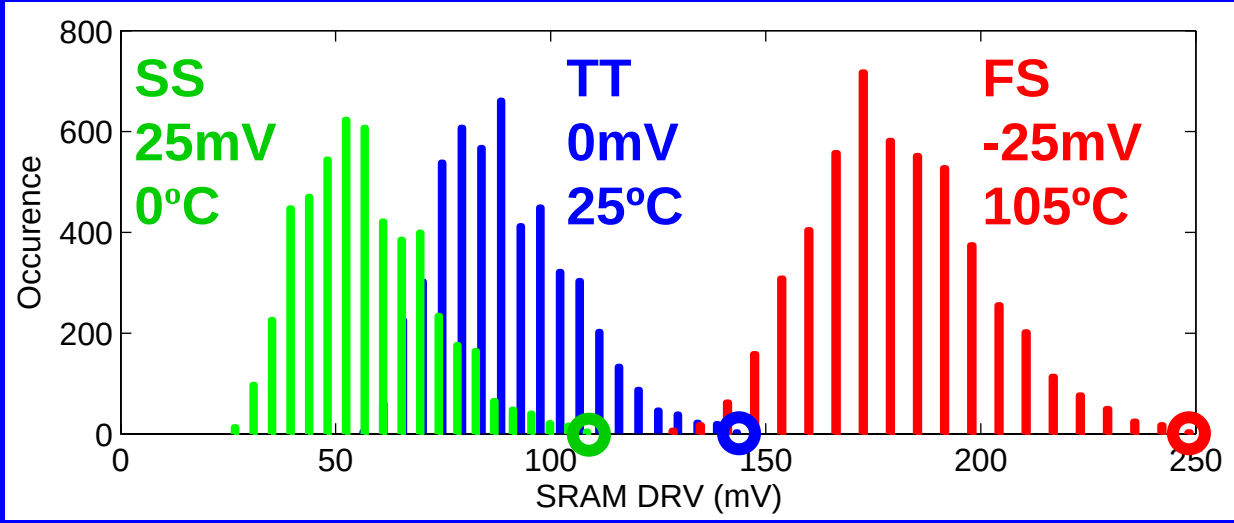
- Leakage power grows
- SRAM standby leakage power dominates
- Leakage power reduction by
  - V_{DD} scaling
  - Source biasing
  - Body biasing
  - High V_T FETs
  - etc.

Motivation – V_{DD} Scaling

- SRAM hold stability is degraded
- Data Retention Voltage (DRV):
  - The minimum V_{DD} for preserving cell state *or*
  - The V_{DD} when Static Noise Margin (SNM) is ZERO
- Cell hold failure
  - Occurs when current V_{DD} < DRV

Motivation – DRV

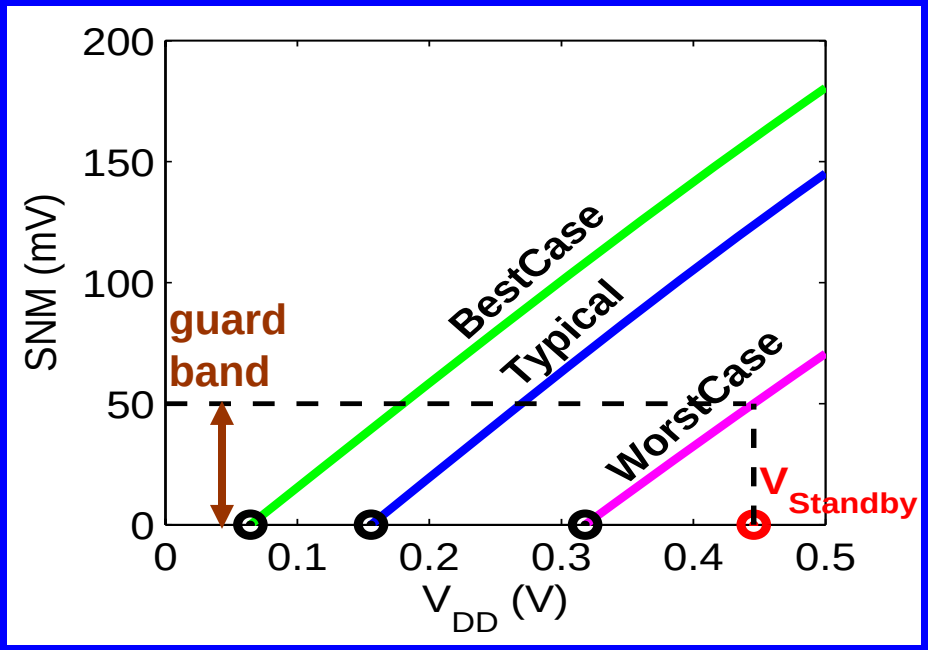
- Variability impacts DRV
- DRV of the cells is distributed
- Tail of the DRV distribution
  - Determines the min(V_{DD}) for SRAM array
  - Moves with global effects (i.e. PVT variations)



*** How to deal with the variations?**

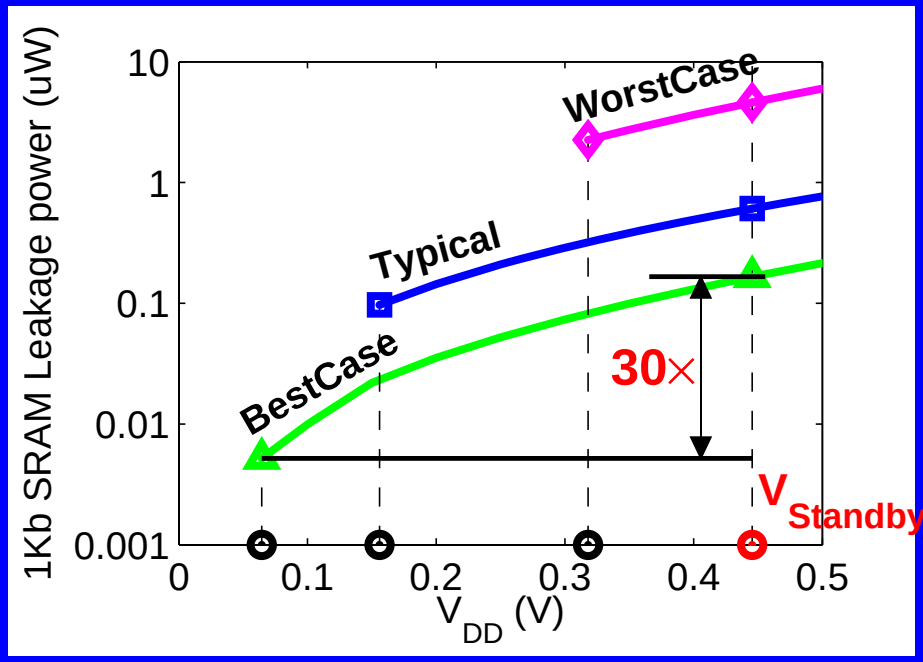
Motivation – Worst-case Approach

- Universal standby supply voltage ($V_{standby}$)
  - Applied to all the dies all the time
- $V_{standby}$ determined by the stability at
  - Worst scenario *and*
  - An extra guard band (e.g. 50mV SNM)



Motivation – Worst-case Approach

- **Advantage**
  - **Robust**
- **Disadvantage**
  - **Limit power savings of non-worst-cases**



*** Can we achieve aggressive power savings?**

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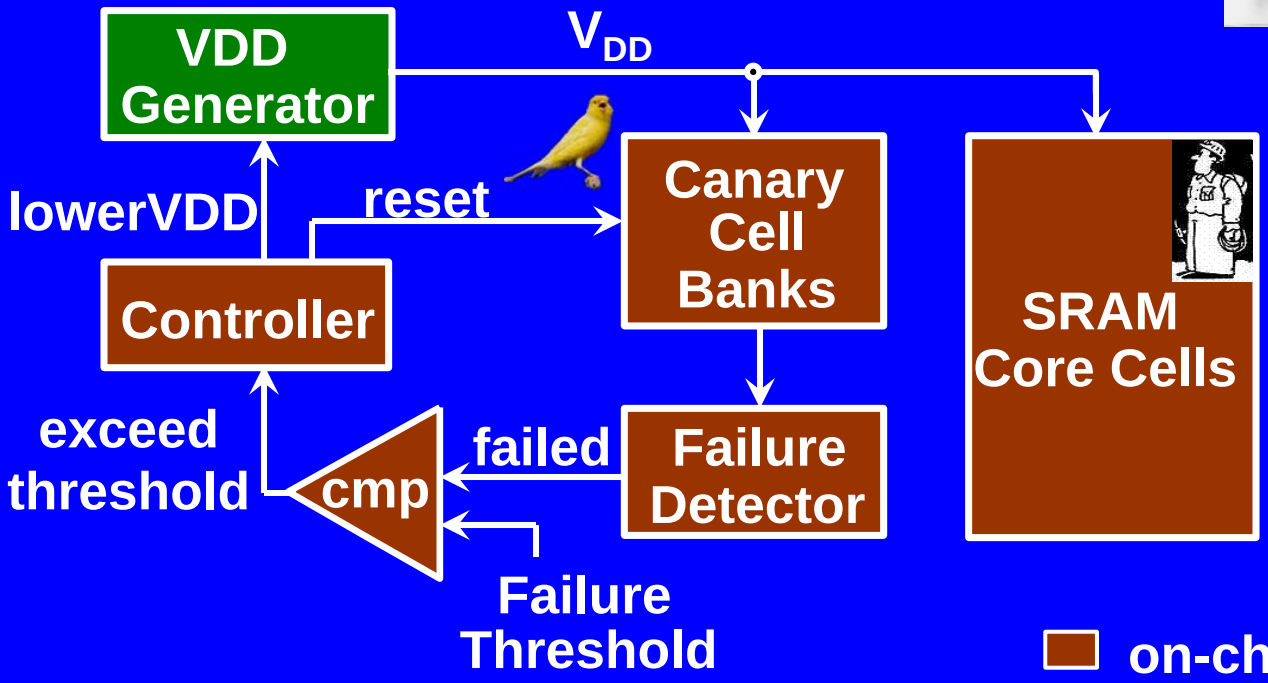
Canary Feedback Scheme

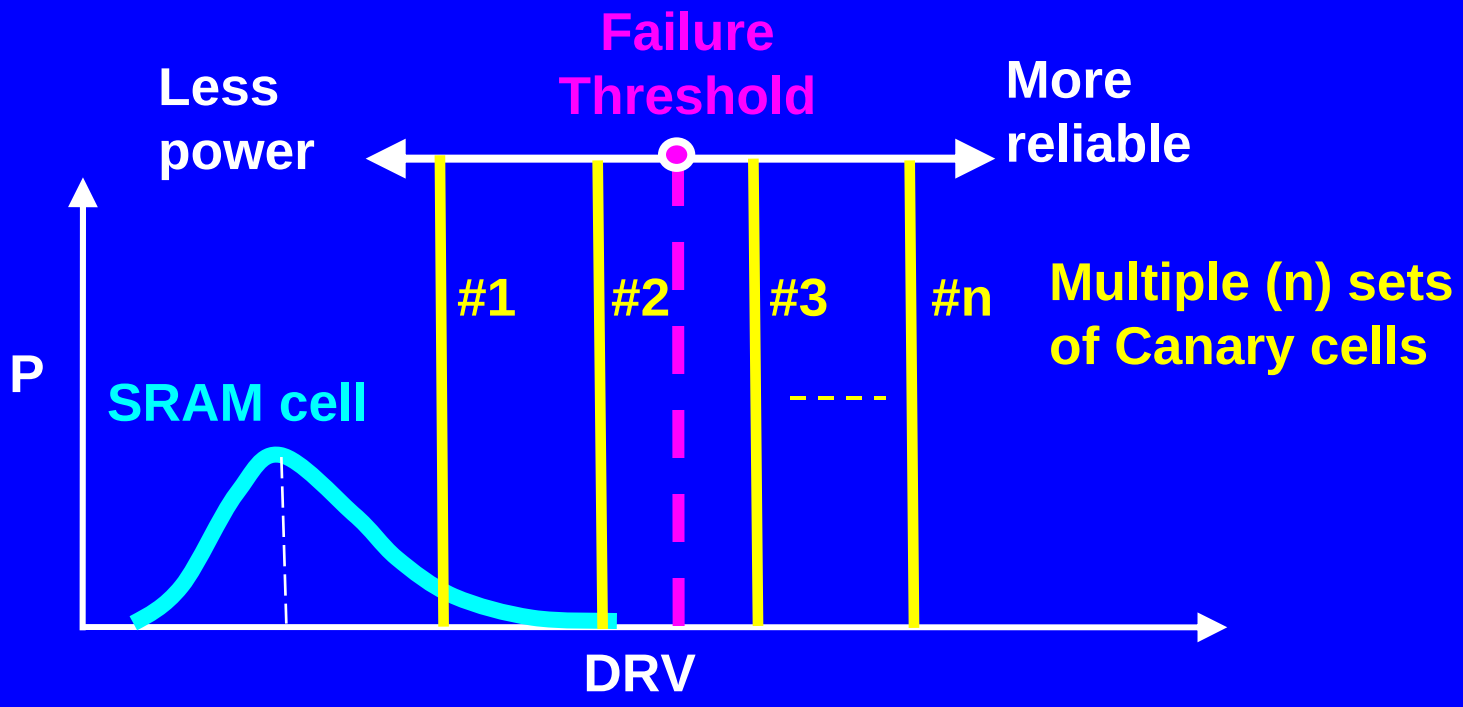
- Use replica bitcells (canary bitcells) inspired by canary birds
- Use Canary bitcells in closed-loop V_{DD} scaling

Canary bird: warning system for coal miner



Major Benefits

- Aggressive power savings by tracking global effects (i.e. PVT variations)
- Mechanism for tradeoff between data reliability and leakage power savings



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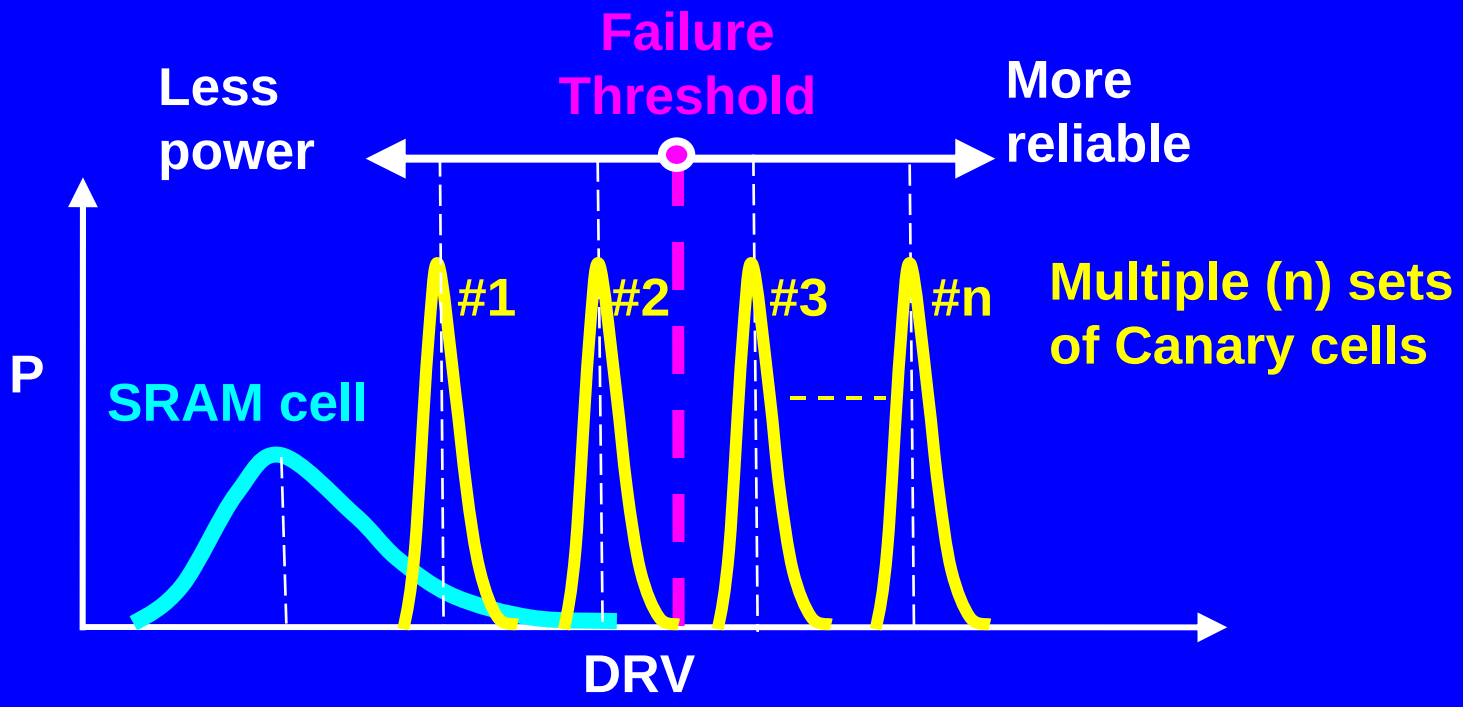

* A higher and tunable canary DRV is essential

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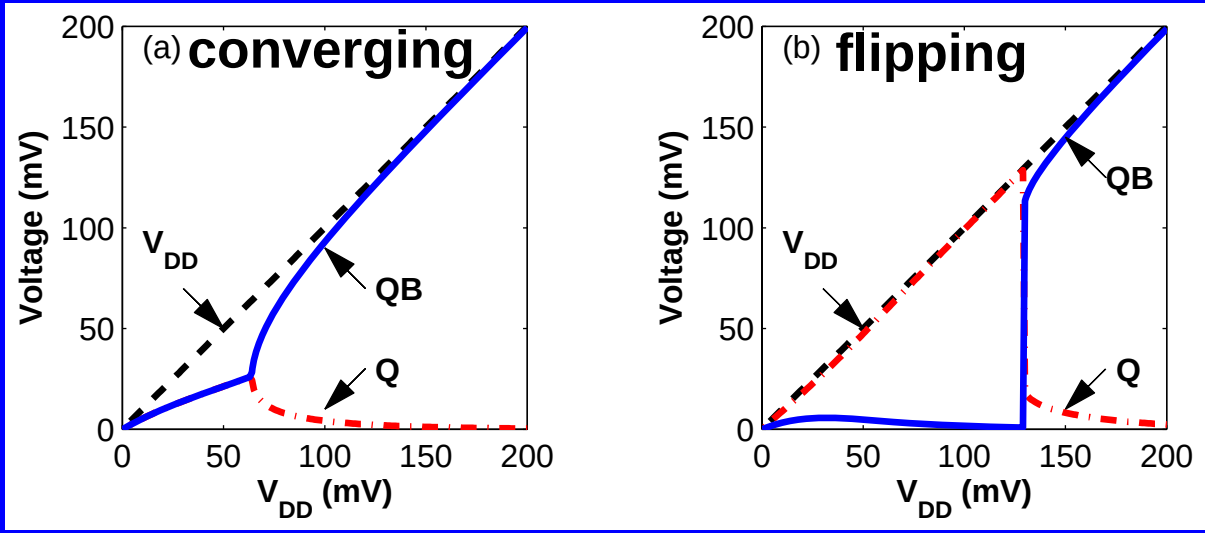
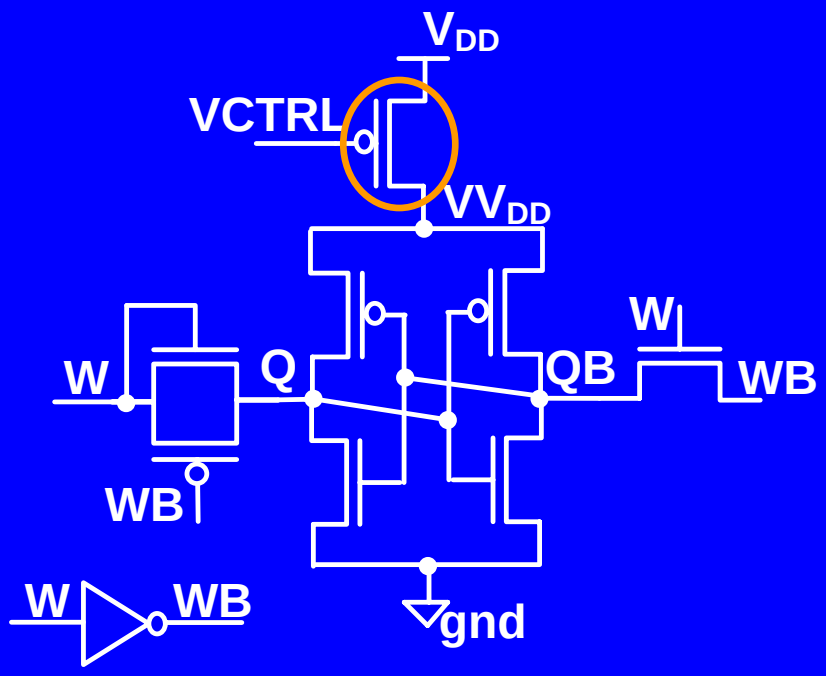
Cell Hold Failure

- 2 types
  - Converging failure
    - Occurs only in balanced (completely symmetrical) cells
    - Very rare under local variations
  - Flipping failure
    - Occurs in imbalanced cells

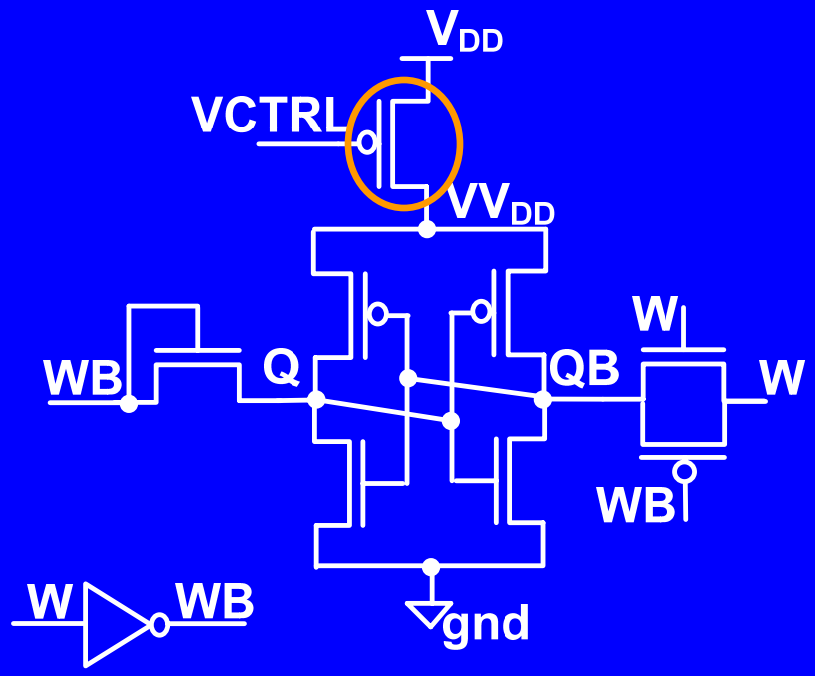


Canary Cell

- Higher canary DRV by
  - PMOS header
  - Worst bitline leakage
  - Worst data pattern (or separate cell ‘0’ & ‘1’ for simplicity)



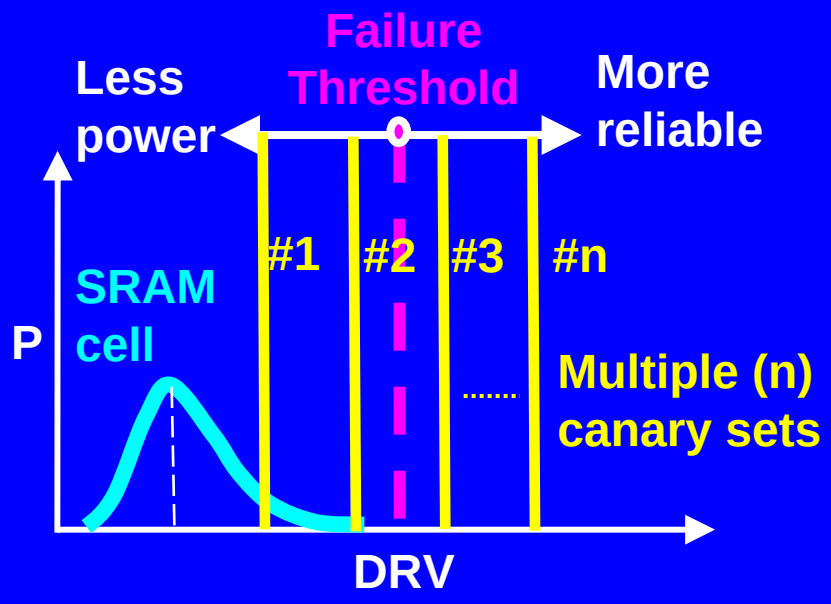
Canary Cell ‘1’



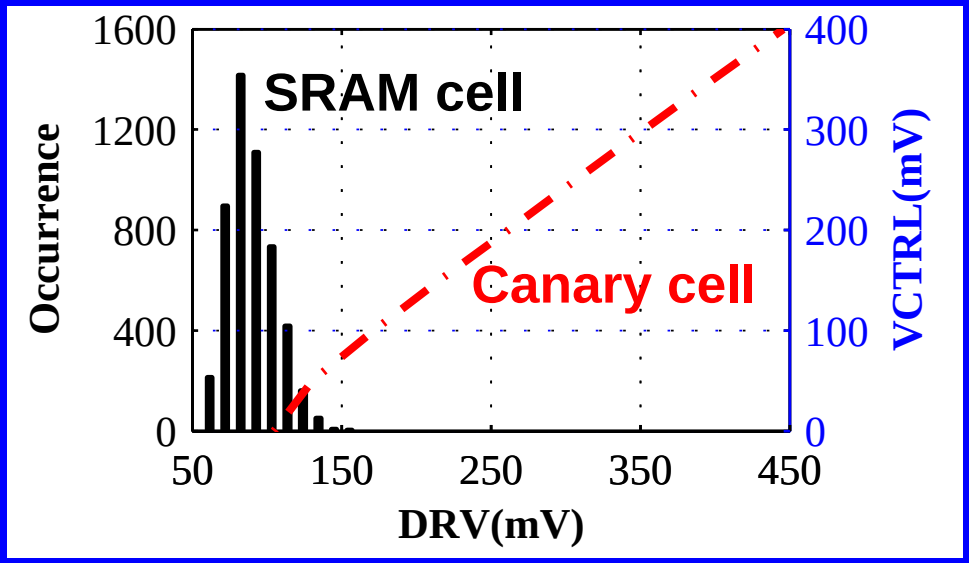
Canary Cell ‘0’

Canary Cell

- Tunable canary DRV by
  - Altering gate voltage (VCTRL) of PMOS header
- Canary set with larger VCTRL has a higher DRV



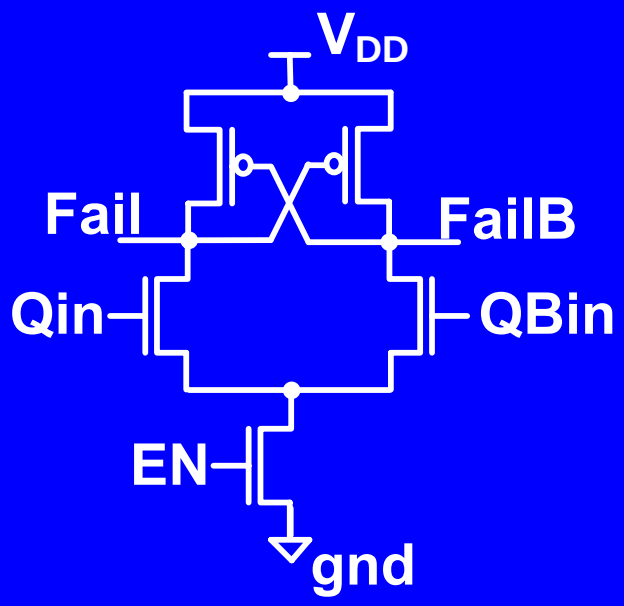
Multiple canary sets design concept

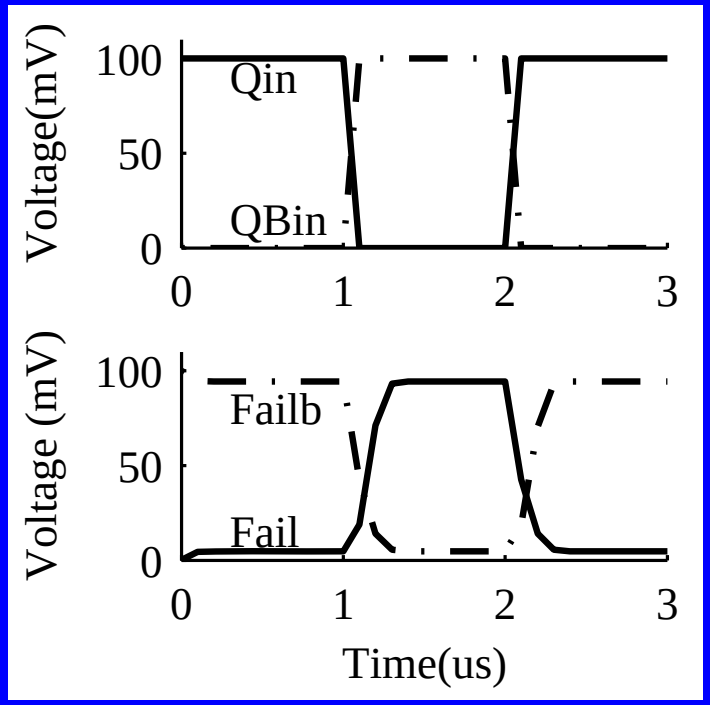


Simulated canary DRV vs. VCTRL relative to SRAM DRV distribution from 5-k Monte-Carlo

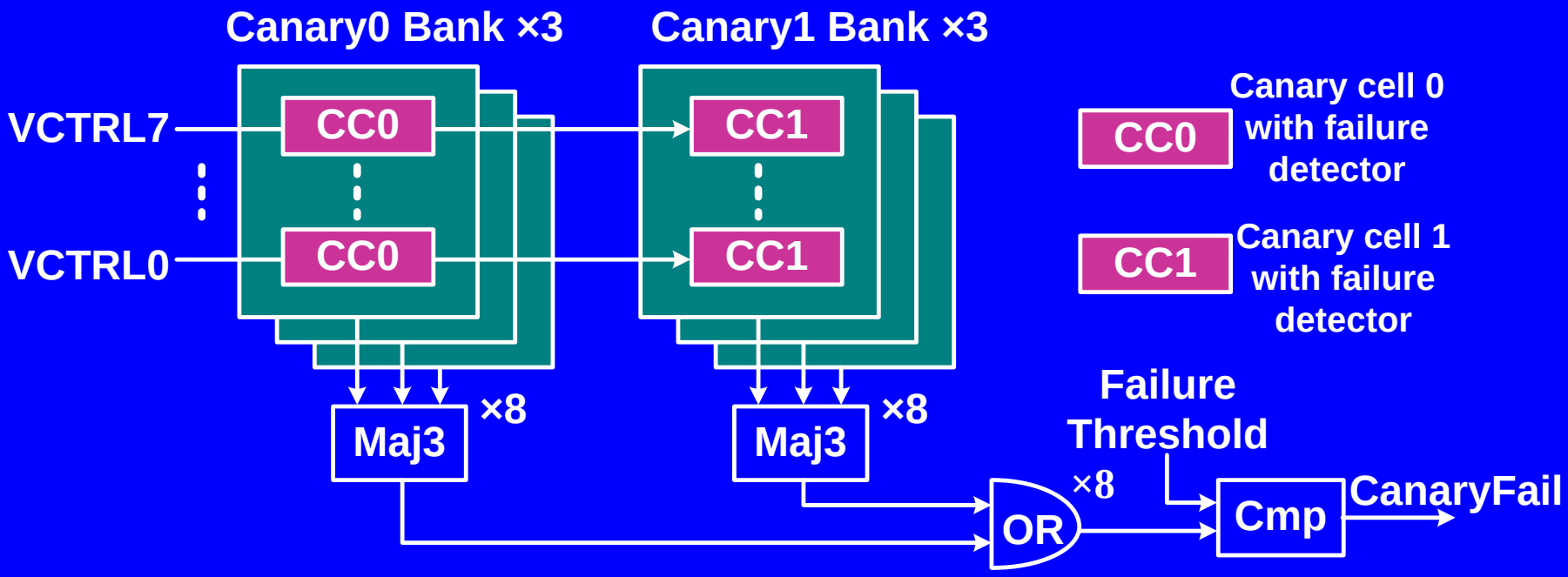
Failure Detector

- Each canary cell connects its own failure detector
- Use sub-threshold SA to detect flipping failures





Canary Bank



- 8 canary sets/rows with respective VCTRL
- 3-way redundancy
- OR operation on canary cell ‘0’ and ‘1’
- Failure threshold comparator

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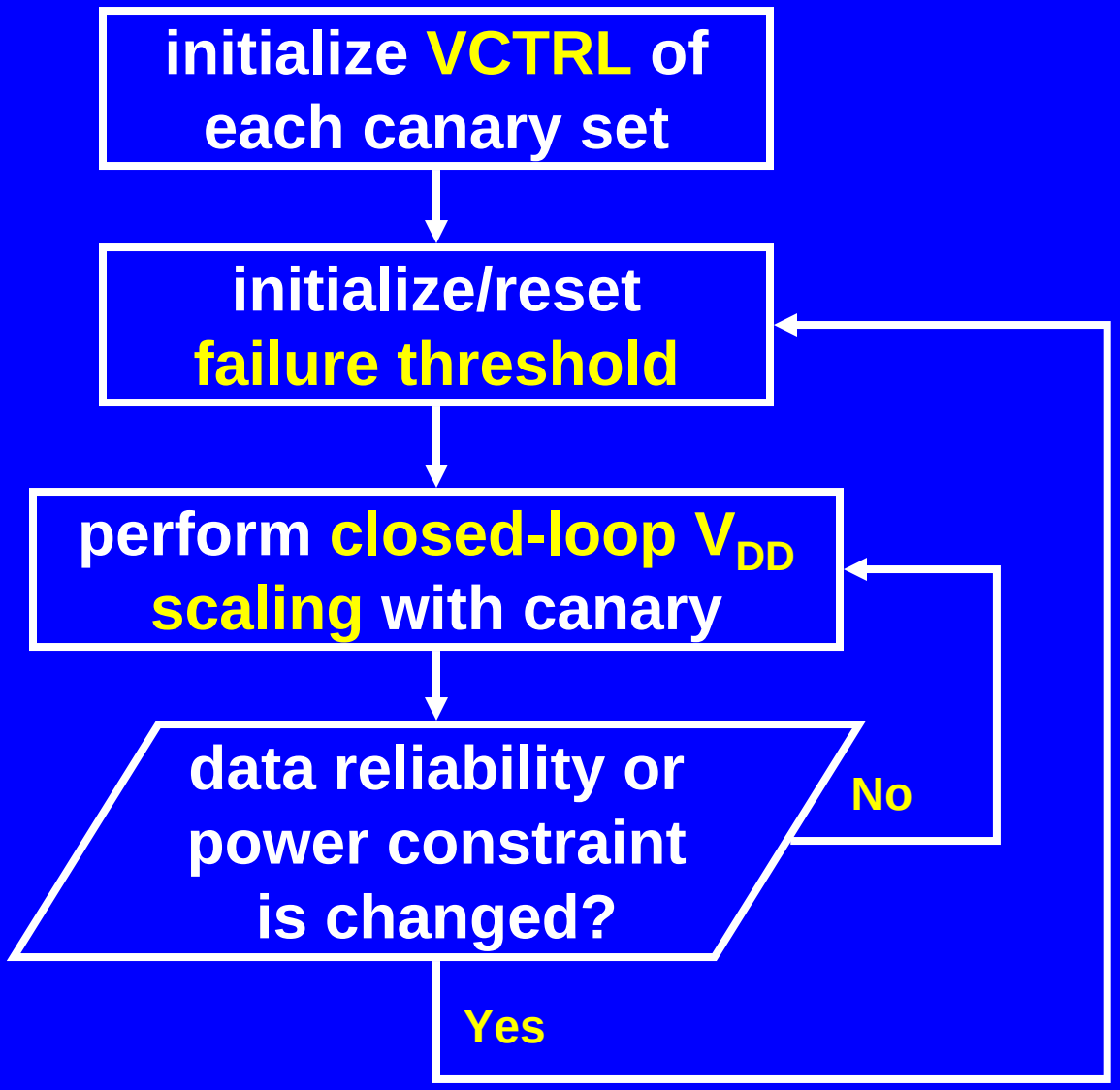
Near-DRV V_{DD} Scaling Procedures



SRAM DRV Characterization

- **Measurement at test time**
  - **Accurate but expensive**
- **Traditional Monte-Carlo (M-C) Simulation**
  - **Accurate but too time-consuming for large arrays**
- **Alternative fast methods**
  - **A new DRV model based on SNM [1]**

$$\max(DRV) = \frac{1}{k}\left(\sqrt{2}\sigma_0 \cdot erfc^{-1}\left(2 - 2\sqrt{\frac{m-1}{m}}\right) - \mu_0\right) + V_0$$

  - **The Statistical Blockade tool [2]**
    Fast Monte-Carlo for simulating rare events

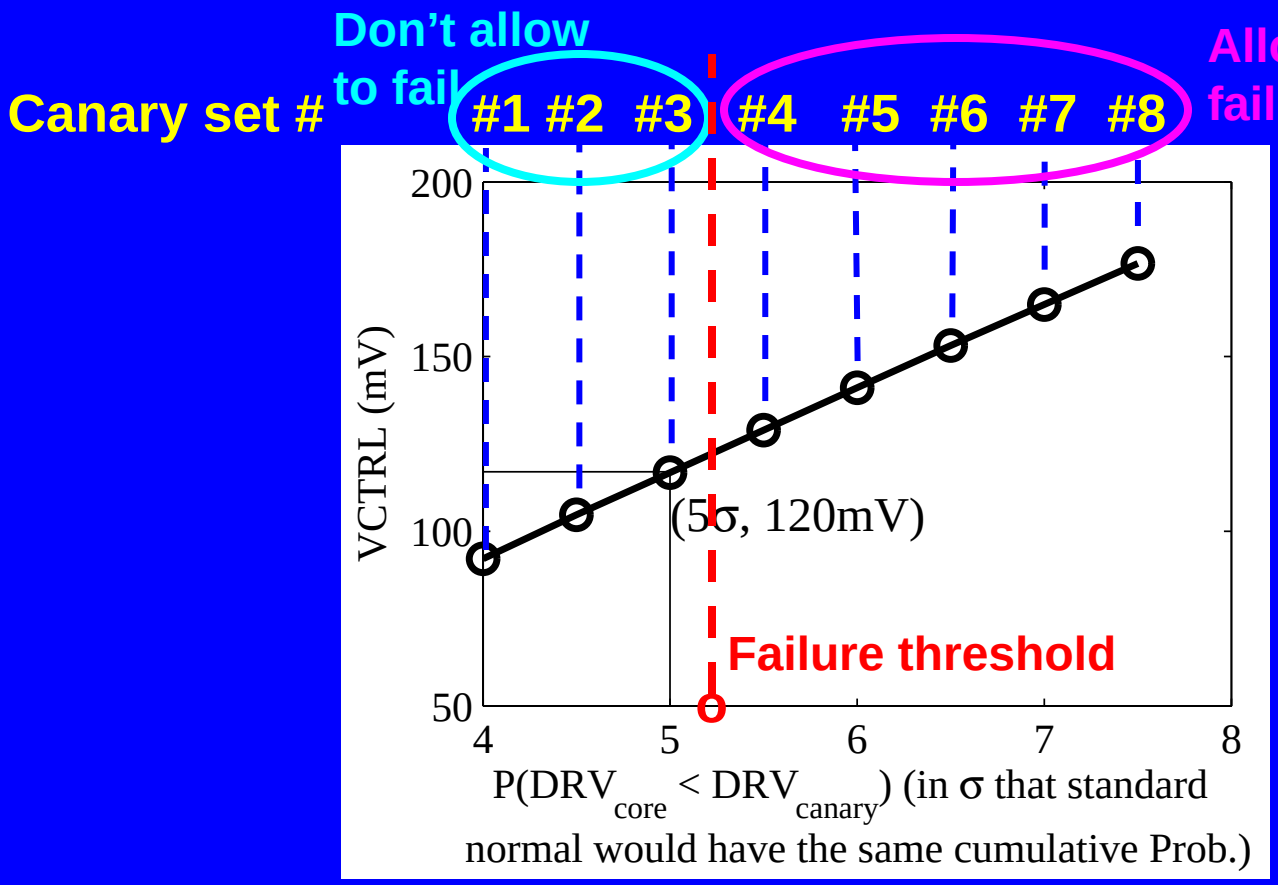
Each has <u>≤2%</u> avg. error rate & <u>≥10^4x</u> speed-up compared with M-C [1]

[1] J. Wang, A. Singhee, R. A. Runtenbar, and B. H. Calhoun, "*Statistical Modeling the minimum standby supply voltage of a full SRAM Array*", ESSCIRC 2007.

[2] A. Singhee and R. A. Runtenbar, "*Statistical Blockade: A Novel Method for Very Fast Monte Carlo Simulation of Rare Circuit Events, and Its Application*", DATE 2007.

Canary Configuration

- Choose VCTRLs of canary sets based on
  - SRAM DRV estimation *and*
  - Linear dependency of Canary DRV on VCTRL
- Pick failure threshold based on the reliability constraint

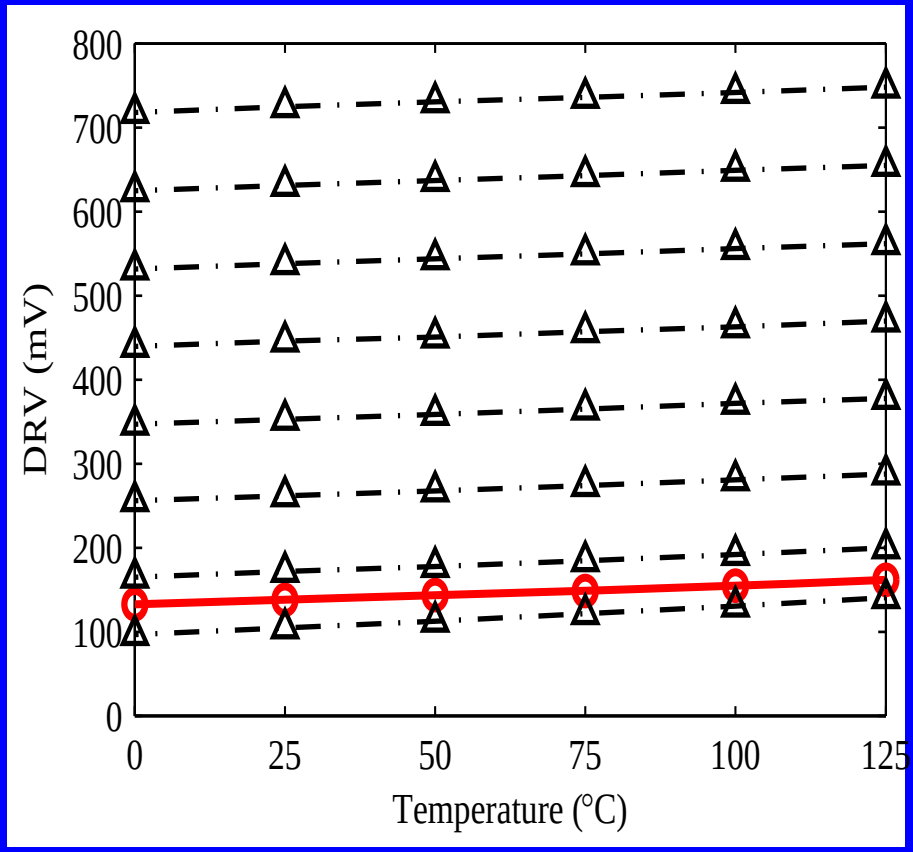


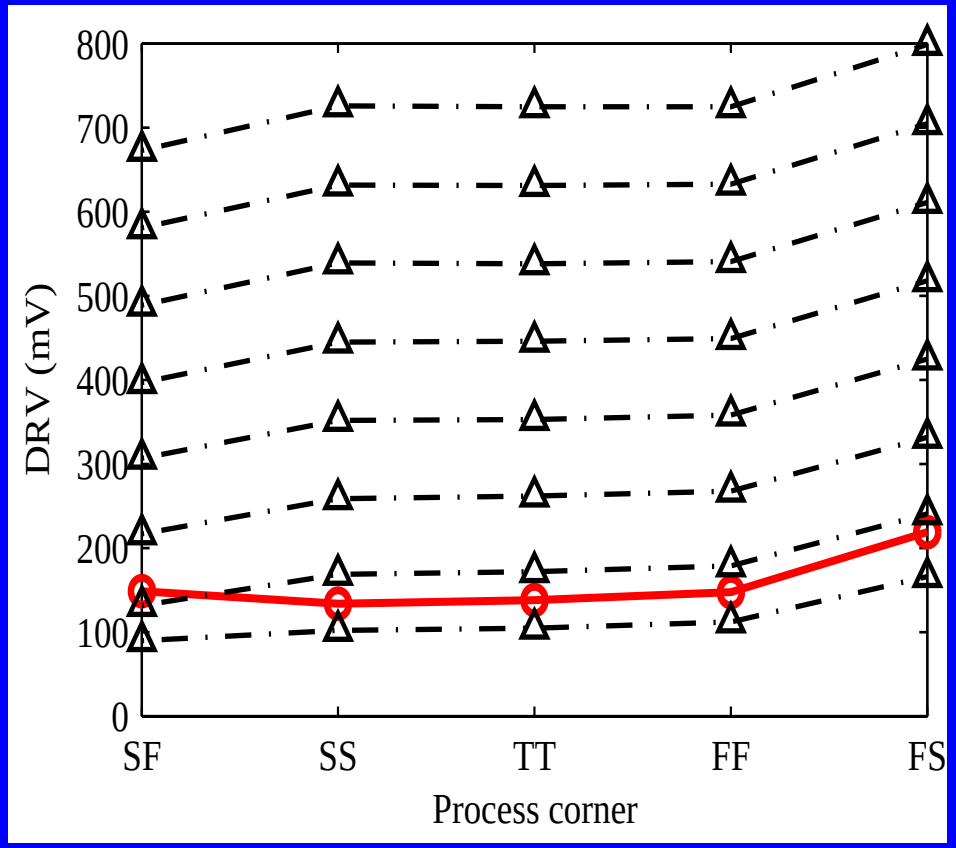
e.g. 5σ (99.9999713%) SRAM cells will fail after canary set #3 (120mV VCTRL)

Canary Tracking Variations

Worst DRV_{core} (e.g. 1Kb SRAM)

DRV of each canary set





- Canaries track temperature changes
- Canaries track global process variation

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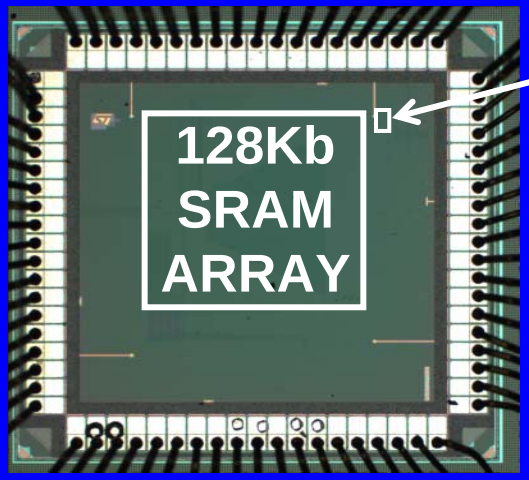
90nm CMOS Test Chip

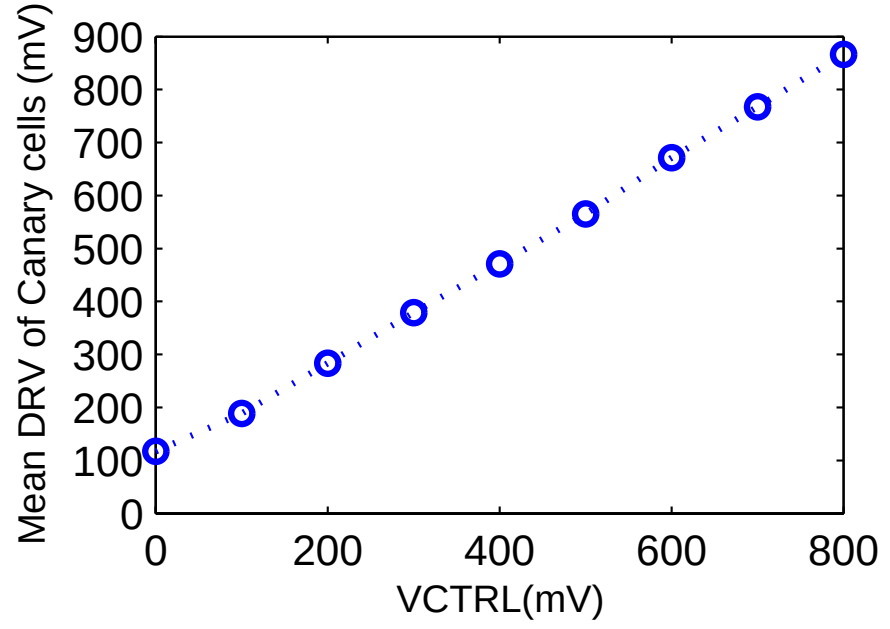
- 90nm bulk, 7 metals, 1.0V VDD
- Die area:
  1.51mm² x 1.51mm²



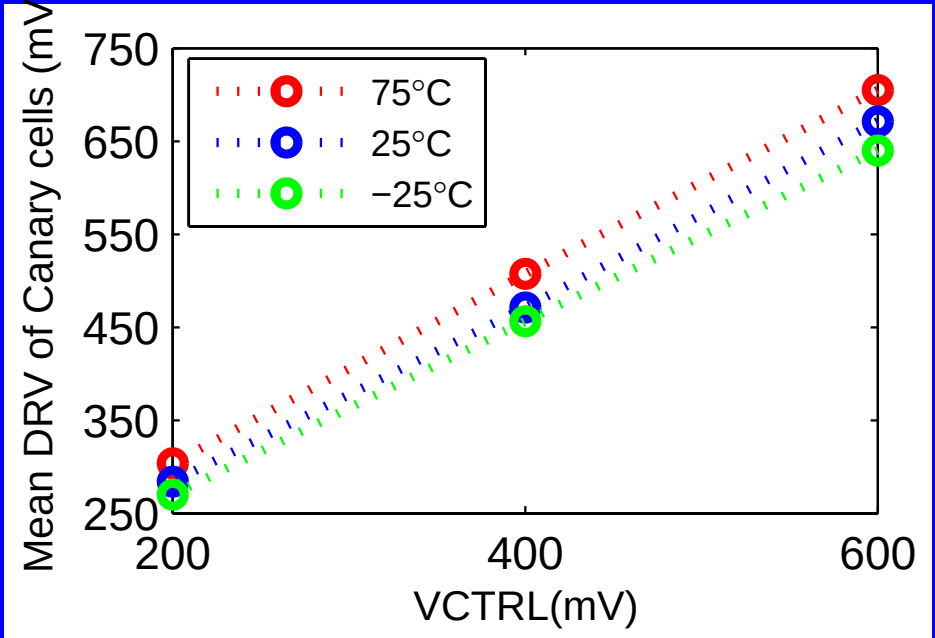
- Active circuit area
  - SRAM array (128Kb): 700x620um²
  - Canary replicas (8x3x2b): 40x70um²
  - Area overhead: 0.6%

Test Chip Measurement 1

- **Measured Canary-cell DRV vs. VCTRL**

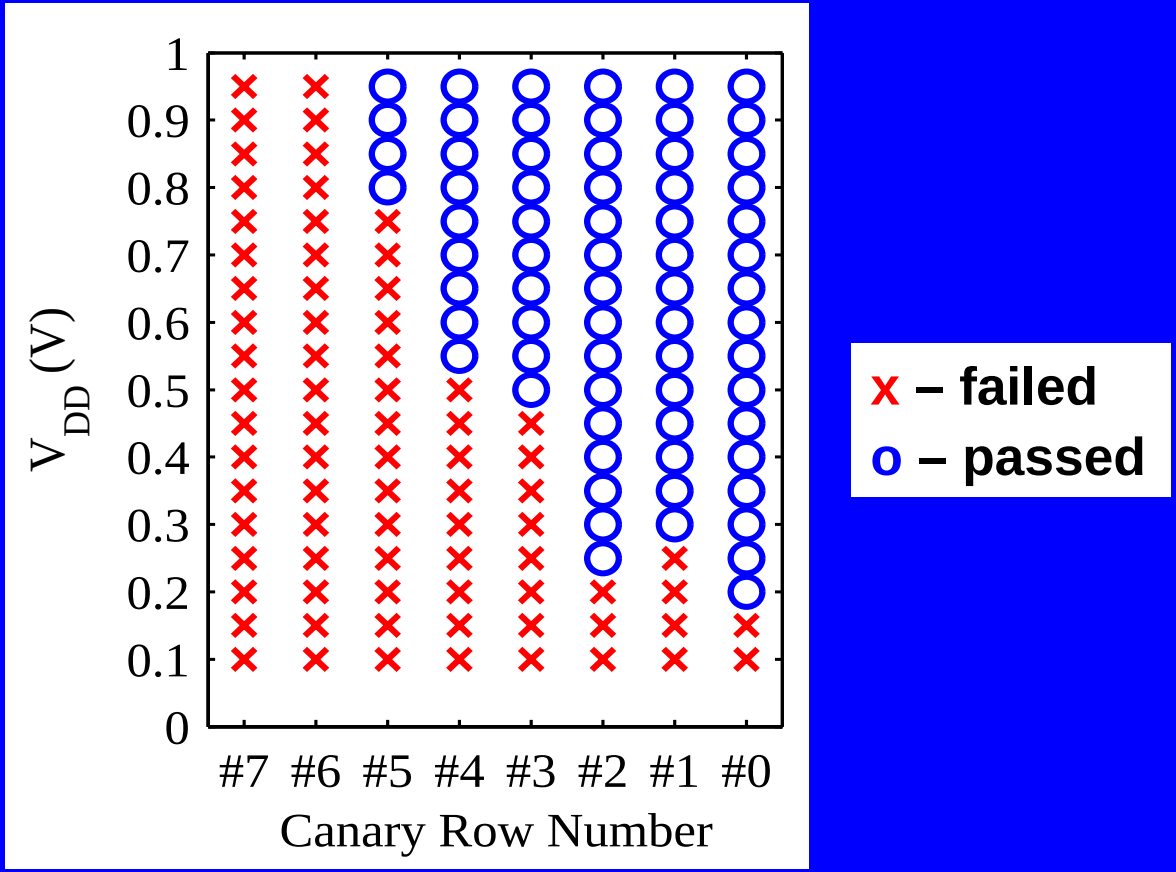


- **Measured Canary-cell DRV tracks temperature variation**



Test Chip Measurement 2

- More canary sets fail with V_{DD} scaling



Conclusion

- New canary feedback scheme is proposed to implement aggressive V_{DD} scaling for SRAM standby leakage power reduction
- By controlling PMOS header, canary sets reliably fail in a continuum at higher voltages than the average of SRAM cells
- Canary cells can successfully track global variations
- Our canary scheme also allows to trade off data reliability with power savings
- Measurement of a 90nm test chip confirms the functions of canary scheme