A 6.45 μW Self-Powered SoC With Integrated Energy-Harvesting Power Management and ULP Asymmetric Radios for Portable Biomedical Systems

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***Abstract*—This paper presents a batteryless system-on-chip (SoC) that operates off energy harvested from indoor solar cells and/or thermoelectric generators (TEGs) on the body. Fabricated in a commercial 0.13 μW process, this SoC sensing platform consists of an integrated energy harvesting and power management unit (EH-PMU) with maximum power point tracking, multiple sensing modalities, programmable core and a low power microcontroller with several hardware accelerators to enable energy-efficient digital signal processing, ultra-low-power (ULP) asymmetric radios for wireless transmission, and a 100 nW wake-up radio. The EH-PMU achieves a peak end-to-end efficiency of 75% delivering power to a 100 μA load. In an example motion detection application, the SoC reads data from an accelerometer through SPI, processes it, and sends it over the radio. The SPI and digital processing consume only 2.27 μW, while the integrated radio consumes 4.18 μW when transmitting at 187.5 kbps for a total of 6.45 μW.**

***Index Terms*—Digital signal processing, energy harvesting, internet-of-things, system-on-chip, wakeup radios.**

I. Introduction

COMPUTING systems catering to the 1 trillion node Internet of Things (IoT) will require sensing platforms that support numerous applications while using energy harvesting to avoid the cost and scalability challenge of battery replacement in such large numbers. This paper presents a system on chip (SoC) designed for physiological sensing on the body. The proposed SoC provides a flexible platform that can be extended for broader use in other IoT applications as well. As described in Fig. 1, these IoT systems will be deployed in a wide range of applications from health monitoring (e.g., blood pressure, electrocardiogram (ECG), etc.), infrastructure and environmental monitoring, home automation, and many others. Since these systems must operate in energy-constrained environments where every small amount of stored energy is essential, there is a need to harvest from diverse sensing modalities such as thermoelectric generators (TEGs) or photovoltaic (PV) solar cells. Moreover, these systems need to start-up and operate from very low input voltages to sustain themselves. Most TEGs provide very low output voltages that cannot be used directly and thus needs to be boosted up and regulated to provide the power supplies (V_{DD}s) of the system [1]–[3]. Hence, the system can start only after the V_{DD}s have become operational. Therefore, the power supplies for ultra-low power (ULP) systems need to be functional at low input voltages. These systems also must be able to acquire (for instance ECG signals), process, store, and transmit

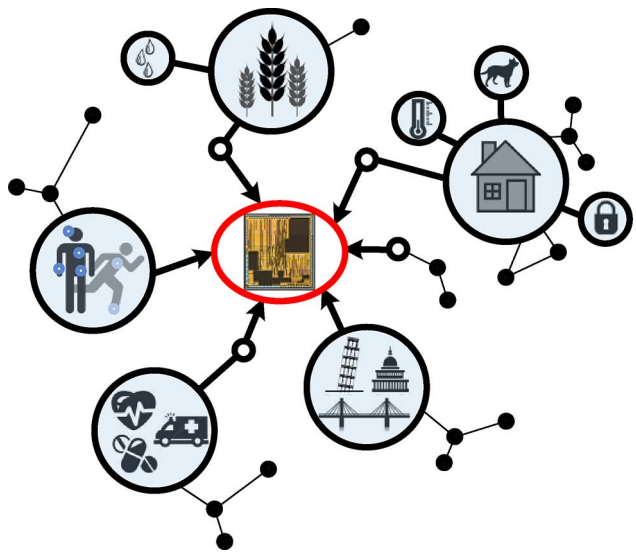

Fig. 1. Motivation for tightly integrated systems to support diverse applications.

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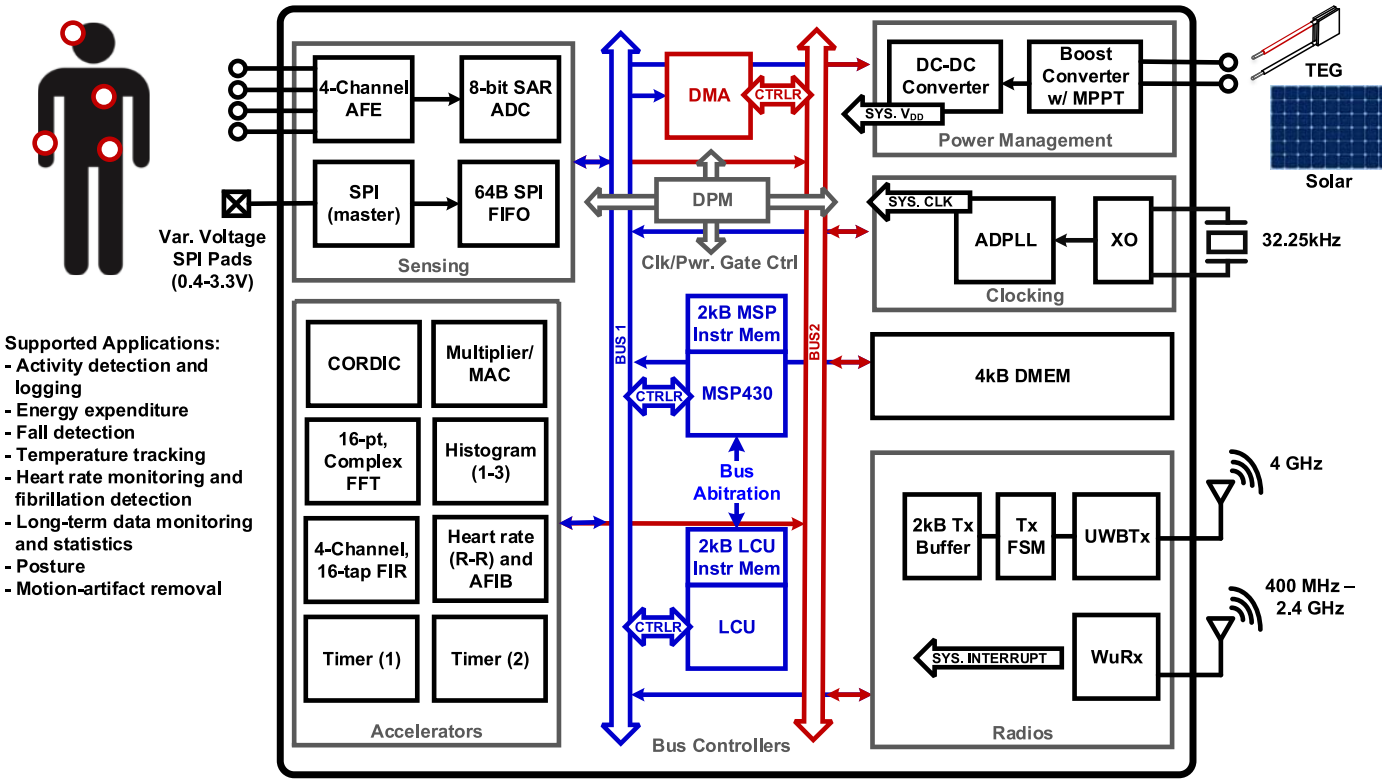

Fig. 2. System block diagram for the SoC, highlighting supported applications and interfaces [16].

data wirelessly to other IoT systems or to a base-station without exceeding their limited energy budget.

Previous IoT SoCs achieve high integration with energy harvesting capabilities [4]–[7], but they tend to have limited application support, need higher end-to-end power efficiency, and require duty cycling for RF communication. This work demonstrates a highly integrated, flexible SoC platform targeting on-body sensing with multiple sensing modalities and a comprehensive digital processing engine to allow a wide range of applications. The SoC also integrates an energy harvesting and power management unit (EH-PMU) with a boost converter for solar and TEG energy harvesting and a single-inductor, multiple-output (SIMO) DC-DC converter for high end-to-end self-powered efficiency. The boost converter harvests energy from the input power source and boosts it to a higher voltage that is stored on an external capacitor, which then serves as the input to the SIMO regulator. An asymmetric radio leverages ULP ultra-wideband (UWB) transmission and an always-on ULP receiver to reduce RF power significantly relative to prior SoCs for communication at higher data rates in an energy-harvesting platform. Section II describes the proposed digital architecture. Section III describes the EH-PMU including the energy harvesting boost converter with maximum power point tracking capability and the SIMO regulator that provides supply voltages to the SoC. Section IV describes the proposed UWB asymmetric radio and the ULP wake-up receiver. Section V presents the measurement results, and Section VI concludes the paper.

II. SoC Digital Architecture

Fig. 2 shows the main building blocks of the proposed SoC. The SoC has two main sensing interfaces: a 4-channel (2 μW/channel) analog front-end (AFE) [5] with an 8-bit analog-to-digital converter (ADC) [5] and SPI with variable voltage output pads (0.4-to-3.3 V) for commercial sensor compatibility. The Opencores MSP430 (OMSP) processor [6] and a suite of accelerators can execute numerous biomedical and environmental signal processing algorithms (e.g., filtering, peak detection, histograms) combining ASIC energy efficiency and flexibility. A Lightweight Control Unit (LCU) can manage chip data and node control while the OMSP is off, and uses a custom instruction set architecture (ISA) and interrupt-driven programs to reduce the program size. The chip's flexible clocking unit, containing a programmable all digital phase locked loop (ADPLL) and system clock configurability, can drive the system clock from a low power crystal. The digital blocks run in the sub-threshold regime on a 0.5 V supply delivered by the PMU.

A. Bus Architecture

The chip uses two 16-bit independent buses (Fig. 2), each controlled by a separate controller. Bus 1 is controlled by either the OMSP or LCU, while Bus 2 is controlled by a two-channel DMA. Both buses have access to all the peripherals within the SoC. At startup, the LCU is the main controller on the chip and can configure the OMSP as the main controller of Bus 1 or as a bus peripheral that is used only for ALU or background operations.

Since the bulk of data in this SoC needs to be transferred between the various peripheral blocks and the on-chip memories, the DMA was designed to manage these transfers efficiently on Bus 2 without constantly engaging the Bus 1 controller (LCU or OMSP). The DMA can be programmed using the controller on

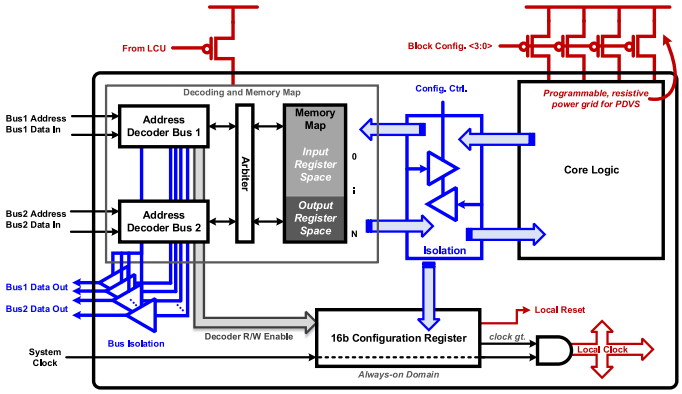

Fig. 3. Block-level architecture of the peripheral units showing fine-grained clock and power gating [16].

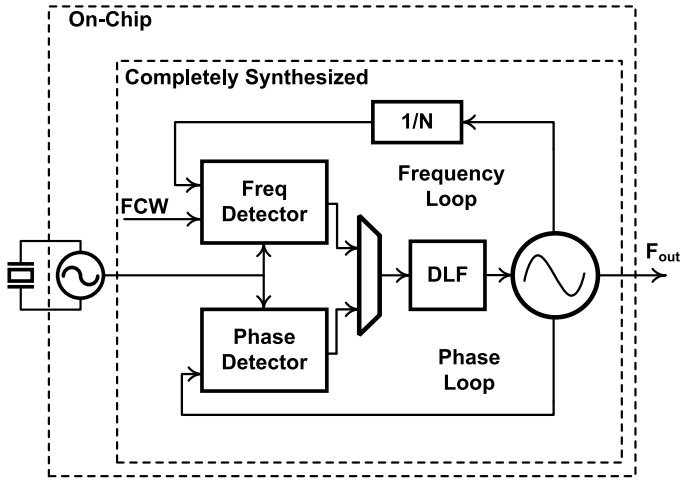

Fig. 4. The integrated ADPLL architecture [19].

Bus 1 to complete data transfers in the peripheral memory space. Programmable options for each channel include source address, destination address, the number of transfers, the transfer type (e.g., peripheral to peripheral or memory to peripheral), intervals between each transfer, and the transfer mode (static, increment, decrement, or round robin). Both channels can be active at once, but one channel has higher priority to resolve conflicts.

All blocks on the chip are memory-mapped peripherals that allow simultaneous access via either bus. Peripheral block wrappers decode and route bus data and manage independent block reset, clock gating, power gating, and power mode settings. Most peripherals contain three power domains: a configuration domain, a bus decoder domain, and a block core logic domain (Fig. 3). The configuration domain is an always- on domain containing the configuration registers that maintains the block state. The bus decoder domain can be power-gated by the LCU when access to the block is not needed. The core logic domain can be turned on/off using the configuration registers.

B. Flexible Clocking

The SoC has a flexible clocking scheme where the system clock can be derived from one of three sources: an external clock source, an integrated crystal oscillator (31.25 kHz) or an on-chip ADPLL [19] with a programmable output frequency between 187.5 kHz and 500 kHz. A digital clock module allows the LCU or the OMSP to control the clock source and to reset the entire SoC. Fig. 4 shows the dual-loop architecture of the ultra-low power ADPLL. The proposed architecture eliminates the divider to consume 300–600 nW from the 0.5 V supply with $\text{jitter} < 0.1\%$ in 0.07 mm^2. The entire ADPLL was implemented using standard digital design flows and automatic place and route (APR). The reference to the ADPLL is derived from the integrated 31.25 kHz crystal oscillator [9]. This oscillator draws a large current on startup to speed up the time to oscillation. Then its internal feedback loop quenches the amplifier so that the oscillator settles into a low power steady state in which it consumes only 29 nW.

C. On-Chip Memory

The chip has a 4 kB data memory and three 2 kB memories: the LCU instruction memory, the OMSP instruction memory, and the radio transmitter buffer. To enable sub-threshold operation, the memories are made up of 8T SRAM bit-cells and employ a read before write scheme to address half-select challenges. The memories are partitioned into 1 kB banks that can be independently power gated when not needed. The arrays operate reliably down to 0.35 V, although they share the 0.5 V digital supply.

D. Hardware Accelerators

The SoC also has a suite of programmable hardware accelerators to support energy efficient digital operation for common functions including an FIR filter, a CORDIC block, an FFT/IFFT, two timer modules, a multiplier, a histogram, and a heart rate (R-R)/atrial fibrillation (AFIB) detection block. The FIR is a four-channel, 16-bit filter, with each channel having up to 16-taps. The number of coefficients, number of active channels, and number of parallel filters are programmable. Each channel can be independently clock gated when not in use.

The CORDIC block implements the following mathematical functions: sine, cosine, arc-tangent, square root, hyperbolic sine/cosine, exponential and natural logarithm. These functions are essential for health monitoring applications such as arrhythmia classification, auscultation aids, or gait speed estimation.

The 16-point, complex FFT and IFFT block repurposes a single radix-2 butterfly per clock cycle and uses in-place memory addressing to reduce the memory requirements. The peripheral set also includes two, independently controlled timers for general-purpose use. The timers can be programmed to increment or decrement, rollover, and have a divided-down clock input for increased range. Each timer generates an interrupt to the LCU and/or OMSP when it expires. The block also has a capture and compare feature. The implemented multiplier from Opencores [6] can be configured to do an unsigned or signed multiplication/MAC. The histogram block can construct up to three histograms of data over time. The bin thresholds and number of active bins are programmable. Each histogram can contain up to 32 bins. One of the histograms has the option of only recording data when its value exceeds a programmable

threshold or stopping data acquisition once a certain number of events have been recorded.

The RR block implements a simplified version of the Pan-Tomkins algorithm [11] to calculate the R-R interval. The output of the RR block goes into the AFIB block that can detect and count AFIB events using the algorithm in [20]. The performance and accuracy of these blocks was evaluated extensively in [5].

E. Digital Power Management

The SoC also contains a digital power management unit (DPM) that monitors the harvested energy by measuring the voltage on the storage capacitor, and controls the different peripherals to ensure that the chip does not lose power when energy-harvesting conditions are poor. This feature was introduced in [5], [10] and enhanced in this SoC to provide more flexibility [16]. The DPM has three voltage thresholds that set the operating mode of the chip (green, yellow, or red). In green mode, the storage capacitor is nearly full, and the chip can perform any functionality. In yellow mode, the storage capacitor is being drained, and the chip must use its energy resources more efficiently. In red mode, the chip is approaching loss of power, and only essential operations must be performed. In this implementation, the three thresholds and operating modes are programmable. When programming the operating modes, the user determines the power and clock gating options for every digital peripheral on the chip. Adding this feature will allow the users the flexibility of determining what operations to prioritize. The DPM can also be programmed to sample the capacitor voltage from the on-chip ADC or a temperature/PVT invariant ring oscillator (RO) [21]. The RO is powered from the unregulated voltage of the storage capacitor. The DPM counts the number of pulses from the RO for a user-defined programmable time-period to infer the capacitor voltage. This value is compared against the programmable thresholds to determine the operating mode. Additionally, the RO is duty-cycled and sampled at a programmable rate based on the types of harvesting modalities, the power consumption and the storage capacitance. The RO reduces the burden on the ADC when the AFE is used to sample input signals.

III. Energy Harvesting & Power Management

The integrated energy harvesting and PMU couples a boost converter [8], [14] and a SIMO DC-DC regulator for power delivery to the SoC. Fig. 5 shows the complete powertrain architecture. The EH-PMU leverages two off-chip high-Q inductors (for the boost converter and the regulator) and an off-chip storage capacitor (or a super-capacitor) for storing harvested energy. The boost converter [8], [14] can harvest from a photovoltaic (PV) solar cell (e.g., with open circuit voltage of 1.7 V) or from a TEG (e.g., with input voltage V_{IN} as low as 10 mV) and charge the storage capacitor up to $V_{CAP} = 1.4$ V. An integrated maximum power point tracking (MPPT) circuit described in [8] tunes the input impedance of the boost converter to extract maximum energy from the ambient source (either TEG or PV). The SIMO utilizes a buck-boost architecture to provide regulated outputs of 1.2 V and 0.5 V from a minimum input voltage (V_{CAP}) of 0.7 V and improves the end-to-end efficiency over [5], which used

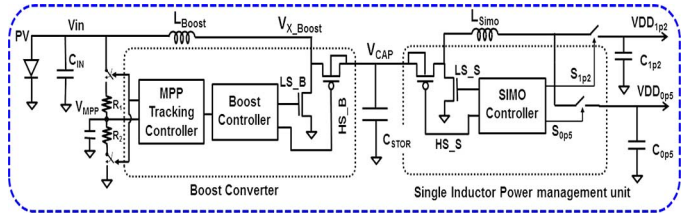

Fig. 5. Energy harvesting and SIMO power management unit [16].

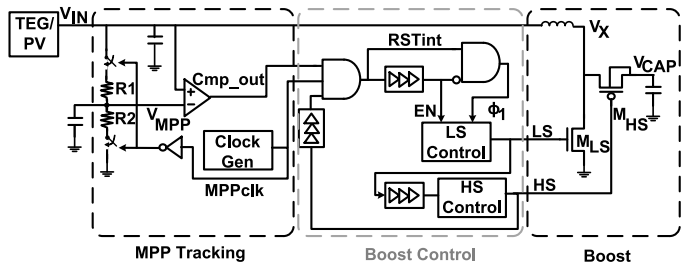

Fig. 6. Architecture of the boost converter [8], [14].

on-chip low drop out (LDO) regulators. Both the SIMO and the boost converter operate in Discontinuous Conduction Mode (DCM) to minimize conduction losses. The control scheme in both the boost converter and the SIMO consists of a peak inductor current control scheme that ensures constant peak current in the inductor with pulse-frequency-modulation (PFM) control to reduce conduction loss and a zero crossing detector to minimize conduction losses across the diode. The PMU also includes a cold-start circuit with a startup voltage of 220 mV.

A. Boost Converter With MPPT Control

Fig. 6 describes the overall architecture of the boost converter with MPPT control, cold-start circuit, and timing control [8], [14] for conventional high-side (HS) and low-side (LS) switches. Theoretically, TEGs provide maximum power at half of the TEG open circuit voltage, and photovoltaic cells provide maximum power at 76% of the PV open circuit voltage. This ratio is implemented by tuning external off-chip resistors R1 and R2. The MPP circuit stores this voltage (V_{MPP}) at the low pulse of MPP_{clk}, which also disables the boost converter. When MPP_{clk} goes high, the boost converter operates until $V_{IN} < V_{MPP}$, then the boost converter and switching are disabled, allowing V_{IN} to recover. Fig. 7 shows simulation results of the MPP tracking and a timing diagram of the HS and LS control scheme.

The boost control circuit generates three non-overlapping clock phases, φ_1, LS, and HS. The φ_1 pulse width is set by a delay line and is used for offset compensation in the comparators and peak inductor current (I_P) control. The LS pulse width is used for I_P control, and the HS pulse is used to turn off M_{HS} to enable zero detection.

B. SIMO DC-DC Regulator

Fig. 8 shows the buck-boost architecture of the SIMO regulator. Initially the HS switch is closed to load the storage capacitor, V_{CAP}, causing the inductor to charge up and thus ramping up the inductor current (denoted by I_{HS}). After a fixed dead time, the HS is switched off, and the LS switch is turned on

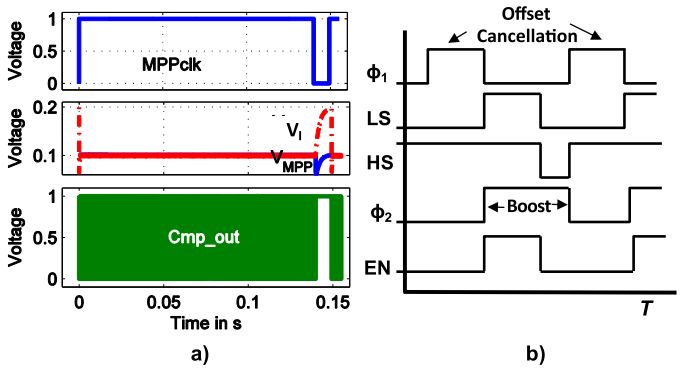

Fig. 7. MPPT operation and boost converter control scheme [8], [14]. (a) Simulation result of MPP tracking. (b) Boost control Timing Signals.

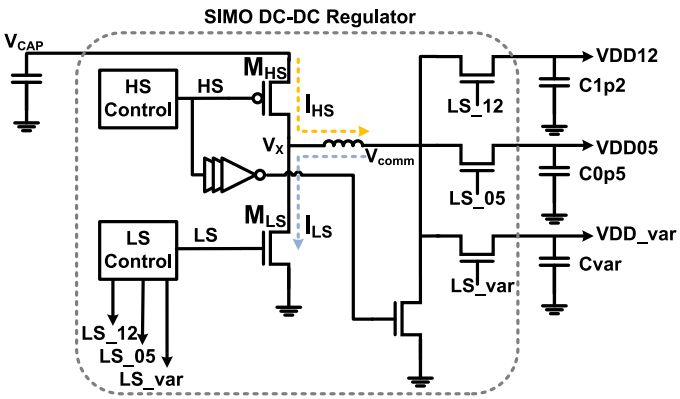

Fig. 8. Block diagram of the power management system.

to transfer the energy (using conduction current I_{LS}) across the inductor to the regulated output rails of 1.2 V (VDD12), 0.5 V (VDD05) and a variable output rail of 0.2–0.35 V (VDD_var).

The output rails (e.g., VDD12) are compared through a feedback network with a reference voltage – V_{ref} – generated by a bandgap reference circuit such as [12]. As long as the fed-back voltage from VDD12 is less than V_{ref}, the peak inductor control circuit is enabled to ramp up the inductor current (I_{HS}) and transfer the power to the output (via I_{LS}) by deploying the LS switch after a fixed dead time. The zero detection comparator monitors node V_x and is enabled as soon as V_x drops below zero.

Fig. 9 shows the peak inductor current control circuit. A constant peak inductor current control scheme is necessary in an inductor based switching regulator for achieving higher efficiency and minimizing conduction losses. A peak inductor current control scheme utilizing the threshold voltage (V_{th}) of a transistor has been described in [13] for a buck converter and in [8], [14] for a boost converter. In this DC-DC regulator, we generate a V_{th}-based peak inductor current control scheme for a buck-boost architecture. The peak current is constant, but the switching frequency is varied to deliver power to varying loads from a fixed input voltage. In Fig. 9(a), we present a bias generation scheme that is invariant to process mismatches and operational at low input voltages for a buck-boost control scheme. The circuit generates a voltage of $V_{CAP}/2+V_{th,p}$ in two stages. In the first stage, $V_{CAP}/2$ is generated using a diode structure, which provides very high impedance and low current. In the

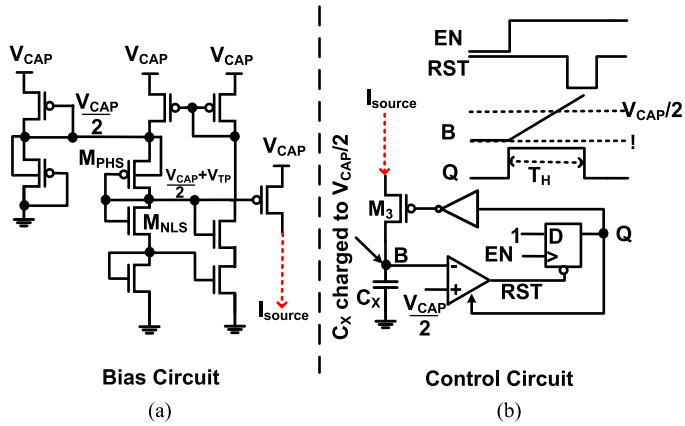

Fig. 9. (a) Bias and (b) control circuits for the peak inductor current control circuits.

next stage, the voltage $V_{CAP}/2 + V_{th,p}$ is generated by dropping this voltage using a PMOS device. The transistor M_{PHS} has a shorter channel length than M_{NLS}. It is critical that the current load from the second stage does not load the first stage to avoid changing the $V_{CAP}/2$ reference. The bias current generated for the next stage is fed back in the feedback loop as shown, which ensures that no current flows from the first stage. The current source provides a current denoted by I_{source} given by

$$I_{source} = k\mu C_{ox}\left(\frac{V_{CAP}}{2} + Vth,p - Vth,p\right)^2$$
$$I_{source} = k\mu C_{ox}\left(\frac{V_{CAP}}{2}\right)^2. \quad (1)$$

The capacitor C_x is charged from 0 to $V_{CAP}/2$ to generate the HS switching time.

$$T_H = \frac{C_X\left(\frac{V_{CAP}}{2}\right)}{I_{source}}$$
$$T_H = \frac{C_X}{k\mu C_{ox}\left(\frac{V_{CAP}}{2}\right)} \quad (2)$$

The peak inductor current is approximately given by

$$I_{PEAK} = \frac{V_{CAP}T_H}{L_{SHR}}.$$

Hence from (2)

$$I_{PEAK} = \frac{2C_X}{k\mu C_{ox}L_{SHR}}. \quad (3)$$

The expression in (3) is independent of input voltage V_{CAP}, the output voltage, or the threshold voltage V_{th} of the transistor. We achieve a constant peak inductor current for a wide input and output range, which is dependent on the gate oxide capacitance, C_{ox}, and the external inductance, L_{SHR}.

For HS control, we present a fast offset compensated zero current detection technique in Fig. 10, which is specifically designed to operate at low input voltages. Zero current detection is

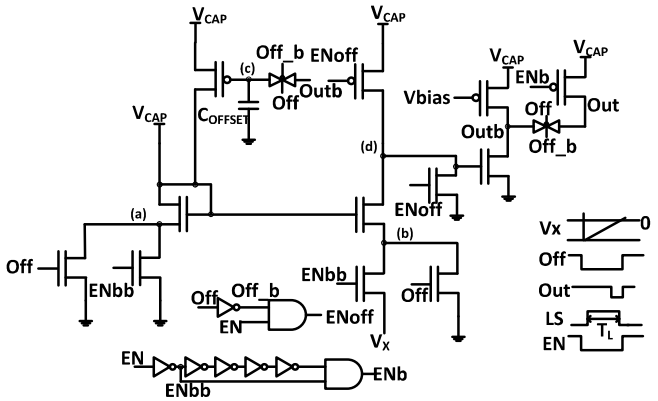

Fig. 10. Zero crossing detection circuit.

needed when the inductor current switches direction so that the regulator can operate in DCM and the power is not delivered across the diode. Hence, zero inductor current crossing detection is needed for achieving higher efficiencies. In this PMU, the zero crossing comparator uses a common-gate amplifier for better performance and is enabled only when the V_x node is pulled below 0 V. The zero detection comparator needs to have a very low input-offset to sense small changes in V_x. Hence offset-compensation is achieved in the first stage with $EN = 1$ and $Off = 1$. When V_x goes below 0 V, the comparator is enabled with $EN = 0$ and $Off = 0$, the LS goes high. As V_x ramps up and crosses 0 V, the comparator output goes low to drive LS low. The comparator is duty-cycled using the EN signal to prevent the higher static current consumed during comparison.

IV. ULP Asymmetric Radio

In order to maintain ULP operation and achieve high data-rate RF communication in many IoT applications, we use an asymmetric RF communication architecture. Fig. 11 shows the proposed architecture and the uplink and downlink signaling for the asymmetric communication.

To lower the power consumption of the transmitter on the SoC, heavily duty-cycled OOK modulation is used, meaning the transmitter (Tx) is only actively on for a very short period of time during a transmission. Thus, the average power can be greatly reduced while still maintaining a valid output power for radiation. To build a low power wakeup receiver (WuRx) a narrowband RF link is chosen, a rectifier is used to replace the power hungry LNA and a bank of 15-bit CDMA codes is used for synchronization [9]. Non-duty cycled OOK modulation is used to lower the power consumption of the wakeup receiver on the SoC and also to simplify the transmitter implementation in the base-station or aggregator communicating with the SoC. Utilizing ULP asymmetric radios for communication between the SoC and the aggregator can bring down the power consumption of the UWB Tx and the WuRx to 4 μW and 116 nW, respectively, enabling the whole SoC to operate on harvested energy.

A. Ultra Wideband (UWB) Uplink

The UWB Tx (Fig. 12) uses OOK modulation with a data rate of 187.5 kbps, chosen to match the data rate of the 802.15.6 WBAN standard. The center frequency is 3.994 GHz with a 500 MHz bandwidth. It consists of a pulse-width generation circuit that uses two separate signal paths with different variable delays to create a short pulse, which is then used to enable/disable a ring oscillator, creating the UWB pulses. To improve the accuracy of the ring oscillator, it can be calibrated open-loop – through current starving – to achieve the 4 GHz range. A Class AB power amplifier buffers the signal onto the antenna. A finite state machine (Tx FSM) controls the data transfer and contains a 2 kB sub-threshold memory buffer that stores the raw data to be transmitted. This data includes any synchronization and preamble headers the base station receiver might need and is written by the LCU or OMSP. The Tx FSM is responsible for clocking the data out of the memory and serializing it before transmission. It also has the option to append a timestamp to the serial data before it is sent. The 4 GHz ring oscillator consists of two parallel 3-stage CMOS-based ring oscillators with the first stage consisting of a NAND gate to allow for the pulse signal to enable and disable the ring's oscillation. Binary weighted current sources on both NMOS and PMOS control the speed and power of the oscillations.

The UWB receiver on the aggregator is shown in Fig. 13. It uses energy detection architecture to directly down convert the RF signal to baseband. A low noise, high gain and high bandwidth gain stage is designed centered at 3.9 GHz. A diode rectifier and a high-speed comparator are used to down-convert and digitize the received packets. A Spartan-6 FPGA is used for the baseband processing, and an IOIO-OTG is used to enable a top-level control through an Android phone with a customized user interface. To synchronize the incoming packets, the highly duty-cycled analog signal is latched to a fraction of one bit length to compensate for the variation of the center frequency in the free run ring oscillator of the transmitter, and suppress noise and interference from different SoCs. The receiver is synchronized when comparing the latched signal at some specific timing slots with the pre-stored preamble code through a programmable threshold. Once the threshold is exceeded, the receiver will start storing data for further processing, as illustrated in Fig. 11.

B. Narrowband Downlink

The CDMA WuRx [9] has four separate interrupt outputs, two hardcoded to each of the OMSP and LCU, and the other two programmable outputs. Each interrupt is triggered by a unique 15-bit OOK modulated Kasami code. In order to operate in the nW range, a high-sensitivity, passive RF rectifier is used to replace the power hungry LNA. The rectifier must receive a selectable 15-bit OOK modulated CDMA code and implement automatic threshold feedback to prevent false wakeups, detect interference and adjust the receiver sensitivity.

From the antenna and band-select filter, the RF signal passes through an off-chip 2-element passive matching network that boosts the signal in 5 dB before going into the rectifier. A 30-stage rectifier working in the sub-threshold region is used to directly down convert the RF signal to baseband [18]. Zero threshold transistors and 30 stages are chosen to achieve sufficient RF gain with fast charge time. The comparator is clocked by the on-chip reference and applies regenerative feedback. The threshold of the comparator is controlled in a feedback

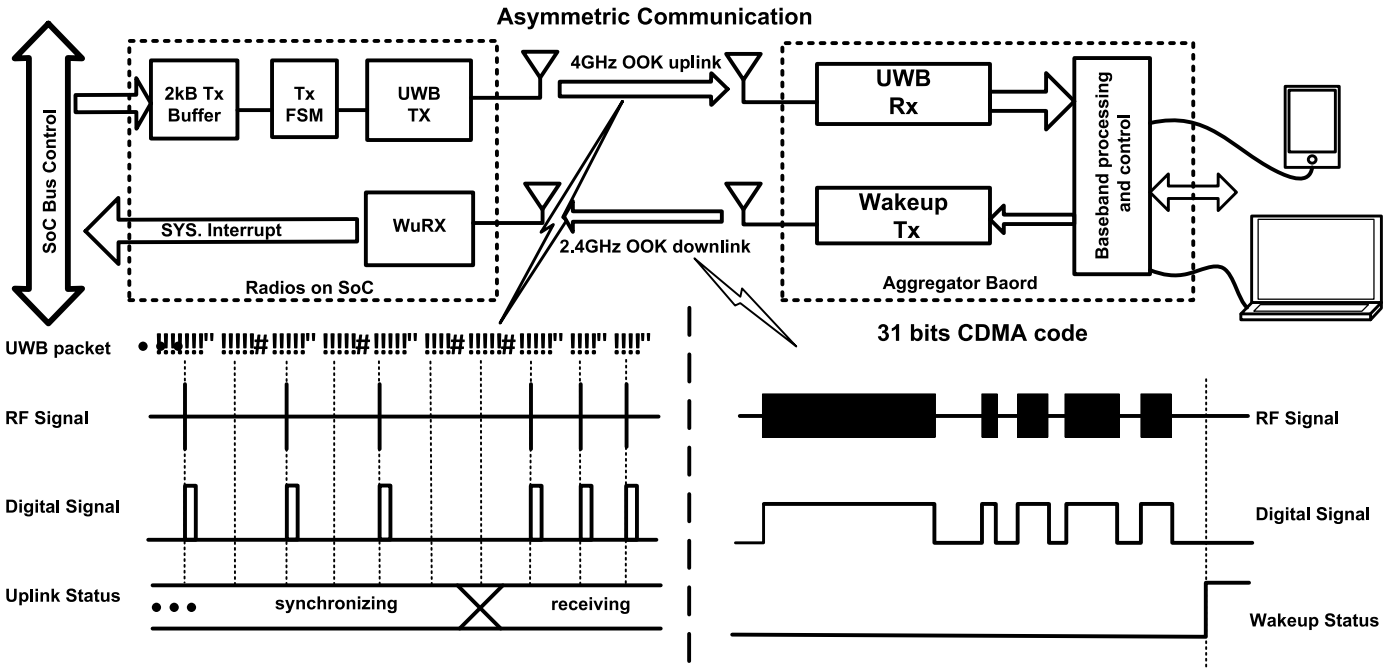

Fig. 11. Architecture of asymmetric radios and signaling.

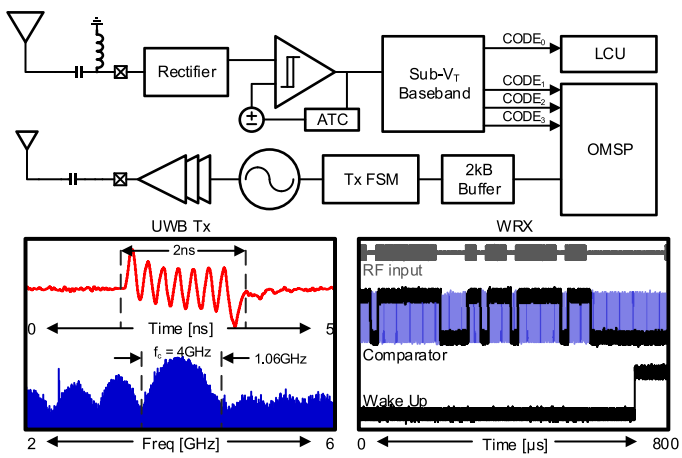

Fig. 12. Architecture of the transceiver in sensor node SoC [16].

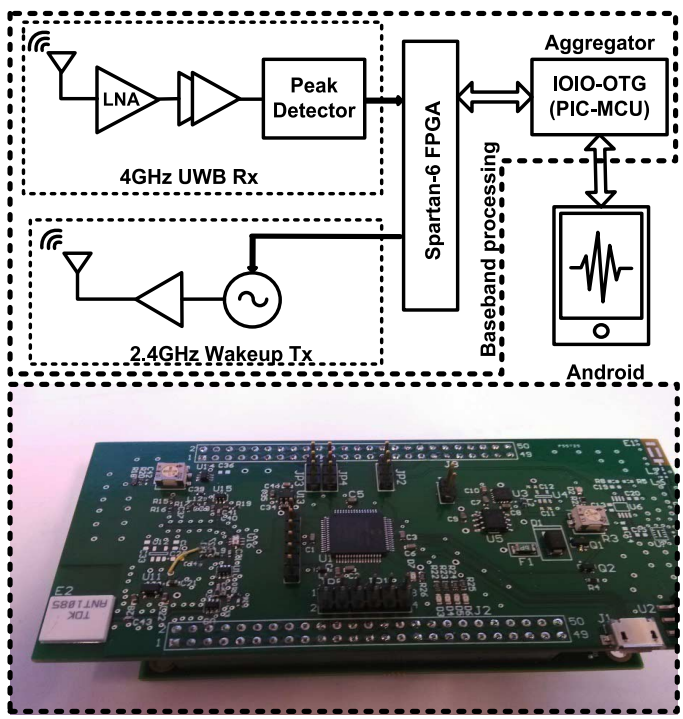

Fig. 13. The aggregator architecture.

loop with a programmable 4-bit binary weighted code by the Automatic Threshold Control (ATC), which dynamically changes the comparator's offset voltage to overcome interference signals [9]. As the RF input signal comes in, the RF rectifier outputs the signal to the comparator. Since the WuRx is gain-limited, as the ATC reduces the comparator's offset, a smaller output from the rectifier will trip the comparator resulting in higher sensitivity.

The comparator compares the output of the rectifier with its threshold. The ATC monitors the samples coming from the comparator output for one 15-bit code period. If the number of 1's is greater than a user defined value (value1), then the ATC will increase the comparator threshold to bring the sensitivity of the receiver above that of the interfering signal. When the number of 0's at the output of the comparator reaches a separate, user defined value (value2), the ATC then reduces the threshold to increase the sensitivity of the receiver. With this mechanism, the comparator can reject interference signals. To synchronize the transmitted code and issue a wakeup, a bank of four correlators continuously correlates the 4 ×-oversampled comparator bit-stream with a programmable, 15-bit CDMA code. The baseband processor is synthesized in sub-threshold in order to save power. The correlator compares the last two samples in each bit slice. Therefore, each 15-bit code results in a total of 30 comparisons. A programmable correlator threshold allows the user to define a value between 1 and 29 that must be exceeded

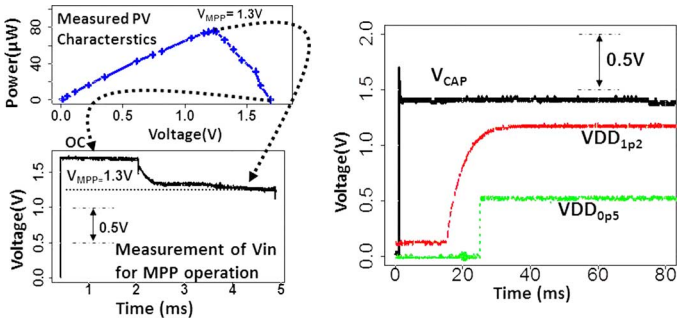

Fig. 14. Measured MPP operation and start-up from harvested PV energy [16].

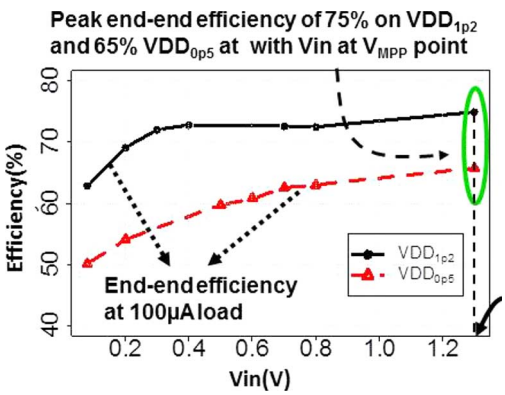

Fig. 15. Measured end-to-end efficiency of the 1.2 V and 0.5 V rails [16].

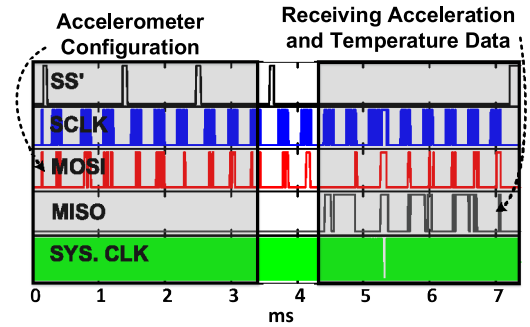

Fig. 16. SPI accelerometer data exchange [16].

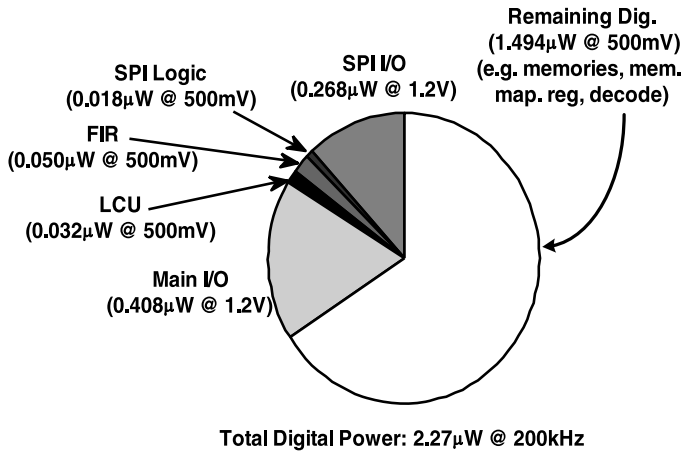

Fig. 17. Digital power breakdown [16].

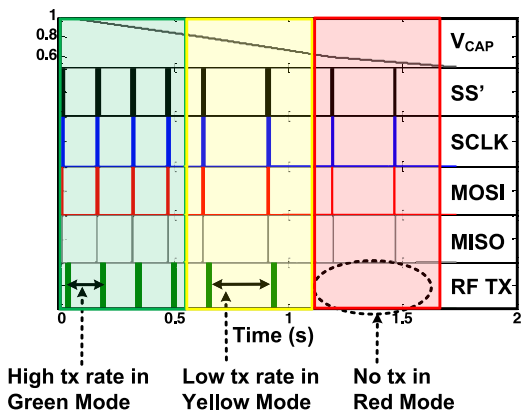

Fig. 18. DPM operating modes.

in order to declare a code received indicating a valid wake-up event. Since the receiver is 4 $\times$-oversampled, four correlators operate at the same time and each correlator receives shifted samples of each bit slice. In each correlator, all possible shifts of the 15-bit Gold code are simultaneously correlated with the incoming bit stream, so that after a single 15-bit sequence, the receiver is guaranteed to synchronize to the wake-up signal. If any of the four correlator's results is greater than the correlator threshold, the wake-up signal will be asserted.

A 2.4 GHz oscillator directly modulates the CDMA code from the wakeup transmitter in the aggregator whenever it is enabled by the code and interrupts from an Android phone.

V. Measurement Results

A. Energy Harvesting and Power Management

To demonstrate MPPT operation and system startup, we used a commercial PV solar cell. We characterized the solar cell under indoor light conditions and measured the open circuit voltage to be around 1.7 V. Fig. 14 shows that the PV cell provided maximum power at an output voltage of 1.3 V. It was observed from measurements that the boost converter enabled the MPPT loop to tune the input impedance of the boost converter so that the PV cell is loaded to operate at its maximum power point. After the harvested energy is stored on the storage capacitor, the SIMO regulator cold-starts and provides regulated 1.2 V and 0.5 V supply to the SoC.

Fig. 15 shows the measured end-to-end efficiency of the energy harvesting and power management system, which harvests energy from indoor PV cell and supplies 1.2 V and 0.5 V regulated outputs at 100 μA load current. The overall PMU achieves a peak efficiency of 75% at 1.2 V output and 65% at 0.5 V output with the boost converter harvesting energy from the PV cell at its maximum power point. The regulator achieves higher efficiency than [5] owing to its peak inductor current control scheme, which allows minimal variation in peak inductor current with input power and output load to reduce the conduction loss.

B. Motion Capture Application With Accelerometer

The chip was tested end-to-end for motion capture with an ADXL362Z accelerometer while powered from indoor solar by the PMU. The SPI on the chip is used to communicate with the

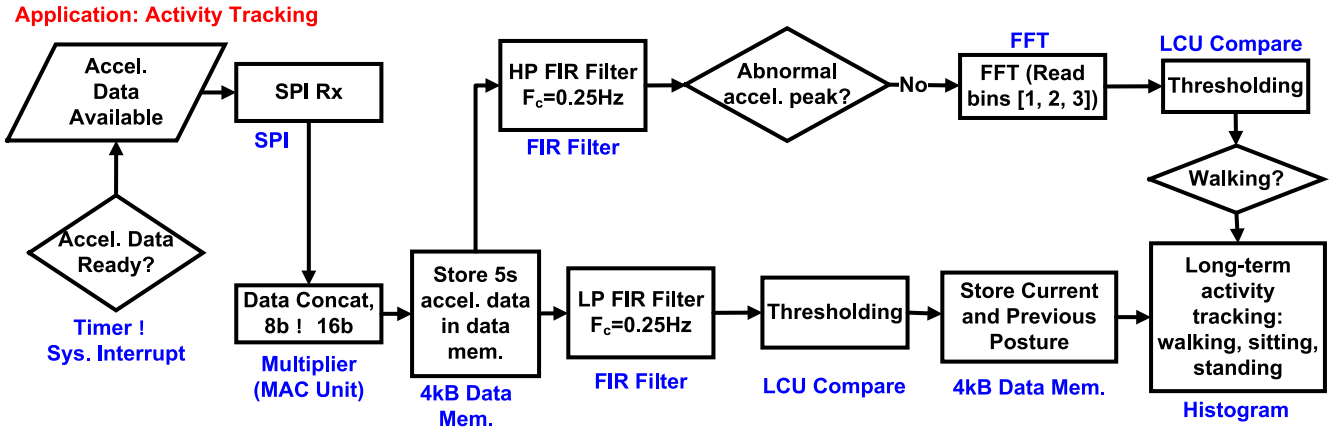

Fig. 19. Activity tracking using the proposed SoC.

accelerometer as shown in Fig. 16. Every two bytes of data received through SPI are concatenated and filtered before being transmitted over the radio. Configuration bytes are first sent to the ADXL362Z before acceleration data can be received. The ADXL362Z then sends two bytes of acceleration data that are concatenated within the multiplier block then the result is fed to the FIR filter for DC filtering. Finally, the output of the FIR filter is transmitted over the radio to an aggregator. The chip consumes 6.45 μW while streaming the raw motion data wirelessly over UWB. Fig. 17 shows the breakdown of power among the different blocks.

C. Stop Light Operation Using DPM

The DPM can be programmed to monitor the voltage on the capacitor and power or clock gate different blocks to make sure that critical data is not lost. Fig. 18 shows the three modes of operation of the DPM. In this example, the ADC is used to measure that voltage while data is being received on the SPI interface. When V_{CAP} is above the green threshold, the accelerator blocks are operational and data can be transmitted at the required rate. When V_{CAP} drops below the yellow threshold (0.8 V in this example), the accelerator blocks are power gated and the frequency of transmission is reduced. In this case only critical data is transmitted over the radio. When V_{CAP} drops below the critical red threshold (0.6 V in this example), the RF, data memory and all accelerator blocks are power gated while the instruction memories are clock gated to reduce the current drawn from the capacitor.

D. System Flexibility

Due to the flexible data path capabilities and the many accelerators available, the SoC can easily support a number of applications. The AFE interface and the RR-AFIB blocks can be used for heart rate monitoring and AFIB detection as was previously demonstrated in [5]. The SPI interface can be used to communicate with different sensors such as the ADXL362Z to gather accelerometer and temperature data. The different on-chip hardware accelerators can then be used to implement fall detection, activity monitoring, motion artifact removal and other algorithms. Fig. 19 shows activity tracking as an example algorithm that can be implemented on the SoC, and the different hardware accelerators used in each step of the algorithm. In this application, the SoC can detect whether the user is standing, walking, or sitting based on accelerometer data gathered over 5 s intervals using the LCU, multiplier, FIR, FFT and timer blocks. This information can then be fed into the histogram block for long-term activity tracking.

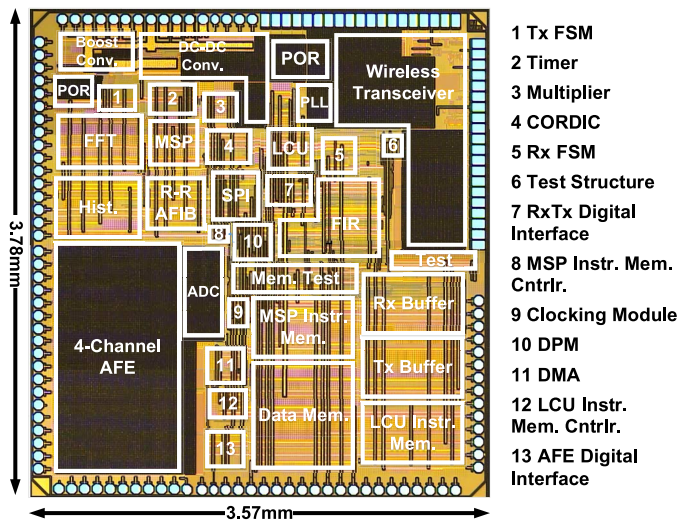

Fig. 20. Table of comparison and chip micrograph.

E. Summary

Fig. 20 shows the chip micrograph detailing the different blocks. Table I compares the proposed SoC with the state-of-the-art. This SoC has the largest suite of accelerators targeting wearable and IoT applications. The integrated PMU is capable of boosting from a low input voltage of 10 mV and achieves the highest end-to-end efficiency (75%). The asymmetric RF transceiver allows the chip to transmit important data while only consuming 4.18 μW and to receive wake-up signals while consuming only 161 pJ/bit.

VI. Conclusion

To date, this SoC has the highest level of integration of a wearable wireless sensor IC, including energy harvesting and a full transceiver, for the lowest power. This chip also has the highest energy harvesting/regulation efficiency and achieves

TABLE I
COMPARISON BETWEEN THE PROPOSED WORK AND THE STATE-OF-THE-ART

		This Work	ISSCC '14 [4]	JSSC '13 [5]	ISSCC '14 [7]
	Sensor Interfaces	Analog (ECG, EEG, EMG), Digital (SPI)	Analog(ECG, bioimpedence) Digital (SPI, I2C, UART)	Analog (ECG, EMG, EEG)	Analog (ECG)
Digital	MCU	MSP430	ARM Cortex M0	8-bit PIC	ARM Cortex M0
	Peripherals	DMA,FIR,FFT,CORDIC, Timer, Histogram, Multiplier, R-R AFIB	DMA, Matrix-Multiply-Accumulate	DMA FIFO, FIR, Envelope Detector, R-R AFIB	FIR, FFT
	On-Chip Memory	12 kB (0.35V-0.7V)	128 KB	5.5 kB	3.7 kB
	DVS	Y	N	Y	N
	DPM	Y	N	Y	N
	Flexible Clocking	ADPLL (187.5 to 500kHz with /1/2/4/8)	MCU Clock (1-20 MHz)	200 kHz (with /1/2/4)	10 kHz
	Digital Power	2.27 µW	120 µW	2.1 µW	45 nW
PMU	Integrated PMU	Y	N	Y	N
	Energy Harvesting	Solar, TEG	-	TEG	-
	End-End PMU Eff.	74.9%	-	38%	-
	Regulated Output	1.2V,0.5V,Variable	-	1.2V,1V,0.5 V (2)	-
	SIMO Regulation	Y	-	N	-
	Boost Voltage	10 mV	-	30 mV	-
AFE	ADC Resolution	8	13.5	8	8
	ADC Sample Freq	128/256 Hz	500 Hz	128/256 Hz	500 Hz
	AFE Channels	4	3	4	1
Radios	Integrated Tx/Rx	Y	N	N	N
	Tx Band	2400MHz-2480 MHz (3.99 GHz center)	-	402 / 433 MHz	-
	Tx Data Rate	187.5 kbps	-	200 kbps	-
	Tx Output Power	-28.9 dBm	-	-18.5 dBm	-
	Tx Power	4.18 µW	-	160 µW	-
	Rx Center Frequency	400-2400 MHz	-	-	-
	Rx Data Rate	7.8125 kbps	-	-	-
	Rx Power	112 nW	-	-	-
	WuRx Energy	161 pJ/bit	-	-	-
	Technology	130 nm	180 nm	130nm	65 nm
	Die Area	13.49 mm^2	49.00 mm^2	8.25 mm^2	3.32 mm^2
	Max. Voltage	1.4 V	1.2 V	1.2 V	0.6 V

lower power RF connectivity by 38 ×. The carefully integrated ULP components on this SoC support numerous wearable physiological sensing and IoT applications on a self-powered platform.

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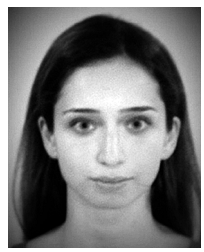

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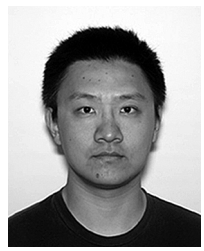

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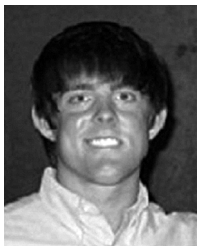

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