A 50nW, 100kbps Clock/Data Recovery Circuit in an FSK RF Receiver on a Body Sensor Node

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26th International Conference on VLSI
January 2013
Pune,India

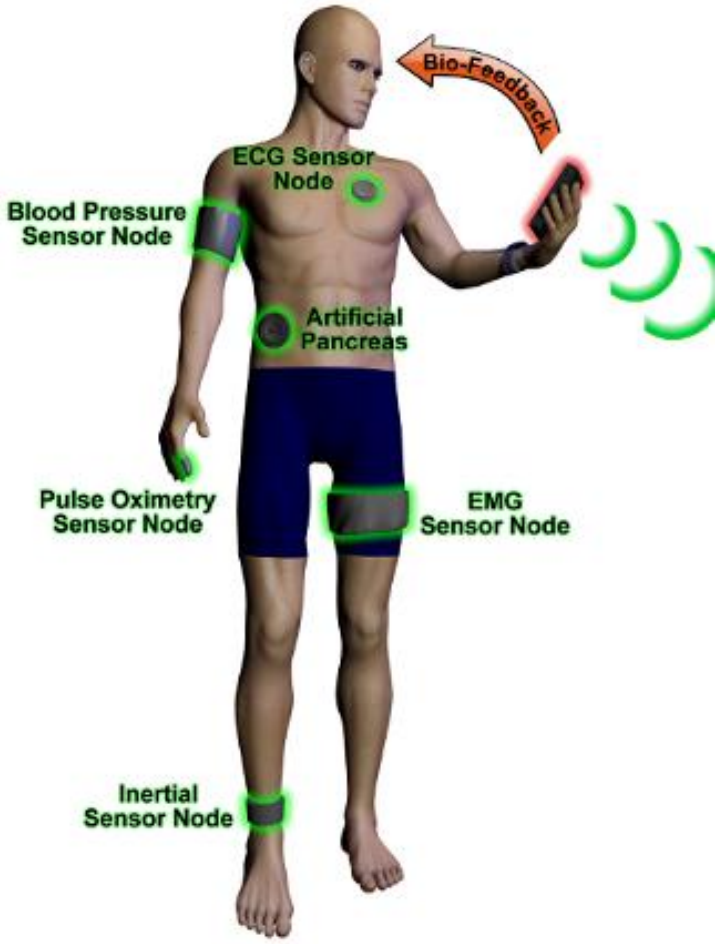
Body Sensor Node (BSN)

Features

- BSNs promise to change the way we experience life
- Comprehensive and unobtrusive human health monitoring.

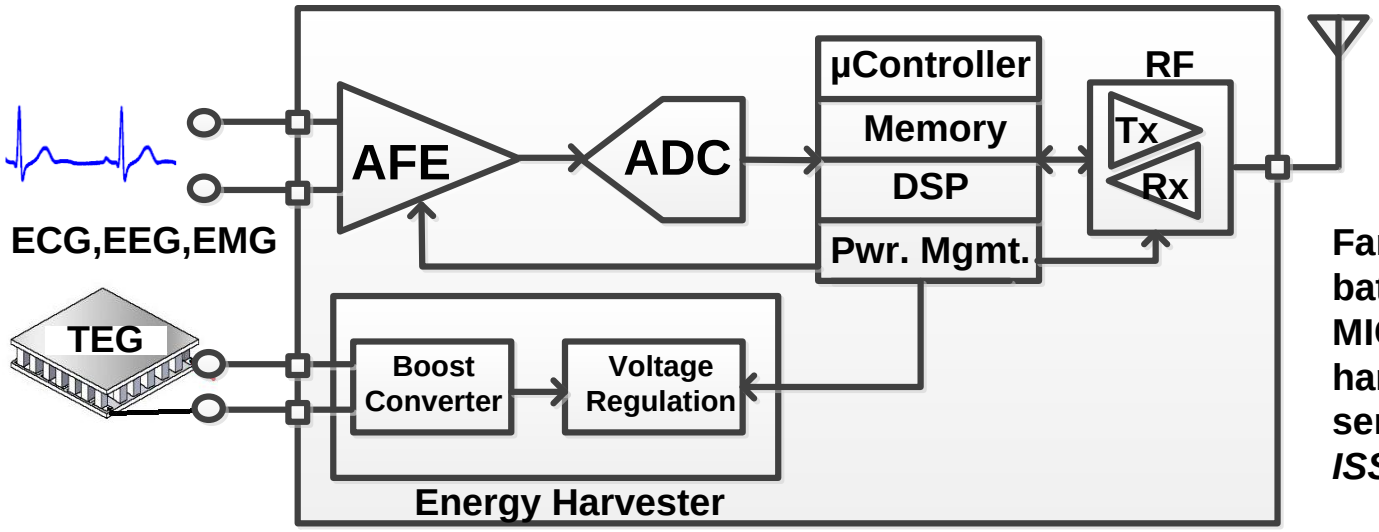
Needs

- Small Form Factor, light wait
- Runs on harvested energy (Body heat)
- Low cost.
- **Ultra Low Power**



Ex :- Fan Zhang et al. ”A batteryless 19μW MICS/ISM-band energy harvesting body area sensor node SoC.” *ISSCC 2012*

BSN



Energy Harvesting BSN Soc [1]

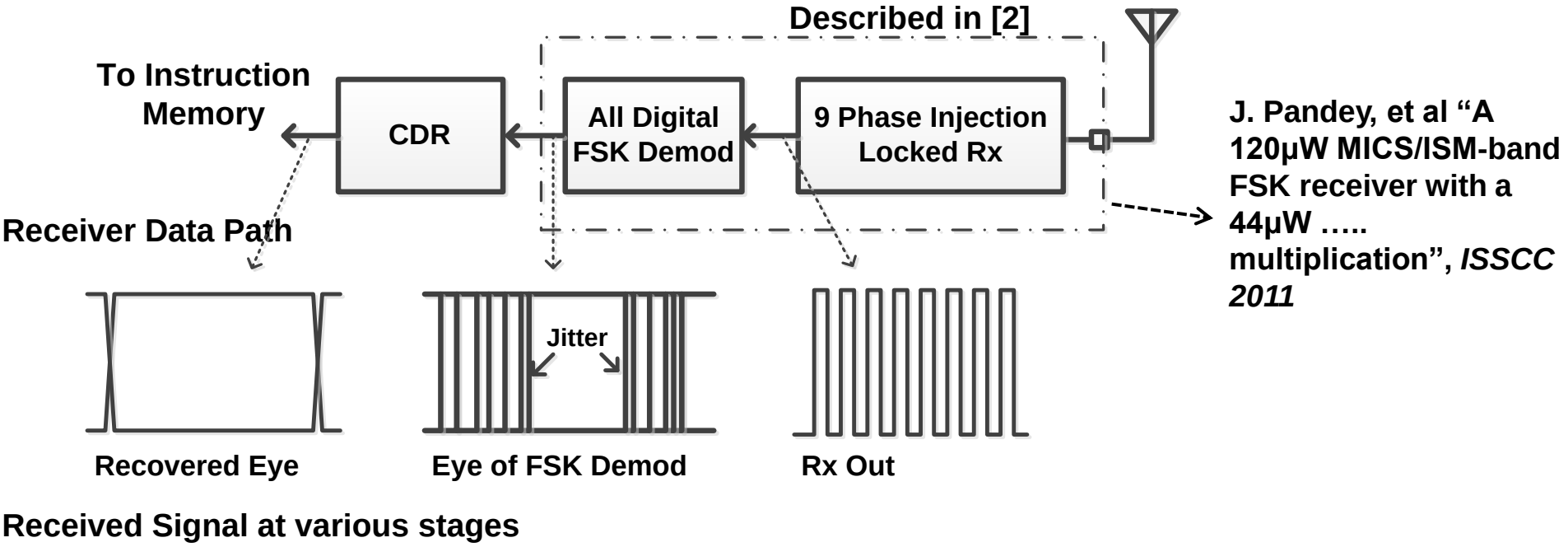
Fan Zhang et al. "A batteryless 19µW MICS/ISM-band energy harvesting body area sensor node SoC." *ISSCC 2012*

- Harvests Energy using TEG from body Heat
- AFE, ADC, DSP, etc. performs sensing
- RF Rx, Tx used for communication.
- Average power consumption 19µW.
- **In this paper we talk about CDR circuit in the RF receiver**

Outline

- **BSN RF Receiver**
  - CDR Requirements
- **Clock Recovery**
- **Data Recovery**
  - Phase Detection
  - Timing
  - Sensitivity
  - Control
- **Limitations**
- **Measurement**
- **Comparison**
- **References**

BSN RF Receiver

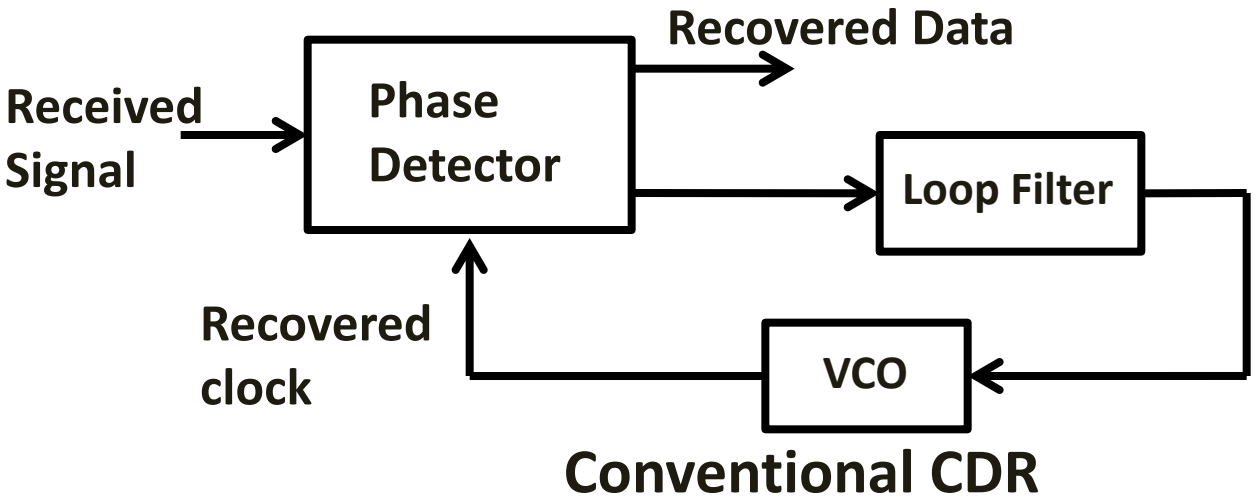


- [2] shows 9 phase injection locked Rx and all digital FSK Demod.
- It does not show CDR, needed to recover Data for DSP
- **In this paper we talk about CDR circuit in the RF receiver**

CDR Requirements for BSN

- Conventional approach in designing CDR usually involves a design of PLLs or DLLs
- These solutions are too expensive in terms of area and power for a BSN. Ex:- [4] uses PLL with 110µW Power >> our SoC Power of 19µW.
- All digital FSK Demod is used in [2] to save power
- A low power, lower cost and lower area CDR circuit is needed for BSN

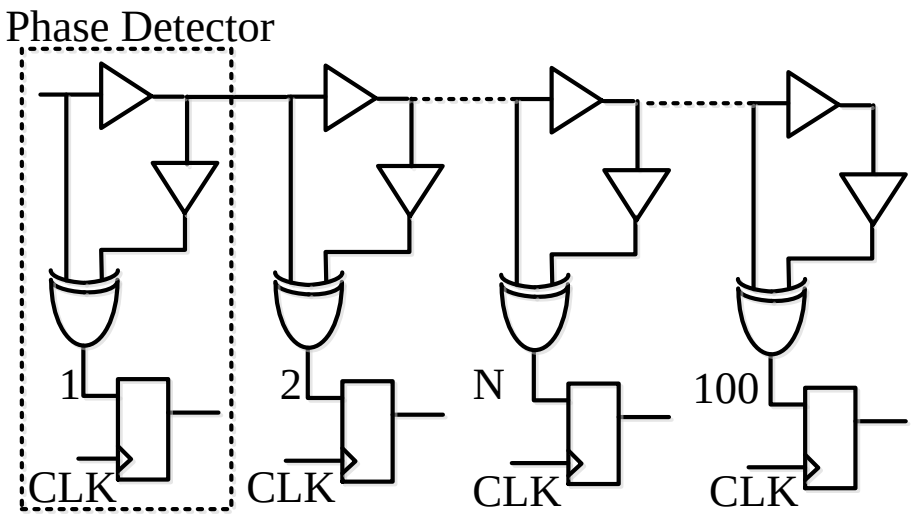
Clock Recovery

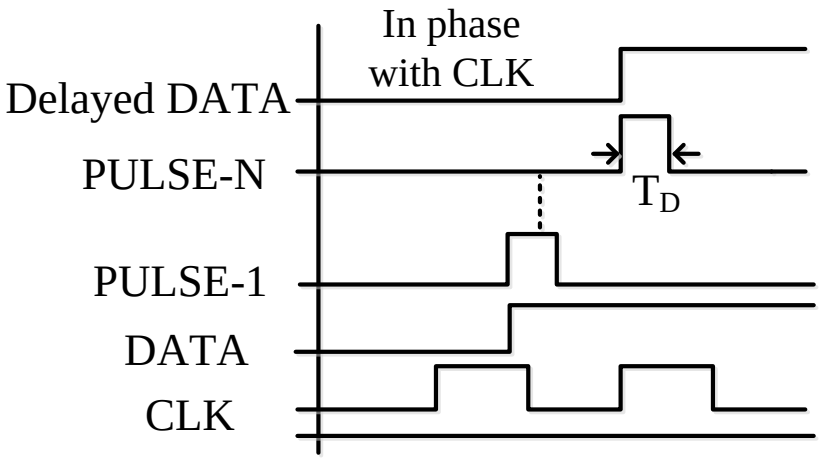


Conventional CDR

- Conventionally CLk is recovered from signal, uses PLL
- In our BSN, Data at 100kB/s, 200khz XTAL for Tx
- Also SoC clock for DSP 200khz from XTAL.
- **SoC clock is used to recover data, eliminating a PLL.**

Data Recovery →Phase Detection



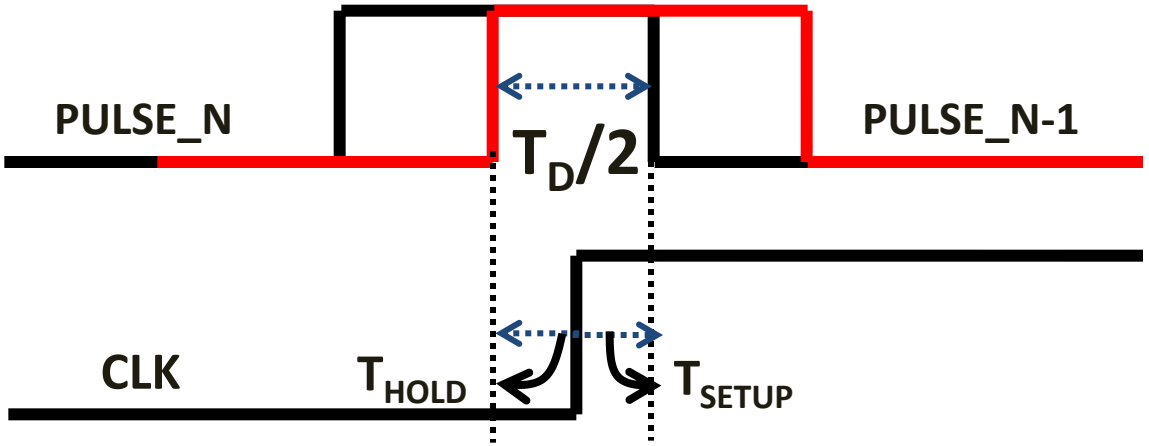


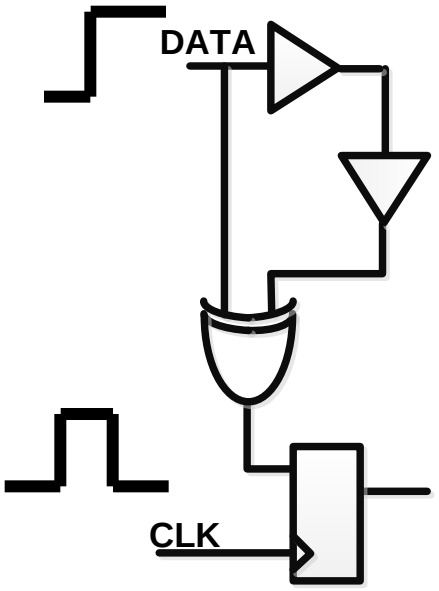
- Pulse generated at each point in delay line.
- Feeds to D-Flip Flop (DFF) clocked at 200 kHz.

- **The pulse close to the edge of the clock will be caught by FF. Point indicating data in phase with clock**

- A number of these phase detectors are placed in series

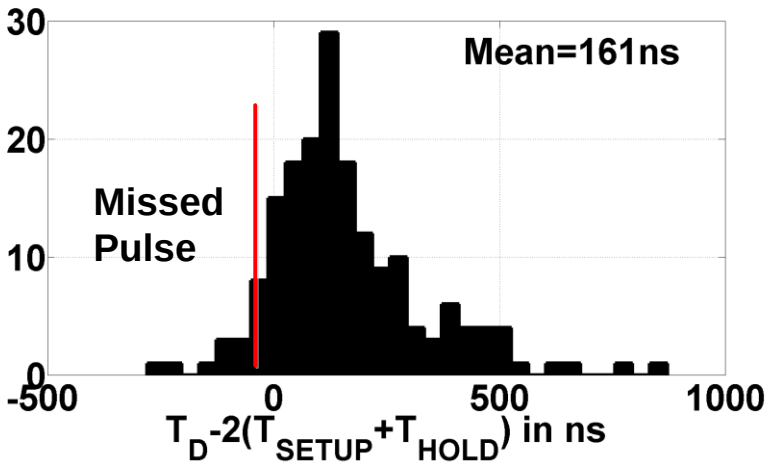
Timing requirement





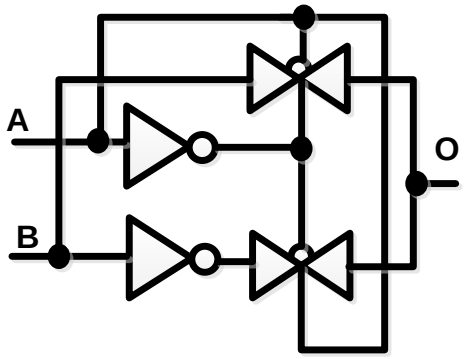
Phase Detector

- To catch at least one of the pulses, pulse width should meet the following criteria
- $T_D/2>(T_{HOLD}+T_{SETUP})$
- **This criteria is met for most of the process points.**

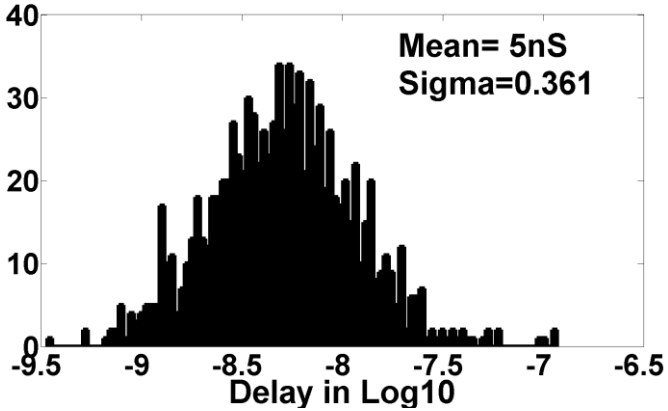


Design Margin

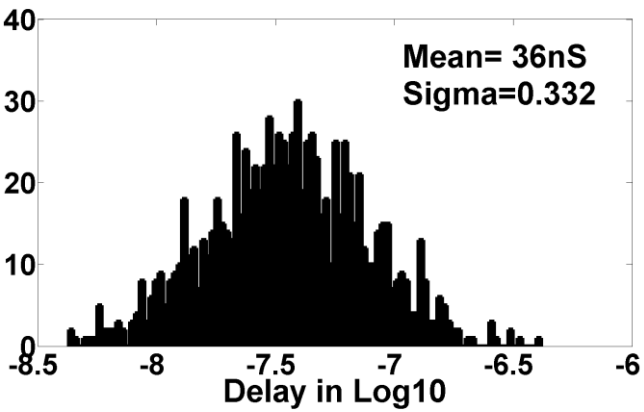
XOR Gate in pulse generator



Transmission gate XOR



Delay of Transmission gate in XOR

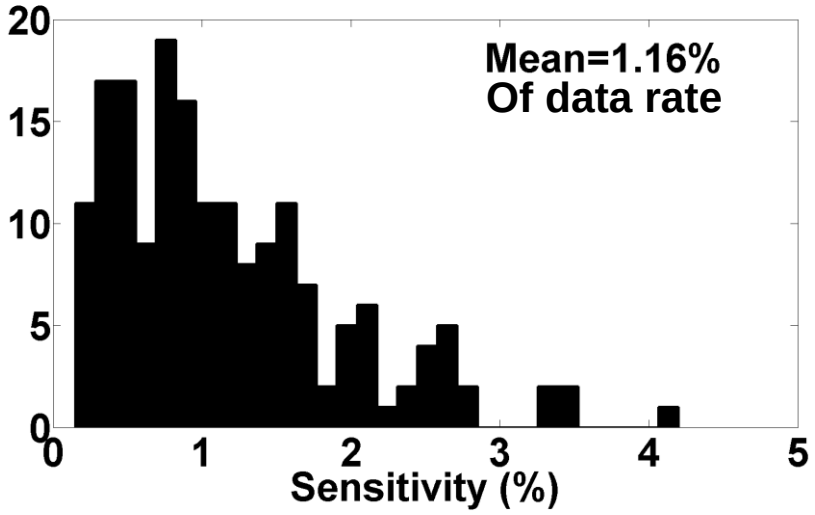


Delay of XOR gate in Std. Cell

XOR gate used in PD

- XOR gate is critical to the performance of the PD, we used a transmission gate XOR
- It has much better performance at 500mV than the standard cell XOR.
- The transmission gate XOR has mean delay of 5ns and an area of 3.6x6.0 μm^2. The standard cell based XOR has a mean delay of 36ns and area of 3.6x8.0 μm^2.

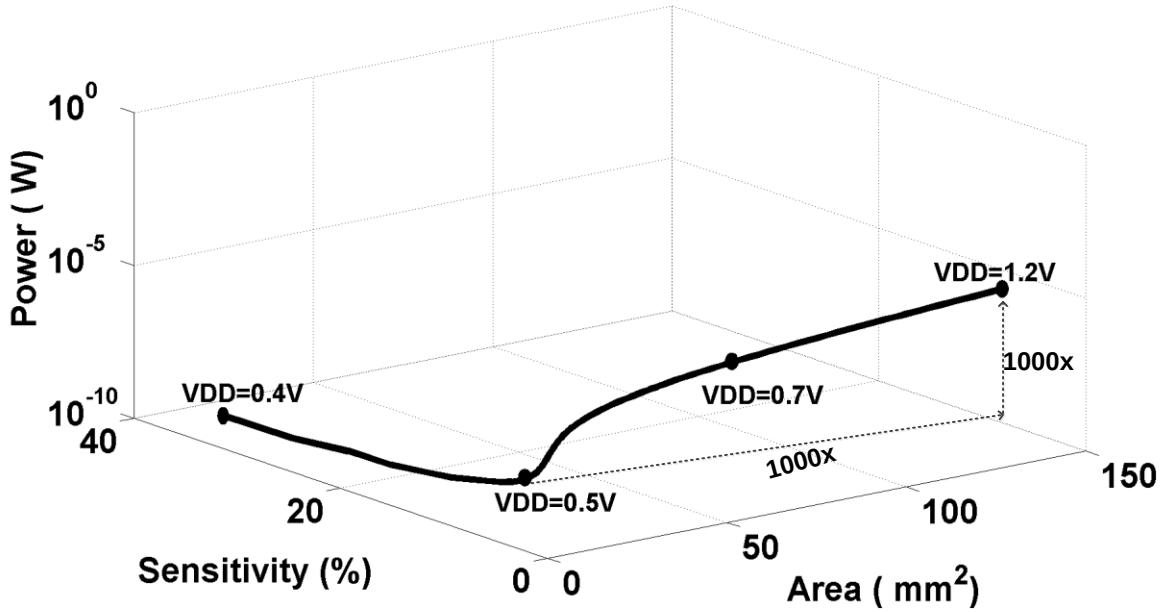
Sensitivity of Phase Detection



Resolution of Delay Line

- One buffer delay sets the sensitivity of the delay line. Lower sensitivity will reduce the amount of input jitter that the CDR circuit can tolerate.
- The mean is close to 1% of the data rate period.
- we used 100 stages in the delay line.

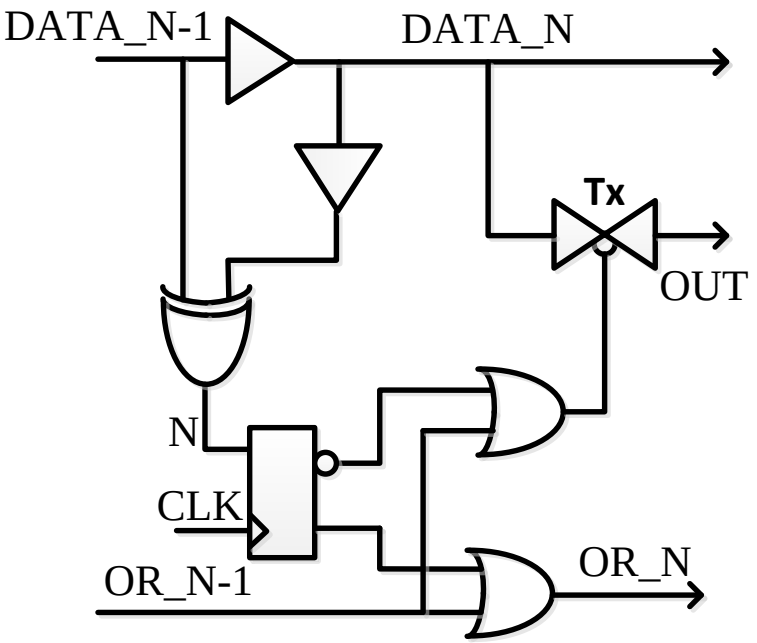
Sensitivity : Design Tradeoff



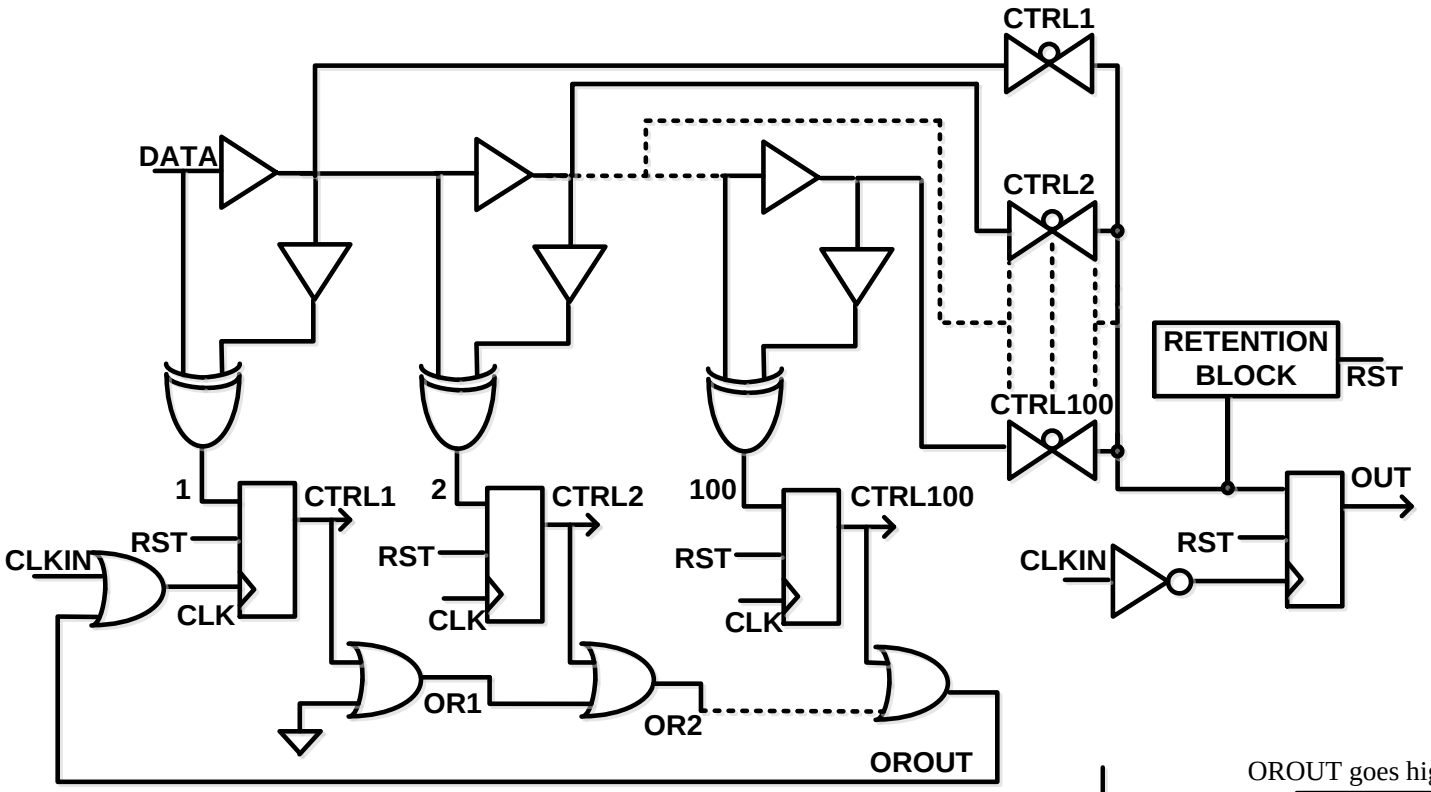
Power, Area and Sensitivity tradeoff

- Increasing VDD decreases delay through the buffer. This improves the sensitivity but increases the area and power.
- VDD~0.5V has 1% sensitivity, 1000X lower area, and 1000X lower power than at 1.2V. The SoC [1] digital VDD is also 0.5V, so it was used for the CDR circuit.

Control Circuit

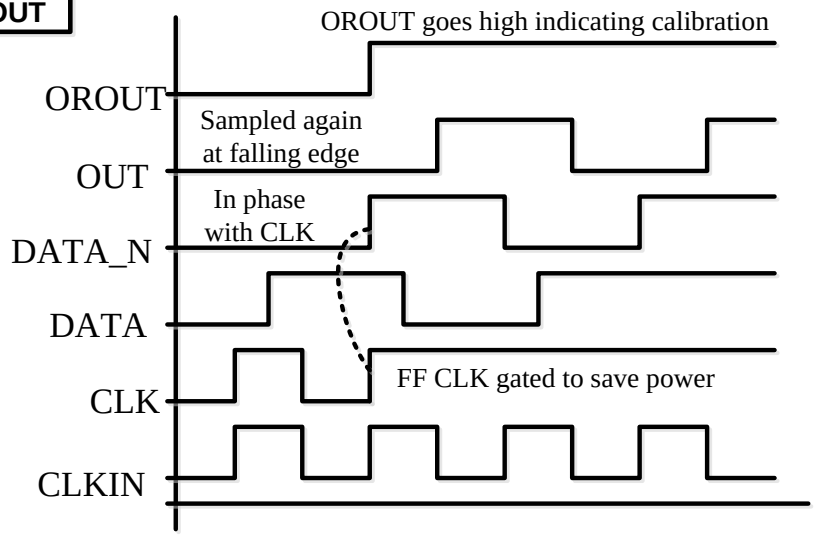


- If OR_N-1=0 and the output of DFF goes high, then the transmission gate Tx turns ON, selecting that output of the delay line.
- **It indicates that data is in phase with lock**



Complete Circuit Diagram

- **Once the data has been brought in phase with clock, the CDR goes into lock for the period of of Tx.**
- **Once a transmission ends, the CDR resets and is now ready for the next transmission.**



Timing Diagram CDR

Limitations of the Design

Clock difference b/w Rx and Tx

- clock recovery is not adapted continually, lowers the BER
- Account for the offset between the Tx and Rx clock frequencies.
- Rx and Tx are generated from Xtal, maximum offset of 50ppm [6] , setting inherent BER of CDR to $5x10^{-5}$.
- This does not significantly degrade the overall BER of the link, which is set by the RX and is 10^{-3} [2].
- **This also illustrates that explicit clock recovery is not needed in this case**

Limitations of the Design

Process variation of total Delay of the delay line

- A second limitation is that the total delay of the delay line should be greater than 5µs for this circuit to work correctly.

- Since the delay in sub-threshold varies exponentially with process variation, the spread of the total delay will be very large.

- We can compensate variation by lengthening the delay line or by reducing VDD slightly.

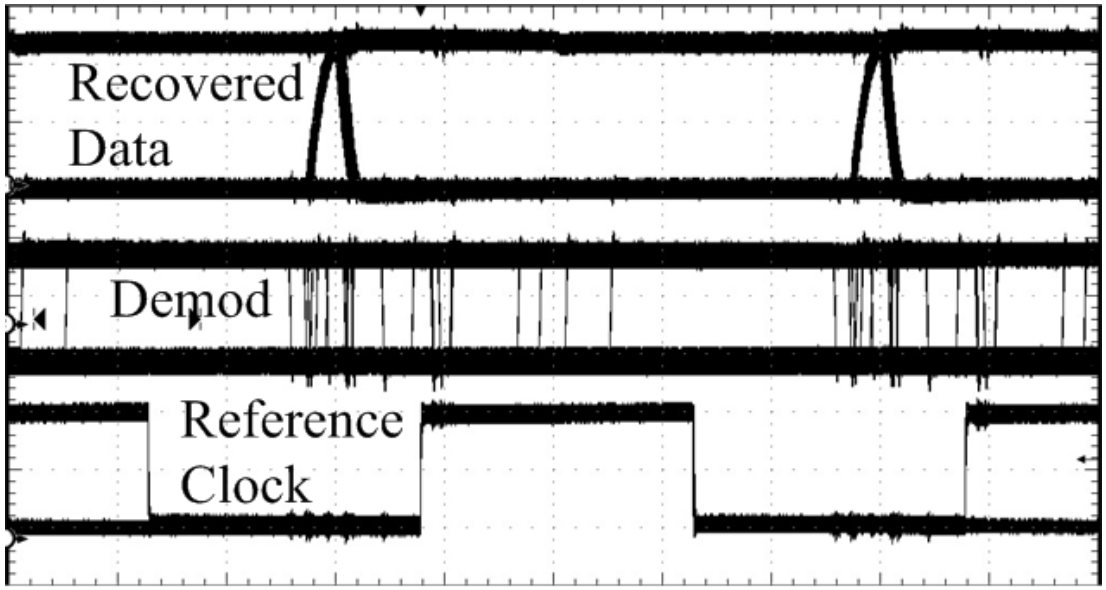
Limitations of the Design

Metastability

- It is also possible that the DFF in one of the phase detectors can enter a meta-stable state during calibration, increasing power consumption briefly.

- However, this probability is very low due to noise (thermal, flicker etc.) and the 2.5µs hold period.

Measurement



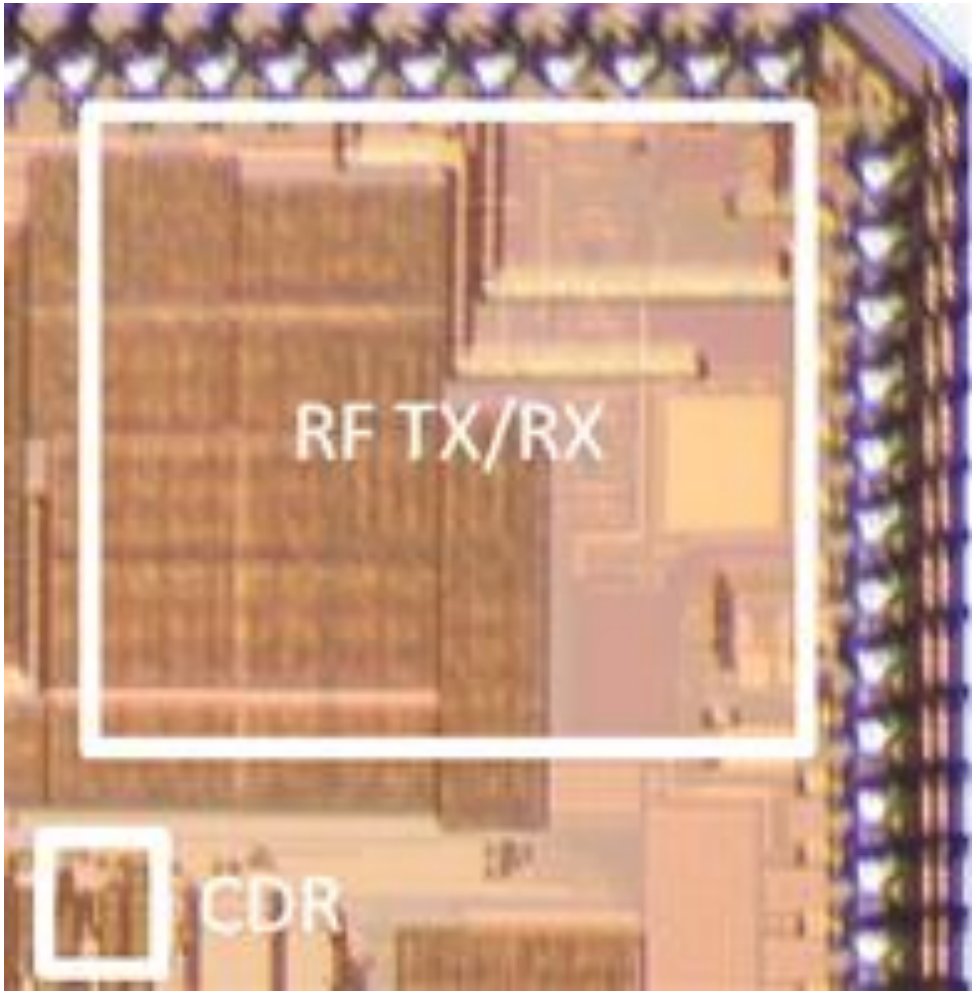
- In the measurement test we measured eye diagram of the FSK demod out and the CDR data out for a 2^7-1 pseudo random data sequence running through the RX at a data rate of 100 kbps.
- The FSK demod output has a jitter of ~2µs, while the data recovery circuit recovers the data with a jitter of 16ns.

Design Comparison

	[3]	[4]	[5]	This Work
Technology	90nm	0.25µm	0.18µm	0.13µm
Data Rate	200kb/s	2Mb/s	10Mb/s	100kb/s
Acquisition Time	54µs	45µs	-	2.5µs
Power (CDR)	217nW	112µW	8.05µW	**50nW**
Energy/bit	1pJ	56pJ	0.8pJ	**0.5pJ**
Area (mm^2)	0.035	-	0.09	**0.017**

Design Comparison

Chip



Conclusion

- **We presented a low power CDR circuit for a wireless body sensor node.**
- **It consumes 50nW at 100kbps or 0.4pJ/bit.**
- **Recovers data from FSK demod of the receiver with upto 2µs jitter. It locks over 18X faster than prior art.**
- **The proposed circuit is fabricated in a 0.13µm CMOS technology. It can recover data with an input jitter of up to 2.4µs with >2X less power and >2X less area than prior work.**
- **The proposed circuit is completely implemented using digital gates and can easily be synthesizable.**

Acknowledgement

This work was supported in part by the NSF NERC ASSIST center (EEC-1160483)

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