A 50nW, 100kbps Clock/Data Recovery Circuit in an FSK RF Receiver on a Body Sensor Node

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***Abstract*-This paper presents a low power clock and data recovery (CDR) circuit for a wireless body sensor node. The proposed circuit interfaces the RF receiver output with the digital processing. It consumes 50nW at 100kbps. It uses a delay locked loop (DLL) that is calibrated in one-shot fashion to save power, locking over 18X faster than prior art. The proposed circuit is fabricated in a 0.13µm CMOS technology. It recovers data with an input jitter of up to 2.4µs with >2X less power and >2X less area than prior work. The proposed circuit is a synthesizable all digital implementation**.

I. INTRODUCTION

Body Sensor Nodes (BSNs) promise to change the way we experience life by providing rich information about our activities, health, and environment. These miniaturized nodes are responsible for sensing data periodically, processing it, and communicating information wirelessly. Since these devices require small size and long lifetimes, they must operate at very low power levels. The power needed for wireless communication usually dominates a BSN's total power. RF transceivers used in BSNs undergo considerable performance degradation to meet power goals. Therefore, obtaining a fully-integrated low power end-to-end BSN SoC remains a challenge. The CDR circuit is critical to achieving a low BER for a BSN receiver. In this paper we present an ultra-low power CDR circuit that is used in our BSN SoC [1] that runs without a battery using harvested energy, which makes low power design essential. Fig. 1 shows the block diagram of the SoC that uses a thermo-electric generator (TEG) to harvest energy from body heat. The SoC includes (but [1] does not mention) a 9-phase injection locked RF receiver first reported in [2], which did not include a CDR circuit. An FSK demodulator followed by a CDR circuit is needed to recover sampled data (Fig. 2 and Fig. 3). The conventional approach to designing a CDR or FSK demodulator circuit usually

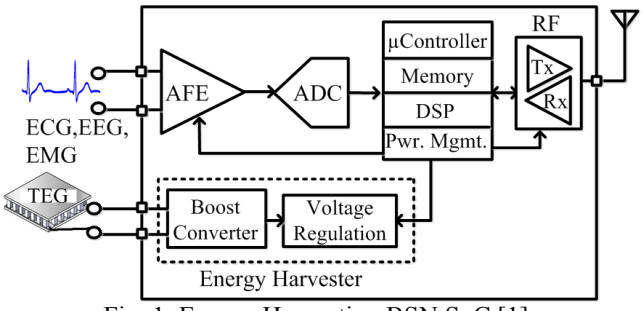

Fig. 1. Energy Harvesting BSN SoC [1]

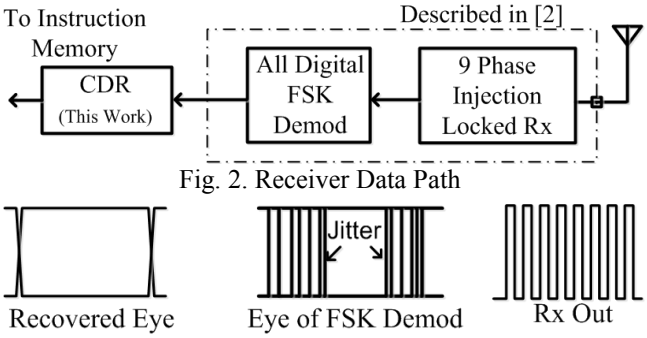

Fig. 2. Receiver Data Path

Fig. 3. Received Signal at Various Stages

involves a phase locked loop (PLL) or delay locked loop (DLL) that is too costly in area and power for energy harvesting BSN applications. The design of a low power CDR for BSN is an ongoing effort [3-5]. In [3], 3b4b encoding of data is used to maximize the data transition and achieves a power of 217nW. [4] and [5] use PLL based CDR and have higher power consumption. Our receiver [2] uses an all digital FSK demodulator to save power, and the proposed CDR captures the demodulator output.

II. CLOCK AND DATA RECOVERY CIRCUIT

Our CDR circuit consumes 50nW of power and recovers data from the output of an FSK receiver operating at 100 kbps. The received clock is derived from a 200 kHz crystal oscillator (2µW) that clocks the digital circuits of our BSN chip [1]. This helps us to reuse the existing clock which eliminates the need for a voltage controlled oscillator (VCO). If Rx and Tx clock vary by 50ppm [6], then the channel should be recalibrated every 20k cycles which sets the inherent BER of CDR to $5x10^{-5}$.

A. Phase Detection

Fig. 4 shows our phase detector (PD) circuit. A pulse generator at each delay point in the delay line generates a

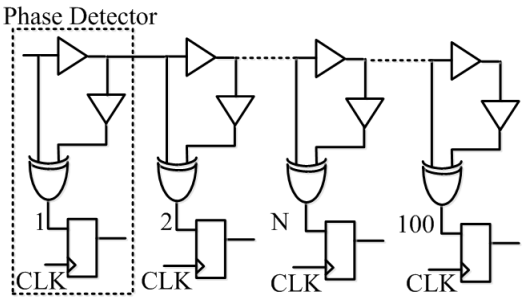

Fig. 4. Delay Line with Phase Detectors

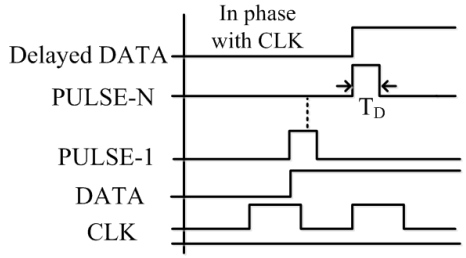

Fig. 5. Timing Diagram and Phase Detection

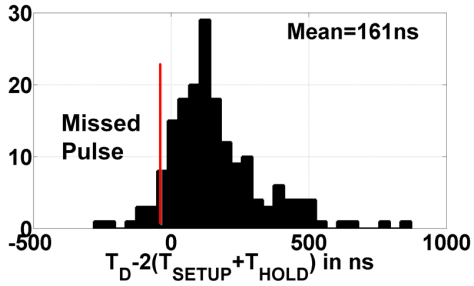

Fig. 6. Design Margin for Pulse Generator

pulse of T_D when data makes a transition. This pulse feeds a D-Flip Flop (DFF) clocked by the oscillator at 200 kHz. If the pulse goes high around the point where clock goes high, the DFF catches the pulse, indicating that data is in-phase with the clock. A number of these phase detectors are placed in series as shown in Fig. 4. Fig. 5 illustrates the concept with an idealized timing diagram. $T_D > 2*(T_{Setup}+T_{Hold})$ is a sufficient condition to ensure that at least one DFF goes high. Fig. 6 shows the histogram of $T_D - 2* (T_{Setup}+T_{Hold})$ obtained from Monte-Carlo simulations. We satisfy this condition for most of the process points. If this condition is not satisfied then none of the pulses in the line is latched for a given edge. The lock can then occur on the next edge of the data. There is sufficient jitter at the input to make the probability of multiple misses insignificant.

B. XOR Gate

The performance of the XOR gate standard cell was very poor at 500mV. Since this circuit is critical to the performance of the PD, we used a transmission gate XOR shown in Fig. 7 with better performance at 500mV than the standard cell XOR. Adding this new cell to the standard cell library enables synthesis of the design. Transmission

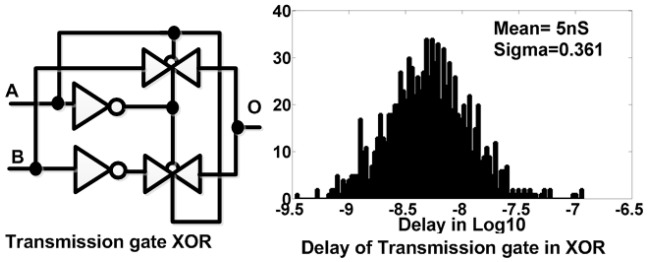

Fig. 7. XOR gate Performance

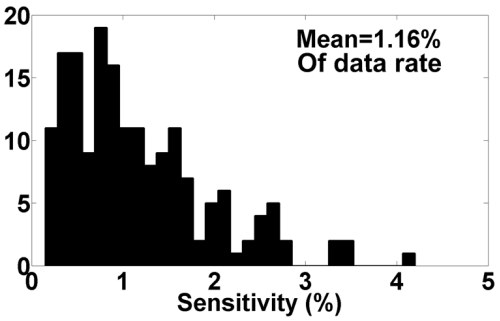

Fig. 8. Sensitivity of the Delay Line

gate XOR has mean delay of 5ns and an area of 3.6x6.0 μm^2. The standard cell based XOR has a mean delay of 36ns and area of 3.6x8.0 μm^2. The transmission gate based XOR gate has better performance than its standard cell counterpart at voltages near threshold because it does not have transistors in cascoded structure. The cascoded structure severely impacts the performance at such voltages.

C. Sensitivity of Phase detection

One buffer delay sets the sensitivity of the delay line. Lower sensitivity will reduce the amount of input jitter that the CDR circuit can tolerate. Fig. 8 shows the histogram of the sensitivity of the PD as the percentage of data rate. The mean is close to 1% of the data rate period. Also, the total delay through the delay line should be greater than the period, for the data to be captured by the clock. So we used 100 stages in the delay line. Power and area also affect the choice of stages. Increasing V_{DD} decreases delay through the buffer. This improves the sensitivity but increases the area and power as more stages are needed. Fig. 9 shows the sensitivity, power, and area tradeoff. V_{DD}~0.5V has 1% sensitivity, 1000X lower area, and 1000X lower power than at 1.2V. The SoC [1] digital V_{DD} is also 0.5V, so it was used for the CDR circuit.

The point on the delay line where the DFF output goes high indicates the required delay in the data to bring it in phase with the clock. Monitoring these points over a few cycles can let us choose the correct point in the delay line to calibrate the sampling instant, much like a DLL. However,

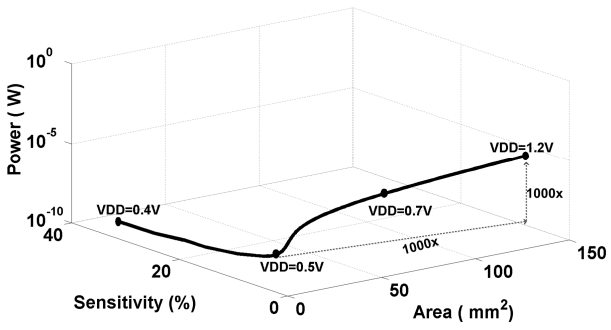

Fig. 9. Power Area and Sensitivity tradeoff

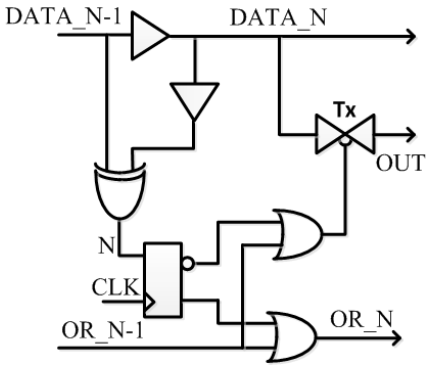

Fig. 10. Control Circuit

it will increase the receiver energy to leave it on for a longer period of time. The receiver consumes 200pJ/bit [2]. We choose to calibrate the circuit at the first calibration point in one-shot fashion. This minimizes the receiver on-time, which saves power. Once the delay point is selected, a control circuit is needed to output the data.

D. Control Circuit

Fig. 10 shows the control circuit. If OR_N-1=0 and the output of DFF goes high, then the transmission gate Tx turns ON, selecting that output of the delay line. Also, OR_N goes to the next stage as well. So OR_N=1 will prevent the multiple selections. Fig. 11 shows the timing diagram, and Fig. 12 shows a complete circuit diagram. The selected data is re-sampled at the falling edge of the clock. This removes the jitter in the data that will come in the subsequent cycles, up to half a clock cycle of jitter (~2.5µs). The retention block keeps the net going into the DFF at ground before the calibration. Once the path is calibrated, the clock to the DFFs is gated using OROUT (Fig. 11). The flops retain their values for the entire period of transmission. Once a transmission ends, the CDR resets and is now ready for the next transmission.

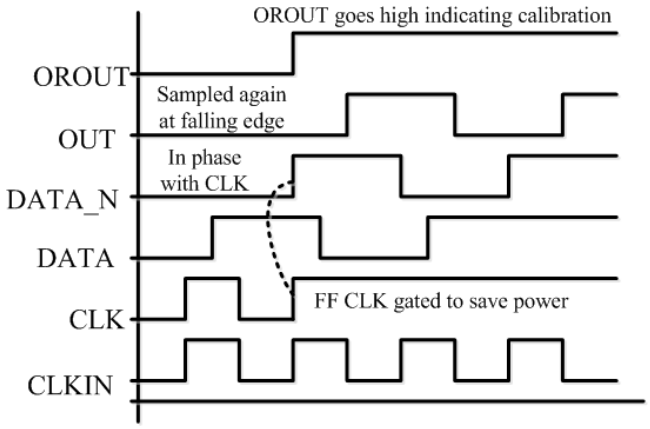

Fig. 11. Timing Diagram

One limitation of the design is that clock recovery is not adapted continually, which lowers the BER of the circuit. This is needed to account for the offset between the Tx and Rx clock frequencies. If Rx and Tx clock are generated from crystal oscillator and vary by 50ppm [6], then the channel should be recalibrated every 20k cycles which sets the inherent BER of CDR to $5x10^{-5}$. However, this limitation does not significantly degrade the overall BER of the link, which is set by the RX and is 10^{-3} [2]. A second limitation is that the total delay of the delay line should be greater than 5µs for this circuit to work correctly. Since the delay in sub-threshold varies exponentially with process variation, the spread of the total delay will be very large. We can compensate variation by lengthening the delay line or by reducing V_{DD} slightly. It is also possible that the DFF in one of the phase detectors can enter a meta-stable state during calibration, increasing power consumption briefly. However, this probability is very low due to noise (thermal, flicker etc.) and the 2.5µs hold period.

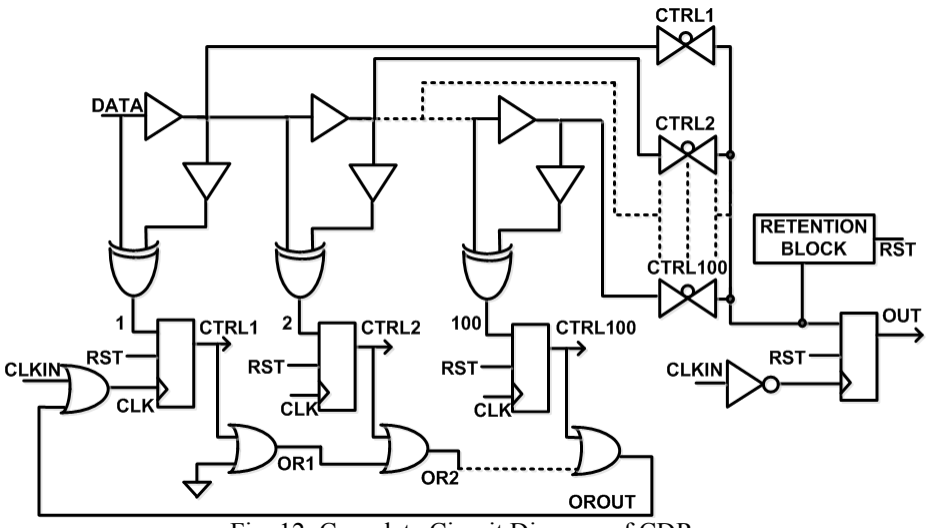

Fig. 12. Complete Circuit Diagram of CDR

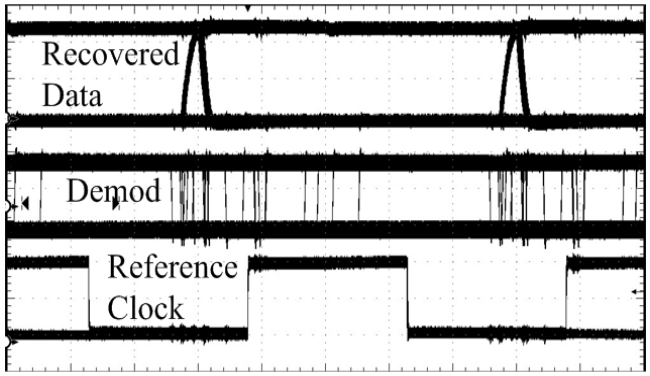

Fig. 13. Measured Data recovery from FSK Demod with 2µs Jitter

III. MEASUREMENTS

The proposed circuit is fabricated in 130nm CMOS technology. We used 0.5V as the power supply for the CDR circuit and it consume 50nW of average power. In the measurement test we measured eye diagram of the FSK demod out and the CDR data out for a 2^7-1 pseudo random data sequence running through the RX at a data rate of 100 kbps. Fig. 13 shows the measurement results. The FSK demod output has a jitter of ~2µs, while the data recovery circuit recovers the data with a jitter of 16ns. The area of the proposed circuit is 0.017µm^2. It consumes 50nW of power which translates to 0.5pJ/bit.

TABLE **1** compares the work with the literature on low power CDRs. Our chip is over 2X lower power, over 2X lower area (lowering cost and leakage power), and has 18X faster acquisition time than comparable prior art. The proposed circuit is purely digital and hence can easily be synthesized. These features make it ideally suited to applications like energy harvesting BSNs for which low

TABLE 1

Design Comparison show that CDR consumes less than 2x power and 2X area than prior art

	[3]	[4]	[5]	This Work
Technology	90nm	0.25µm	0.18µm	0.13µm
Data Rate	200kb/s	2Mb/s	10Mb/s	100kb/s
Acquisition Time	54µs	45µs	-	2.5µs
Power (CDR)	217nW	112µW	8.05µW	50nW
Energy/bit	1pJ	56pJ	0.8pJ	0.5pJ
Area(mm^2)	0.035	-	0.09	0.017

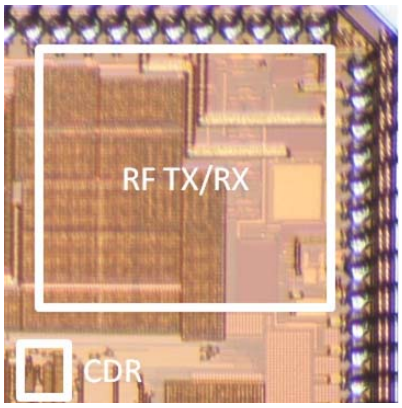

Fig. 14. Die Photo of the CDR along with Rx/Tx

power consumption is a driving constraint. Fig. 14 shows the die photo the CDR.

IV. CONCLUSION

We presented a low power CDR circuit for a wireless body sensor node. The proposed circuit interfaces the RF receiver output with the digital processing. It consumes 50nW at 100kbps or 0.4pJ/bit. Measurement results show that the CDR circuit recovers the data from FSK demod of the receiver with upto 2µs jitter. The proposed circuit is calibrated in one-shot fashion to save power, locking over 18X faster than prior art. The proposed circuit is fabricated in a 0.13µm CMOS technology. It can recover data with an input jitter of up to 2.4µs with >2X less power and >2X less area than prior work. The proposed circuit is completely implemented using digital gates and can easily be synthesizable.

REFERENCES

[1] F. Zhang, et. al, "A Battery-less 19µW MICS/ISM-Band Energy Harvesting Body Area Sensor Node SoC ", *IEEE International Solid State Circuits Conference,* 2012

[2] J. Pandey, S. Jianlei and B. Otis, "A 120µW MICS/ISM-band FSK receiver with a 44µW low-power mode based on injection-locking and 9x frequency multiplication", *IEEE International Solid State Circuits Conference,* 2011

[3] T. Kleeburg, J. Loo, N. J. Guilar, E. Fong and R. Amritharajah , "Ultra-low-voltage circuits for sensor applications powered by free-space optics", *IEEE International Solid State Circuits Conference,* 2010

[4] S-J Song, N. Cho, and H-J Yoo, "A 0.2-mW 2-Mb/s Digital Transceiver Based on Wideband Signaling for Human Body Communications", *IEEE Journal on Solid State Circuit*, September 2007

[5] S. Kim, et. al, "A low-power referenceless clock and data recovery circuit with clock-edge modulation for biomedical sensor applications", *IEEE International Symposium on Low Power Electronics and Design,* 2007

[6] LQXO-4 Oscillator, Low Power Crystal Oscillator- Datasheet. SATEK Corporation, ORANGA, CA