

Modeling DC-DC Converter Efficiency and Power Management in Ultra Low Power Systems

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Abstract— This paper presents a model of a DC-DC converter that is used to study power management techniques like DVFS, PDVS, etc. It accurately predicts the behavior of DC-DC converters of varying topologies across output voltage and current load and predicts the relative benefits of different power management options.

Index Terms—DC-DC, DVFS, Power Management.

I. INTRODUCTION

This paper presents a model to accurately establish the benefits of power management techniques for ultra low power (ULP) SoCs. Various power management techniques like dynamic voltage and frequency scaling (DVFS), clock gating, power gating, etc. are now commonly employed in many SoCs. However, the power benefits of these techniques cannot be established accurately without assessing their impact on the DC-DC converter that delivers power. For example, DVFS uses high voltage to support higher performance and lower voltage to save power. However, changing the output voltage of a DC-DC converter incorporates significant power overhead, and the efficiency can vary widely across voltage and current load. These overheads may offset the benefits from DVFS. There is a need to measure the benefits of power management techniques like DVFS, clock gating, etc. in conjunction with their impact on the DC-DC converter. This is particularly important for near- or sub-threshold systems that operate in a very dynamic power environment. This paper presents a model that enables the study of various power management techniques by taking into account their impact on DC-DC converters of different topologies.

II. DC-DC CONVERTER POWER MODEL

The efficiency of a DC-DC converter is a function of its output load, output voltage V_O , the switching frequency, etc. In a dynamic power environment, for ex. DVFS, V_O and load current vary dynamically, which changes efficiency of the converter resulting in energy overhead. Also, the converter can take significant time to settle from one voltage to another resulting in timing overhead. Additional energy overhead comes in the form of charging and discharging of the decoupling capacitor. To establish the benefit of a given power management technique like DVFS, we need to account for these overheads. The proposed model accounts for these

overheads and provides a framework where a given power management technique can be suitably studied.

A. DC-DC Efficiency with Load Current

The efficiency of a DC-DC converter degrades at both high load and light load condition. At higher load, where the output current is higher, the switch transistor needs to be on for longer duration of time (assuming pulse width modulation (PWM) control) which results in an elevated conduction loss. At light load condition the switching losses increase. Assuming PWM control scheme, we know that the power loss is given by,

$$P_{Loss} \propto aI_L + b/I_L \text{ where } I_L \text{ is the load current.}$$

The efficiency with load current I_L can be approximated as,

$$\eta_i = \eta_2 - (\eta_2 - \eta_1) * (\log(I_L/I_0))^2 / 4 \dots\dots\dots(i)$$

Where η_2 is the peak efficiency occurring at load I_0 , η_1 is the minimum efficiency at a given load.

B. Efficiency with Output Voltage:

The peak efficiency of the converter decreases with a decreasing output voltage. For a given load current, the switching loss and conduction loss of the converter remains the same. The decreased output power level at lower voltages results in a decreased efficiency. The efficiency with voltage can be modeled as,

$$\eta_v = \eta_1 + m * (V - V_{min}) \dots\dots\dots(ii)$$

Where m is the slope of the line given by $m = (\eta_2 - \eta_1) / (V_{max} - V_{min})$. From (i) and (ii) The combined voltage and load efficiency can be written as

$$\eta = \eta_v * \eta_i \dots\dots\dots(iii)$$

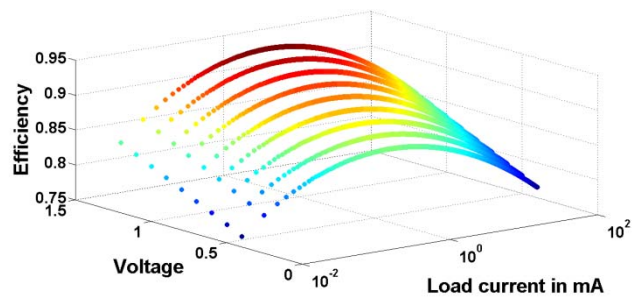


Figure 1: Efficiency with Load Current and Voltage (V_O)

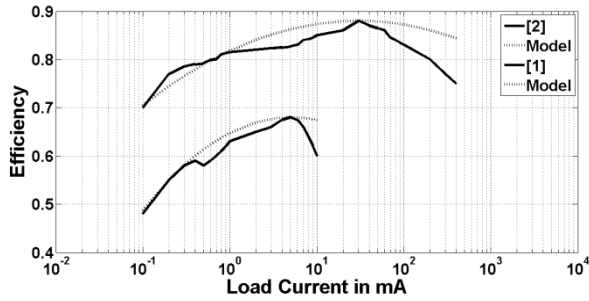


Figure 2: Proposed Model vs Numbers from literature

Figure 1 shows the output of the proposed model with V_O and load current. A DC-DC converter designed for a specific voltage and load will follow this trend when its load current or output voltage changes. Figure 2 compares the proposed model with efficiency data from literature [1,2]. It shows that the model can predict the behavior of a DC-DC converter within 90% accuracy across different architectures

C. Settling Time:

The settling time of a converter is the time it takes to reach the desired supply voltage. A typical converter has a large inductor and a large filter capacitor which makes the settling time very large (few μ S to mS [2]). In a dynamic environment like DVFS, UDVS etc. the output voltage V_O is expected to change. The settling time of a converter to reach the desired voltage becomes an important overhead for these scenarios. The additional settling time ΔT in our proposed model is approximated as,

$$\Delta T = T/V * \Delta V \dots \dots \dots (iv)$$

Where T is the settling time of the converter when output voltage is charged to V from ground.

D. Rail Switching Energy:

The change in the output voltage of a converter results in a change of the stored energy on the capacitor. Some of this stored energy is dissipated if the new voltage is lower than the previous voltage, whereas energy is consumed from the source supply, V_{in} , if the new voltage is higher than the previous voltage. The additional energy overhead E_c is given by equation (v) where V_1 and V_2 are the new and previous voltages of the converter. If V_1 is greater than V_2 , work is to be done by the supply V_{in} . When V_1 is less than V_2 , no work is done by V_{in} hence energy overhead will be zero.

$$E_c = V_{in} * CL * \{ \max(V_1 - V_2, 0) \} \dots \dots \dots (v)$$

Equation (iii) helps us to predict the losses at a given load and voltage condition, while (iv) and (v) gives the conversion

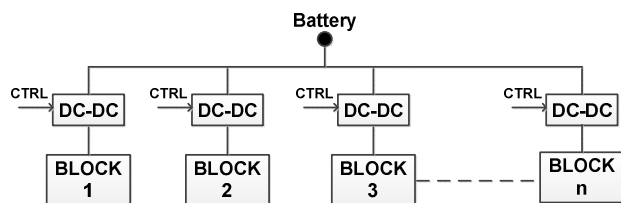


Figure 3: Dedicated DC-DC Converter per Block

VDD	Load	Time of operation	VDD	Load	Time of operation
V1 V	i1 uA	T1+ Δ T1 uS	0.9 V	100uA	6+2 uS
V2 V	i2 uA	T2+ Δ T2 uS	1.2 V	900uA	5+3 uS
....

Optimal condition for a block

Example Table

Figure 4: Operating Condition for Dedicated DC-DC

energy and timing overhead. These equations enable a framework where overheads which originate from a DC-DC converter can be calculated for techniques like DVFS to accurately measure their energy benefits.

III. BLOCK LEVEL POWER MANAGEMENT TECHNIQUE

DVFS has been used to save power in an SoC. Even bigger energy savings can be realized by implementing block level DVFS. Figure 3 shows the idealized implementation. However, it is not practically possible to implement such system because of area and cost. We study this scheme using our model to analyze its benefits by taking into account the overheads discussed earlier in the paper. Later on we compare this with a more practical implementation of block level power management.

A. Framework for Energy Calculation in DVFS:

Figure 4 shows the operating condition of an example block that has a dedicated DC-DC converter. VDD and load changes with time. We have assumed a random distribution on power supply. It changes from 0.4V to 1.2V. ΔT is the settling time of the converter and we use $T=20\mu$ S and $V=1V$ in equation (iv) [2]. The load capacitor on each block is assumed to be 200pF.

$$E_{op} = V1 * i1 * (T1 + \Delta T1) / \eta1 + V2 * i2 * (T2 + \Delta T2) / \eta2 + \dots (vi)$$

E_{op} is the operating energy and η is calculated using (iii)

$$E_c = V_{in} * CL * \{ \max(V1 - V2, 0) + \max(V2 - V3, 0) \} \dots$$

$$Total\ Energy = E_{op} + E_c \dots \dots (vii)$$

Each block is modeled as a chain of inverters with different depths. The delay of the block is calculated as its time of operation. The power supply level changes for 100 iterations. The rate at which voltage scaling happens is varied from 10nS to 1mS. The energy dissipation in each case is compared with a single VDD (always 1.2V) block. Figure 5 shows the result of our experiment. We find at that at fast rates of voltage scaling (~ 10 nS), the overheads of a DC-DC converter dominates and there is an energy loss. Energy benefits can be realized for TOP greater than 1 μ s with maximum benefit of more 150% can be

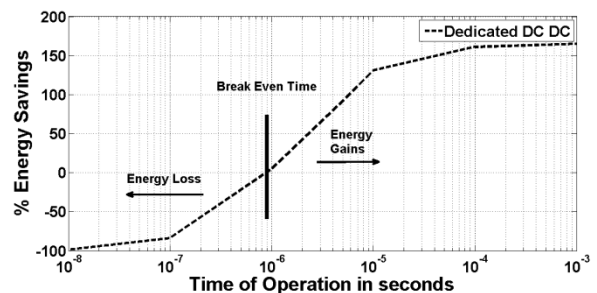


Figure 5: Energy Benefits with the Rate of Voltage Scaling

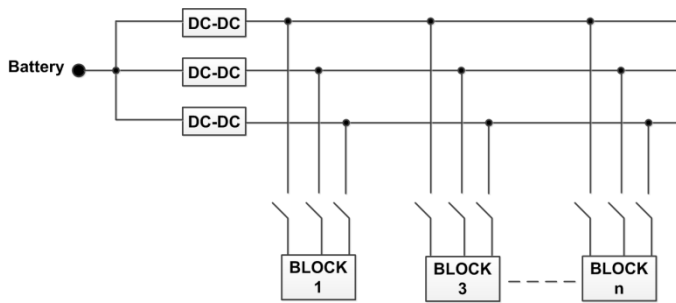


Figure 6: PDVS : Block Level Voltage Scaling Technique

achieved at slower rate of scaling. This implies that, for these assumptions, the 5 VDD system would save energy relative to the single VDD system when accounting for changes in the workload that are slower than $\sim 1\mu s$.

B. Panoptic Dynamic Voltage Scaling (PDVS):

Figure 6 shows the block diagram of a block level voltage scaling technique called panoptic dynamic voltage scaling (PDVS) [3]. In the PDVS technique, a block can switch from one voltage to another by the use of headers as shown in Figure 11. The advantage of this technique is that it enables a much faster switching. An equivalent DVFS voltage can be realized by dithering between the supplies. This scheme is more practical and has lower cost.

C. Framework for Energy Calculation in PDVS:

We reproduce the operating condition of a block from Figure 4. This block operates at different voltages for different times to accomplish optimal energy operation. We break down operating condition of Figure 4 into Figure 7. If a block has to operate at V_1 ($0.4V < V_1 < 0.8V$) for T_1 time, PDVS accomplishes it by connecting the block to 0.4V for T_{11} and 0.8V for T_{12} , such that $T_{11} + T_{12} = T_1$ of Figure 4. This approach is called voltage dithering. The time T_{11} and T_{12} are such that the performance of the block does not change. A final operating condition is given by Figure 8 can be obtained. The load on each supply will change depending on the blocks that are connected to it and results in a continuous time varying load on each supply. We integrate in time to obtain the energy. Each supply has larger load variation which will have an impact on the overall efficiency. The total energy is given by ,

$$E_{op} = 0.4 \int i_1(t) / \eta_1(i_1) * dt + 0.8 \int i_2(t) / \eta_2(i_2) * dt + 1.2 \int i_3(t) / \eta_2(i_2) * dt$$

VDD	Load			T _{op}
	0.4V	0.8V	1.2V	
V1V	i11 uA	0	0	T11
V1V	0	i12 uA	0	T12
V2V	0	i21 uA	0	T21
V2V	0	0	i22 uA	T21
....

Figure 7: Operating Condition for PDVS

Load			dT _{Op}
0.4V	0.8V	1.2V	
$i_1(t)$	$i_2(t)$	$i_3(t)$	1e-9

Figure 8: PDVS Final load table

$$E_c = 1.2 * CL * 0.4(1+0+0+0..) + 0.8 * CL * 0.4(0+1+1+0..)$$

$$Total Energy = E_{op} + E_c$$

We keep the same system set-up as was used for the dedicated DC-DC converter case. It should be noted that there will not be an overhead of settling time in this case. We assume a capacitive load of 20pF on each block.

IV. RESULTS

Figure 9 compares the PDVS scheme with a dedicated DC-DC converter case. The PDVS scheme has a break-even time of 30ns compared to 1uS in the dedicated supply case. This is because of the absence of settling time in PDVS as the block is charged to the rail instantly. It also has lower conversion energy. The total energy benefits from the PDVS scheme is however lower than the dedicated DC-DC converter case, because it sees much wider load variation. The PDVS scheme however is better suited for implementing block level DVFS owing to its much smaller break-even time.

V. CONCLUSIONS

A power model which can accurately predict the behavior of DC-DC converter in a dynamic environment has been presented. The model has been validated and compared with existing literature. We use this model to study block level power management techniques for an SOC. The model predicts that there is a break-even time, before the benefit of voltage scaling becomes positive. We can therefore merit one technique over the other in a given use case scenario by employing the proposed model.

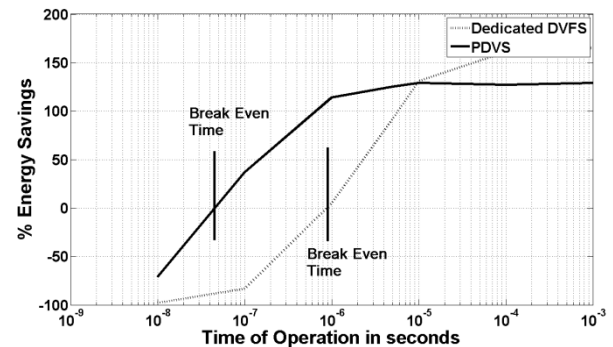


Figure 9: Energy Benefits of PDVS and Dedicated DVFS

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