Analyzing and Modeling Process Balance for Sub-threshold Circuit Design

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ABSTRACT
This paper describes the strong effects on sub-threshold digital circuit operation of the ratio of PMOS and NMOS current in a given process. We define the concept of process balance/ imbalance as describing this ratio and explain the impact of different circuit and environmental parameters on process balance. Many of these characteristics are best understood by the degree to which they increase or further decrease process balance. We also propose a model that provides accurate estimation of the effects of process balance that is useful for understanding the impact of process variations and the appropriate types of circuits to use for sub-threshold operation in a given process.

Categories and Subject Descriptors
B.7.1 [**Integrated Circuits**]: Design Styles – *VLSI, Advanced technologies.*

General Terms: Performance, Design, Reliability, Theory

Keywords: Sub-threshold digital circuits; minimum energy operation; sub-threshold modeling; process balance; process imbalance; variations.

1. INTRODUCTION
Power consumption in CMOS integrated circuits has increased to the point that circuit design has entered a power-limited era [1]. Essentially all designs in modern technologies are constrained in some way by the amount of power they consume. Power constraints become especially important for embedded applications due to the need to extend system lifetimes. Emerging applications such as wireless microsensor networks and medical devices are severely energy-constrained as a result of small form factors and extended lifetime requirements. The necessity to conserve every scrap of energy makes energy-constrained applications an ideal fit for sub-threshold circuit operation.

Both analog (e.g. [2]) and digital (e.g. [3]) sub-threshold circuits were identified for low power applications in the 1970s. Although analog sub-threshold circuits were investigated since that time, digital operation was largely ignored until the late 1990s [4]. Sub-threshold digital circuits use a supply voltage V_{DD} that is less than the threshold voltage, V_T, of the transistors. In this region, both on- and off-current depend exponentially on V_{GS}-V_T. Although digital sub-threshold circuits are slower due to the lower current, they also reduce power and energy consumption significantly due to the quadratic reduction of these metrics with supply voltage. Sub-threshold circuits are known to provide minimum energy operation over most scenarios [5][6]. The minimum energy point occurs because of the exponential increase in leakage energy per operation (due to longer cycle times) that eventually exceeds the diminishing contribution of dynamic energy per operation.

Recent previous work in this area has made sub-threshold circuits a more viable option for low-power designers. The first sub-threshold processor, an FFT processor, demonstrated logic operation down to 180mV and experimentally verified minimum energy operation [7]. The first sub-threshold memory, a 256kb array in 65nm CMOS, was demonstrated [8], and more generalized sub-threshold processors are appearing [9]. Still, several key issues must be resolved to improve the design process before sub-threshold circuits can achieve widespread use.

The most daunting obstacle to sub-threshold circuits is process variation. Variations in CMOS process parameters, interconnect and transistor dimensions, and device characteristics make reliable circuits more difficult to design in general in deep sub-micron processes, and variations will only worsen as devices continue to shrink. The impact of such variations is amplified in sub-threshold circuits because of the exponential dependence of device currents on parameters such as threshold voltage. In the best case, variation reduces the available energy savings in sub-threshold [10], and, in the worst case, they can cause functional failure (e.g. [8]). Variations can occur at a large scale from die-to-die (D2D, or global variations) or locally within a die (WID, or local variation [17]). Although physical variations exist in many parameters, we focus on threshold voltage variation in this paper.

We will define the notion of process balance and show that a clear understanding of this characteristic of sub-threshold circuits is essential to evaluating the impact of both D2D and WID variations in different processes and to developing general methodologies for sub-threshold design. Many previous works have examined sub-threshold operation in a specific process and then offered conclusions that might not necessarily apply broadly to sub-threshold circuits in other contexts (e.g. [4]-[13]). We will show that, unlike for strong inversion circuits, these conclusions are often not applicable because other processes are differently balanced. Our analysis will extend the state of the art for sub-threshold design by specifying exactly when generalizations are likely to work and when they should be approached with caution. We also provide models that illustrate how different amounts of process imbalance alter circuit characteristics to the extent that they require different changes in circuit selection and design.

Section 2 defines process balance and process imbalance and analyzes the impact of various factors for different types of processes. Sections 3 and 4 describe the specific impact of process imbalance on combinational logic and SRAM bitcells, respectively. Section 5 provides models for evaluating the impact of process imbalance on digital circuits, and Section 6 offers our conclusions.

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2. Sub-threshold Process Balance/Imbalance

This section defines the concepts of process balance and imbalance and then describes the impact of a number of effects on the sub-threshold balance of a particular process.

2.1 Process Balance/Imbalance

For strong inversion operation, processes all start from a common reference point. Specifically, NMOS devices are always ~2-3 times stronger than iso-sized PMOS devices due to the higher mobility of electrons relative to holes. We can therefore describe CMOS processes as having essentially the same "balance" for strong inversion operation. However, this is decidedly not the case for sub-threshold circuits. Although processes can theoretically be designed for sub-threshold operation (e.g. [11]), the relative rarity of sub-threshold circuits makes this unlikely in practice. Instead process engineers define each process for strong inversion operation, and the characteristics of the process for sub-threshold operation are a secondary or even ignored consideration. As a result, processes that are very similar in strong inversion can exhibit markedly different traits in sub-threshold. We can broadly identify and describe these differences under the heading of process balance.

We define sub-threshold process balance generally as the relative strength of PMOS and NMOS devices in a process. We will specifically define the process balance factor (PBF) as the ratio of PMOS to NMOS on-current for devices having the same physical dimensions in a given process at the typical process corner. A process is considered balanced if the NMOS and PMOS current are the same (or quite close) and increasingly imbalanced as the process balance factor differs more and more from unity. Despite having similar strong inversion characteristics, the ratio of P/N current in sub-threshold can differ substantially from process to process.

Figure 1 shows an example of how processes can differ. The global process corners (e.g. Fast NMOS, Slow PMOS (FS), etc.) create a rough box around the typical point (Typical NMOS, Typical PMOS (TT)) on a plot of relative PMOS and NMOS strength for two conceptual processes. The process balance point determines the location of this box relative to the balanced (symmetrical) case, which is represented by the dashed line (x=y). Global variation in a given process describes where a given die falls within this box, and local variations describe how individual devices vary in strength around that process corner. Process I in Figure 1 represents a Strong-PMOS (S_P) process, because its TT point falls above the balanced line (PBF>1). Process II, on the other hand, demonstrates a Strong-NMOS (S_N) process with a TT point below the symmetrical line (PBF<1). Generally, processes with a TT point farther from the symmetrical case are more imbalanced (PBF farther from 1).

In sub-threshold, device symmetry is quite important because it provides the best-case for circuit stability and robustness for static CMOS circuits. Prior work on sub-threshold circuits has recognized the advantages of having matched PMOS and NMOS current and has suggested or used body biasing to achieve symmetrical devices (e.g. [18][19]). Although the practice of body-biasing can nullify (at least partially) the final impact of process imbalance, a clear understanding of process imbalance and its implications is important for implementing sub-threshold designs and for correctly applying results from the literature. Furthermore, body biasing is not always available (e.g. no triple wells) or is too costly in terms of overhead (power and area).

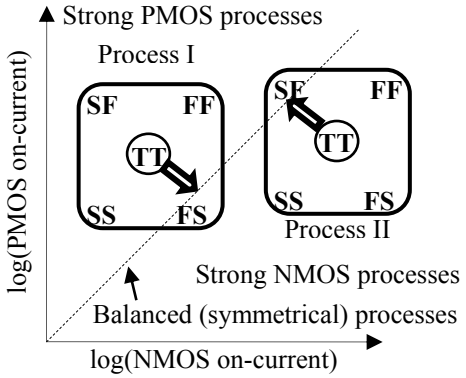

Figure 1: Process imbalance relative to the PMOS/NMOS symmetrical case sets the relative strengths of devices and affects circuit choice and the impact of variations. The TT corner (typical NMOS, typical PMOS) centers the other corners (e.g. Fast NMOS, Slow PMOS (FS)) relative to a balanced process (centered on the dashed line).

Whether or not body biasing is used, process balance is an essential concept to understand for sub-threshold designers.

Prior results related to sub-threshold circuit operation have been published on circuits in both Strong-N (e.g. [12][6]) and Strong-P (e.g. [8][13]) technologies. Often, the conclusions drawn in these works are stated as having general applicability. In fact, we will argue in this paper that they are usually only applicable to processes with similar process balance factors, and caution is advisable in transferring them to processes with different balance points.

Figure 2 shows example IV curves of S_N (a) and S_P (b) processes, which are modifications of the processes provided by the predictive technology models (PTMs) [14][15]. S_N and S_P were created by changing the VT_0s and only the VT_0s of the 90nm PTM. Although these are not real processes, they correspond closely with the IV curves of commercial S_N and S_P processes from the authors' experience. Again, the strong inversion characteristics of the two processes are nearly identical, but the PBF differs by nearly two orders of magnitude. Clearly, this change will have substantial impact on the behavior of a given circuit in the two processes.

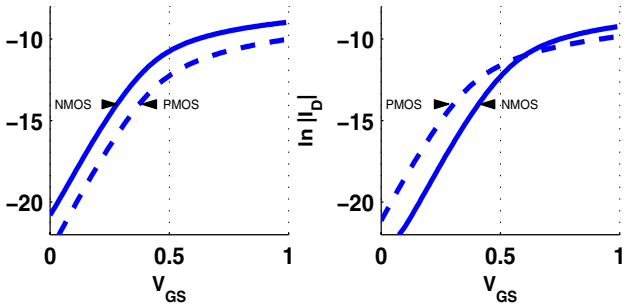

Figure 2: IV curves for sub-threshold processes that are imbalanced to be Strong-N (a) and Strong-P (b).

One notable effect of process balance, which can be inferred from Figure 1, is that global variations have different impact depending on the PBF. For example, the SF global process corner will improve the process balance for the strong NMOS process in Figure 3(a) by bringing the PBF nearer to a value of one (although inverting it to a strong PMOS scenario).

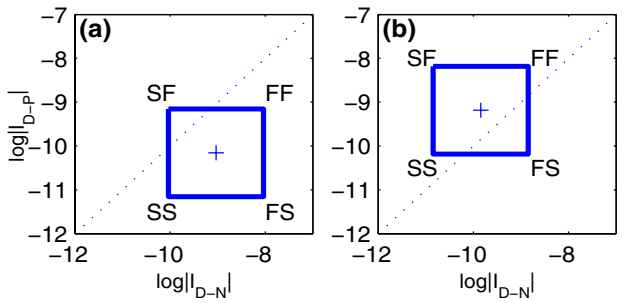

Figure 3: Corner plots for Strong-N (a) and Strong-P (b) processes.

In contrast, the SF global corner will dramatically decrease the balance of the strong PMOS process in Figure 3(b). In both cases, common changes to both NMOS and PMOS (e.g. along the line connecting the SS and FF corners) will not alter the PBF, although these corners will provide large changes in speed. Clearly, the impact of global process corners cannot be correctly evaluated without first understanding the process balance.

By analyzing process balance and referring to the symmetrical case, designers will understand quickly how a circuit will behave across technologies and variation scenarios. Knowing the impact of process balance will help to identify specific circuits that require redesign based on the technology and will facilitate designing sub-threshold circuits in general.

2.2 Factors Affecting Process Balance

A number of different factors can alter the process balance. First, we have specified the PBF to be the ratio of on-current. This definition makes the PBF useful for understanding tradeoffs related to speed, which depends on the on-current. The most common significant difference between NMOS and PMOS that creates an imbalance in sub-threshold on-current is a difference in threshold voltages. So long as other factors are the same (e.g. DIBL, sub-threshold slope (S)), the ratio of P/N currents will remain constant even when V_{GS} changes (as is nearly the case in Figure 2, in which P and N currents are nearly parallel in the sub-threshold region). In general, the PBF tends to be fairly representative of the ratio of P/N current across the full range of V_{GS}, but this is not necessarily the case.

Differences in sub-threshold slope (S) for PMOS and NMOS devices tend to be fairly small, but they are certainly possible. Clearly, different values of sub-threshold slope can cause off-current to be imbalanced even if the PBF is unity. For example, a larger S for PMOS will mean that $I_{OFFP}>I_{OFFN}$ even if the PBF is one. This in turn makes the I_{ON}/I_{OFF} ratio generally worse (e.g. lower) for CMOS gates with output high, because the pull-down tree is leaking. Since the I_{ON}/I_{OFF} ratio is quite important for sub-threshold circuit robustness, this issue is important to understand when S differs for the devices. In Section 5, we will show the impact of differing S on switching threshold and noise margins.

Another trait of devices that affects the process balance is drain-induced barrier lowering (DIBL). If PMOS and NMOS devices have different DIBL coefficients, then the PBF becomes dependent on the operating voltage. If the disparity between NMOS and PMOS DIBL is large, then designers must decide on a specific operating voltage early in the design cycle in order to make correct decisions about circuit structures, etc. A large difference in DIBL coefficients will also make the use of multiple sub-threshold operating voltages more difficult, since process balance will vary across those points.

Process scaling can clearly change the sub-threshold balance point. For example, Figure 4 shows how the PTM processes vary with scaling. These technologies become more N-strong with scaling. Furthermore, taking global variation to be the same percentage of V_T, the global corners spread out farther for more deeply scaled devices, as shown in Figure 4. Figure 5 shows that the DIBL effect becomes more significant with process scaling in the PTMs. This has one side effect that is helpful for sub-threshold operation; although I_{OFF} is larger for more scaled technologies at the nominal V_{DD}, it actually is smaller (because of larger DIBL) for sub-threshold circuits in scaled technologies. Figure 5 shows that the crossover point is around 500mV. Different technologies can obviously show different trends with scaling.

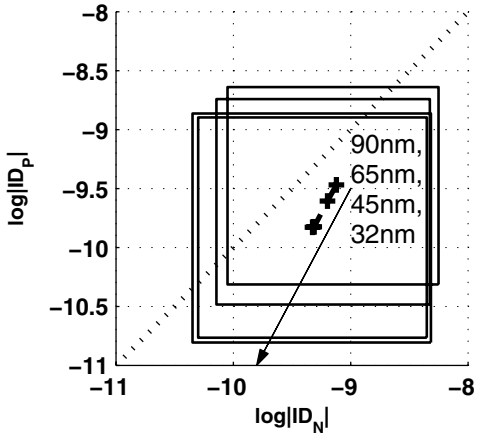

Figure 4: The change in process balance and the impact of global variation for PTMs. Different technologies may show different trends.

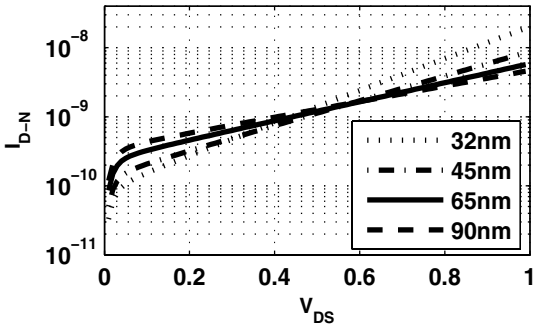

Figure 5: MOSFET current showing DIBL effect on off-current for NMOS using the PTMs. Process balance can change with V_{DD} if P,N DIBL differs.

Sizing also can have an impact on process balance. Generally, the linear W/L impact that first order equations describe is secondary. Since process imbalance can readily produce PBFs that differ from unity by over an order of magnitude, the linear impact of sizing is a weak knob for restoring balance, as shown in [6]. In contrast, higher order effects that result from deep process scaling can impact the process balance more significantly by altering V_T. Specifically, the short channel effect, reverse short channel effect, narrow channel effect, or reverse narrow channel effect can dramatically alter the relationship between PMOS and NMOS current. Figure 6 shows device current versus size at V_{DD}=200mV for a commercial 90nm technology as an example. In this technology, minimum width

devices have much worse process balance than slightly larger devices. These higher order effects can vary with supply voltage, so sub-threshold designers should note their impact at the desired operating point. If reverse short channel effect is dominant, then a special sizing strategy can actually improve sub-threshold robustness [21]. However, the impact of all of these effects tends to vary across technologies.

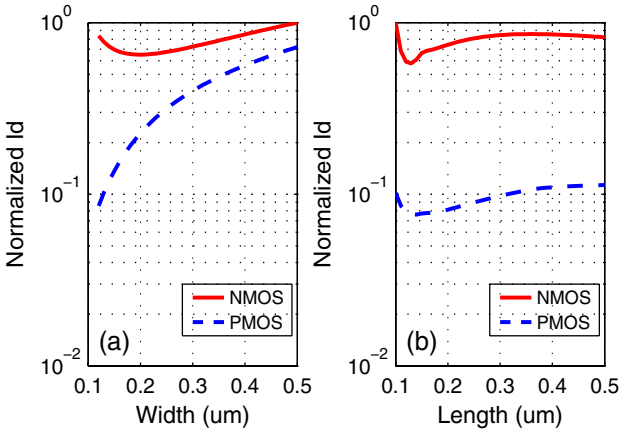

Figure 6: Normalized I_D versus size in a commercial 90nm process. Forward/reverse short/narrow channel effects affect process balance and can vary across processes.

As we have previously discussed, the process balance alters the way in which global variation affects sub-threshold circuit robustness. A similar scenario exists for local variation. Local variations that are beneficial in a strong-PMOS technology are likely to be detrimental in a strong-NMOS technology. In other words, the best-case and worst-case tails of the distributions of various metrics may switch.

We propose that the best method for evaluating variations in the context of process balance is to determine whether they drive the PBF closer or farther from 1 (e.g. increase or decrease balance). Framing the problem this way provides immediate insight into the positive or negative influence of certain variation scenarios.

Changing temperatures also can alter the process balance. This change occurs when NMOS and PMOS currents vary by different rates with temperature. Again, we recommend that the impact of temperature be determined by examining if the process becomes more or less balanced. Suppose that NMOS devices become stronger relative to PMOS at higher temperatures. This means that higher temperatures will increase the balance (move the PBF toward 1) for strong-P technologies and decrease the balance (move the PBF away from 1) for strong-N processes.

3. Impact on Combinational Logic

3.1 Logic Style

Static CMOS is the most common logic style used in sub-threshold due to its robustness. Pseudo-NMOS has also been proposed because some of its disadvantages in strong inversion are mitigated in sub-threshold [4]. The always-on PMOS pull up in pseudo-NMOS is less sensitive to changes in size, but more sensitive to process variations. As a result, the pseudo-NMOS logic style cannot function well in strong-PMOS technologies, because variations in the pull-up device can cause it to overpower the pull-down network despite efforts to counteract this by sizing. Specifically, the distribution of the output low logic level (V_{OL}) can reach nearly to V_{DD} [22]. This sensitivity dramatically reduces the yield of pseudo-NMOS logic for strong-P processes.

Static CMOS logic is more robust across different process balances in terms of functionality. However, different metrics applied to static CMOS will vary broadly as process balance changes. This has strong implications for standard cells designed to operate in sub-threshold. Characterization of standard cell libraries will vary dramatically with technology. Process balance also will alter the robustness of static logic by varying noise margins, which we discuss in the next section.

3.2 Noise Margins

Process variations cause noise margins in static CMOS sub-threshold logic to vary [13]. The impact of these variations will change depending on the process balance. To understand this, we will examine the impact of process balance. Figure 7 shows how the VTC of a sub-threshold inverter changes with process balance. The balanced process has a switching threshold, V_M, that occurs at $V_{DD}/2$. This maximizes the high and low noise margins and sets them equal. For processes that are imbalanced toward strong-P or strong-N, either the noise margin low or high will degrade, respectively. As the figure indicates, the change in V_M and noise margins is symmetrical about the balanced process. In Section 5, we will describe a model for relating V_M to process balance.

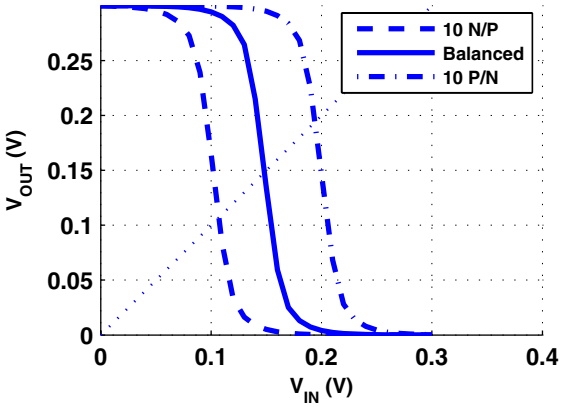

Figure 7: Process balance affects noise margins.

4. Impact on SRAM Bitcell Stability

The Static Noise Margin (SNM) of an SRAM bitcell in sub-threshold is dependent on various factors such as global and local threshold variation, V_{DD}, sizing, and temperature [22]. In addition to these other factors, process imbalance also has an impact on SNM. Figure 8 shows the degradation of SNM for a cell holding its data (hold SNM) for imbalanced processes compared with a balanced process. The maximum hold SNM for a certain V_{DD} in sub-threshold occurs for the balanced process (BAL), which has its trip point V_M of the cell VTCs located at the center coordinate ($V_{DD}/2$, $V_{DD}/2$) because of the equalized strength between NMOS and PMOS. However, for a Strong-NMOS process (S_N), V_M moves to the lower-left side, which causes a degradation of the SNM. With an increase of NMOS strength, V_M moves farther away from the central point and thus SNM is decreased to a lower value. Similarly, the Strong-PMOS process (S_P) also leads to a degradation of SNM but with the V_M moving to the upper-right side. Therefore, to obtain a higher SNM, the imbalanced processes should be adjusted towards the balanced one.

Besides SNM, data retention voltage (DRV) is another critical metric when considering SRAM stability at low voltage during standby operation. DRV is defined as the lower bound of V_{DD} that will preserve data in an SRAM bitcell [24]. The reduction of DRV can improve power savings and/or stability for SRAM. Since the DRV is actually the V_{DD} where the SNM is equal to zero, a lower hold SNM at a given V_{DD} level implies that a higher DRV is required to preserve data. Therefore, imbalanced processes degrade both DRV and SNM. In order to lower the DRV, it is also important to compensate for the imbalanced strength between N and P.

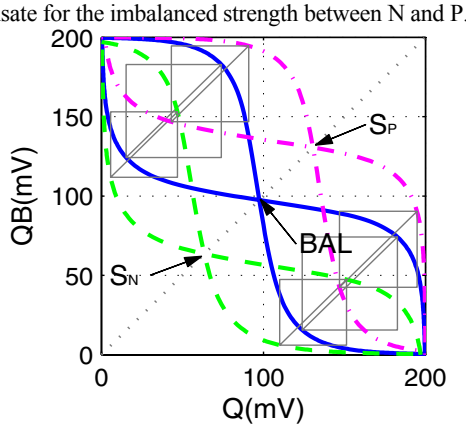

Figure 8: Static Noise Margin (SNM) for imbalanced processes (Strong-P (Sp) and Strong-N (Sn)) degrades.

During a read operation, since the access NMOS is turned on, the voltage of a cell node's '0' becomes higher than zero. For this reason, read SNM is usually dramatically reduced compared with hold SNM. Because of the higher voltage at the node holding '0', the other node which is holding a '1' is more vulnerable to flipping when the driving strength of the pull-down NMOS is strong. A Strong-NMOS process therefore degrades the read SNM. On the other hand, a process with a relatively strong PMOS improves the stability of the node with a '1', and that leads to a higher read SNM. However, if the PMOS is too strong or the NMOS is too weak, read SNM decreases because the '0' node is more sensitive to noise, and thus write-margin can suffer.

5. Modeling Process Imbalance

In order to design circuits operating in the sub-threshold region, it is desirable to model the effect of the process imbalance factor (PBF) of I_P/I_N on circuit behavior. In this section, we model the switching threshold, V_M, of an inverter operating in the sub-threshold region. We initially derive an estimate of the relationship between V_M and PBF by graphically analyzing the imbalance in a simplified plot device current. We then independently confirm the trend shown in this graphical analysis by deriving V_M using weak-inversion current equations.

Figure 9 shows the sub-threshold current for a pair of NMOS and PMOS transistors, which have the same S and no DIBL for mismatch in this conceptual process gives a PBF of I_P/I_N=exp(-2). The current of the ideal balanced case is shown as a dotted line equidistant between the NMOS and PMOS currents.

illustration, operating in the sub-threshold region. Threshold

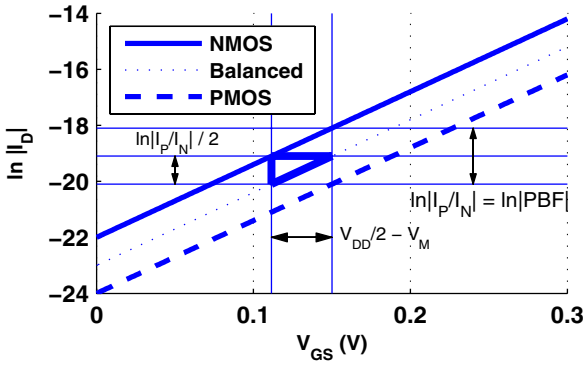

Figure 9: Plot of V_{GS} vs ln|I_D| of conceptual NMOS and PMOS transistors with matched S, no DIBL, PBF=exp(-2), and V_{DD}=0.3V

This plot illustrates how V_M is affected by PBF graphically to demonstrate that this technique can be applied to circuits more complicated than an inverter where analytical equations get too complex. When ln|PBF| drops below zero (when the NMOS is stronger than the PMOS), V_M shifts to the left of (V_{DD}/2). Similarly, when ln|PBF| becomes greater than zero, V_M shifts to the right. This point is illustrated on the plot with the darkly-shaded triangle. Extra lines at Y=$I_{D,VDD/2}$ (I_D of the balanced process at (V_{DD}/2)) and X=(V_{DD}/2) and X=V_M help to clarify key points of interest on the plot. The line at X=V_M is in an unknown location between 0 and V_{DD}/2 since ln|PBF| is less than zero. The slope of the hypotenuse of the dark triangle equals -0.5*ln(I_P/I_N)/ (V_{DD}/2)-V_M. Since this slope also equals ln10/S, we can solve for:

$$V_M = \frac{V_{DD}}{2} + \frac{S}{2}\log_{10}(I_{OFFp}/I_{OFFn}) \qquad (1)$$

where I_{OFFp} and I_{OFFn} are the off current of PMOS and NMOS, respectively, when we ignore DIBL.

In order to confirm this graphical model, we will now derive V_M analytically. The switching threshold of an inverter can be derived by equating the weak-inversion currents through NMOS and PMOS devices (at V_{IN}=V_{OUT}=V_M) and then solving for V_M. This results in (2), shown below:

$$V_M = \frac{V_{DD}n_n(1+\eta_p)}{n_n(1+\eta_p)+n_p(1+\eta_n)} + \frac{n_pV_{Tn}-n_nV_{Tp}}{n_n(1+\eta_p)+n_p(1+\eta_n)} + \frac{n_nn_pV_{th}\ln\left(\frac{(W/L)_pI_{op}}{(W/L)_nI_{on}}\right)}{n_n(1+\eta_p)+n_p(1+\eta_n)} + \frac{n_nn_pV_{th}\ln\left(\frac{1-\exp((-V_{DD}+V_M)/V_{th})}{1-\exp(-V_M/V_{th})}\right)}{n_n(1+\eta_p)+n_p(1+\eta_n)} \qquad (2)$$

where n_n and n_p are sub-threshold slope factors (S=nV_{th}ln10, V_{th}=kT/q), η_n and η_p are linearized DIBL coefficients, and I_{on} and I_{op} are the current at V_{GS}=V_T for NMOS and PMOS, respectively.

Equation (2) shows that asymmetry in device characteristics complicates the relationship between V_M and current ratio. If we assume that the devices are symmetrical except for V_Ts, and there is no DIBL, then (2) reduces to (3):

$$V_M = \frac{V_{DD}}{2} + \frac{V_{Tn} - V_{Tp}}{2} + \frac{nV_{th}\ln\left(\frac{1-\exp\left((-V_{DD}+V_M)/V_{th}\right)}{1-\exp\left(-V_M/V_{th}\right)}\right)}{2} \quad \textbf{(3)}$$

The final term of this equation only becomes significant (due to current roll-off) when V_M nears V_{th} or V_{DD}-V_{th}. Thus, for the range of voltages in between these values, we can ignore the final term. Since, based on our simplifying assumptions, the N and P currents are parallel, we can readily show that V_{Tn}-V_{Tp}=$S\log_{10}(I_{OFFp}/I_{OFFn})$. Thus, (3) reduces to be equal to (1):

$$V_M = \frac{V_{DD}}{2} + \frac{S}{2}\log_{10}(I_{OFFp}/I_{OFFn}) = \frac{V_{DD}}{2} + \frac{V_{Tn}-V_{Tp}}{2} \quad \textbf{(4)}$$

The model in (4) suggests that V_M will vary linearly until it approaches one of the supply rails and the low V_{DS} roll-off term starts to become significant. In order to determine the validity of the model, simulated V_M data for an inverter was plotted on top of the predicted V_M as shown in Figure 10.

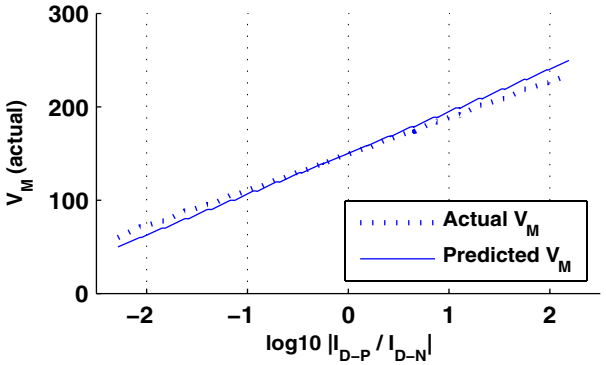

Figure 10: Simulation of V_M vs. log(I_P/I_N) shows the linear relationship over many orders of magnitude.

As seen in Figure 10, the linear prediction provides a fit of the data accurate within an average 3.2% error across five orders of magnitude. The error is due to the fact that differences between the sub-threshold slopes of the P and the N currents as well as the fact that second order effects such as DIBL were ignored.

We can understand the source of this error by examining (2) more closely. Differences between the sub-threshold slopes will cause V_M to shift by a fixed offset from (V_{DD}/2) due to the first, third, and final terms in (2). Sub-threshold slope difference in the second term of (2) essentially weights the difference in V_Ts linearly. DIBL causes an offset due to the first term, but tends to dampen the second, third and fourth terms.

6. Conclusions

In this paper, we have presented the concept of process imbalance and why it arises. In addition, we have described the effect of imbalance on combinational logic, noise margin, and SRAM bitcell stability. We have introduced and defined the Process Imbalance Factor (PBF) and developed a simple linear model to accurately predict the V_M of a minimum-sized inverter to within a mean 3.2% error for a PTM process.

Process balance has a strong impact on the way that process variations and environmental factors, like temperature, affect sub-threshold circuit behavior. The process balance of a given technology will likely even alter circuit choices made during the design process. We have provided a thorough analysis of process balance including a model for understanding its impact on V_M. We have also proposed that the impact of factors such as variation is best determined by analyzing whether those factors increase or decrease the process balance.

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