SRAM-Based NBTI/PBTI Sensor System Design

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ABSTRACT

NBTI has been a major aging mechanism for advanced CMOS technology and PBTI is also looming as a big concern. This work first proposes a compact on-chip sensor design that tracks both NBTI and PBTI for both logic and SRAM circuits. Embedded in an SRAM array the sensor takes the form of a 6T SRAM cell and is at least 30× smaller than previous designs. Extensively reusing the SRAM peripheral circuitry minimizes control logic overhead. Sensing overhead is further amortized as the sensors can be both reconfigured and recycled as functional SRAM cells, potentially increasing SRAM yield when other bit cells fail due to initial process variation or long time aging effects. The paper also proposes a variation-aware sensor system design methodology by quantifying and leveraging the tradeoff between the size and number of sensors and the system sensing precision. Design examples show that a system of 500 sensors can achieve 4mV precision with 98.8% confidence, and a system of 1K sensors designed for 1M SRAM bit cells achieves 2000× area overhead reduction compared to a worst-case based approach.

Categories and Subject Descriptors

B.7.3 [**Hardware**]: INTEGRATED CIRCUITS —*Reliability and Testing*; B.3.4 [**Hardware**]: MEMORY STRUCTURES —*Reliability, Testing, and Fault-Tolerance*

General Terms

Design, Performance, Reliability

Keywords

NBTI, PBTI, Sensor, Sensor System Design, Aging, SRAM, Yield, Redundancy, Process Variation

1. BTI-AWARE DESIGN

NBTI (Negative Bias Temperature Instability) is a major reliability hazard for concurrent CMOS circuit design. NBTI occurs with a negative gate to source voltage and increases PMOS threshold voltage, slowing down logic gates in digital design, causing mismatch in analog design and reducing read and hold noise margins for SRAM (this paper assumes standard 6T cells). Guardbanding through gate upsizing needs to cover the worst case from both manufacturing process variation and use conditions, and can lead to large area and power overhead [1, 2]. In particular, for SRAM upsizing is needed for every cell and reduces write stability.

An alternative is to embed sensors on chip to dynamically track NBTI and issue warnings before it manifests as system level failures. With process variation, multiple sensors may be needed. The sensors inherently capture process parameters like die-to-die variation and use-condition parameters like environment temperature, on-chip power noise and circuit usage. Minimizing sensing overhead is the key to any practical sensor design.

PBTI (Positive Bias Temperature Instability) has not caught much attention mainly due to their ignorable impact for thin gate oxide. PBTI happens when positive gate to source voltage is applied and weakens NFETs similarly as NBTI degrades PFETs. However, the introduction of thick gate oxide with high-k materials may move PBTI front and center in the next generation CMOS technology.

This work proposes a sensor system based on a compact sensor design that can be adapted for both NBTI and PBTI tracking. Motivated from 6T SRAM the sensor consists of only 6 transistors. A sensor system typically consists of hundreds or thousands of sensors to achieve decent sensing precision [9]. By quantifying the tradeoff between the system sensing precision and individual sensor design parameters in the presence of process variation, we arrive at a conclusion that greatly simplifies the precision analysis. Thereby we present a complete sensor system design methodology.

The next section examines related work. Section 3 describes the sensor, followed by the system design in section 4. Section 5 discusses BTI mitigation techniques. A design example and simulation results are shown in section 6. Section 7 concludes the paper.

2. SENSING OVERHEAD COMPARISON

Overhead minimization is the key to any practical sensor design, since the sensor number can go up to hundreds or thousands [3, 9] to achieve a decent precision in the presence of process variation.

Sensors can be designed to track NBTI continuously based on monitoring ring oscillator frequency, circuit delay or current degradation [4–7]. Binary sensors [3] are smaller but only tell whether a critical point is reached. The sensor in [7] is $308\mu m^2$ at $130nm$ technology, and is claimed to be 450× smaller than the sensor in [5]. The embedded sensor in [3] is $28\mu m^2$ in area at $65nm$ technology. In comparison, the proposed sensor is less than 2% larger than an SRAM cell. For our design at $90nm$ technology, this translates to less than $1.8\mu m^2$ in area, about 31× and 85× smaller than sensors in [3] and [7] if scaled into the same technology node. The sensor would be even smaller with sub-DRC rules enabled in high density SRAM designs. Moreover, the overhead associated with the control logic is also minimized by reusing existing SRAM peripheral circuitry for sensor control and data reading.

The sensor can be designed for NBTI, PBTI, or a combination of the two depending on which BTI (NBTI or PBTI) degradation dominates in the targeted technology. A sensor works like the 'check engine' light in cars and 'triggers' when a critical degradation point

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is reached. Being embedded in SRAM does not limit its application to only SRAM, since sensors do not distinguish whether the critical point is characterized for logic circuits or SRAM. Nonetheless, being embedded in SRAM makes the sensors particularly suitable for SRAM, since systematic process variation and power supply manipulation and noise may be better tracked. The proposed sensor presents minimum perturbation to the very regularly structured layout when embedded in SRAM.

A distinct feature of the proposed sensor is that once triggered they naturally become normal SRAM cells and can be recycled as redundancy to replace defect SRAM cells. It will be further shown that at any time during their lifetime, the sensors can function as SRAM cells. However, drafting them before their trigger point disables their function as sensors, while drafting them after the trigger point incurs no penalty. This feature further amortizes the sensing overhead and increases the SRAM yield when normal SRAM cells fail due to either process variation or aging mechanisms.

3. PROPOSED SENSOR DESIGN

Without loss of generality, we first focus on NBTI. Fig.1(a) shows the sensor designed for NBTI tracking. The sensor is essentially an asymmetric 6T SRAM cell with its own power supply (VDDS) separate from that for normal SRAM cells. One load transistor (P1) is designed stronger than the other (P2). The sensor works in two modes: *tracking* (when the sensor tracks the NBTI degradation) and *polling* (when new sensing results are obtained). Notice that sensors in the system do not need to be all synchronized or even in the same mode.

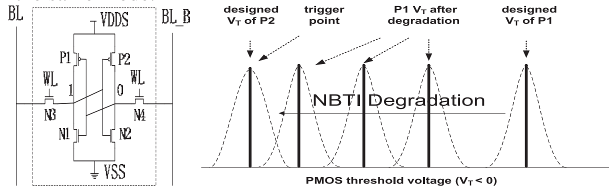

Figure 1: (a) Proposed sensor design. P1 is sized up to be stronger than P2 initially. Essentially an asymmetric SRAM cell with separate power supply. The sensor stores '1' in this figure. (b) NBTI degrades the stronger P1 over time. The solid lines are nominal design parameters and the dashed lines illustrate the effect of process variation. Notice that P1 and P2 may have different distributions.

In the polling mode, the sensor is disabled shortly by collapsing its word line (WL) and VDDS to 0 for one or several clock cycles. While still keeping WL=0, restoring VDDS starts a fight between the two cross coupled inverters. Disabling the sensor ensures the fight starts fresh for both inverters. Intuitively, when P1 is stronger than P2, the fighting favors P1 and the sensor ends up storing '1', and vice versa. Although the polling mode involves several steps, they can be performed asynchronously in several or tens of clock cycles. The recovery effect can be ignored since we are targeting long term NBTI aging effect over years.

The sensor naturally enters the tracking mode after polling. Here the sensor holds the polling result that can be read out anytime before the next polling. Initially with a stronger P1 the polling ends up with '1', putting P1 under NBTI stress in the following tracking stage. As time goes on NBTI negates the strength difference, eventually changing the polling result to '0', at which point we say the sensor *triggers*. This process is illustrated in Fig.1(b).

At the sensor trigger point P1 and P2 become equally strong and the sensor can act as a symmetric 6T cell. In fact this is probably exactly when some SRAM cells start to fail due to BTI. Thus the SRAM array lifetime can be extended as the sensor cells gradually replace failed cells through address mapping.

Fig.1(b) also shows the effect of process variation. A subtle but critical point is that at the trigger point P1 and P2 do not necessarily have the same strength, as the fighting during polling involves all

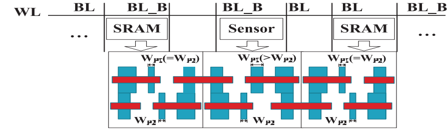

Figure 2: Sensor layout and deployment. Cells are properly mirrored to reflect realistic physical design.

transistors subject to variation. This will be discussed later. Previous work [3, 9] show that to achieve reasonable sensing precision in the presence of variation, thousands of sensors may be required.

By maximally reusing the existing SRAM peripheral circuitry, sensing and data collecting do not require much beyond what an SRAM block already offers. For example, when VDD in SRAM is routed in columns, Fig.2 shows a possible sensor organization to have easy centralized control of the VDDS signal for multiple sensors. The sensor layout can be simply designed by taking an SRAM cell layout and increasing the P1 width while maintaining the cell height, as shown in the bottom of Fig.2. In this way the cells in neighboring columns experience the same physical geometries as if a normal SRAM column were inserted, and the introduced layout perturbation and systematic process variation are minimized.

The discussion above can be adapted easily for a PBTI dominant technology. In Fig.1(a), N2 can be sized up instead of P1, and the sensor still triggers when the polling result flips from '1' to '0'. If PBTI and NBTI effects are comparable, we can track the combined effects, which is a useful worst case, since the two BTI degradation often happen together and add up. For example, in an SRAM cell the PMOS and NMOS on different sides are always stressed concurrently both hurting noise margins. The same happens to the PMOS and NMOS in neighboring stages and both pull-up and pull-down are slowed down affecting the logic path delay. In this case, both P1 and N2 in our sensor need to be sized up proportionally. The sizing up ratio should be determined by both technology and usage characterization, similar to guardband calculation.

4. SYSTEM DESIGN METHODOLOGY

The main question to answer is how to achieve the highest sensing precision with the smallest sensor area. *Precision* is defined as the variation of the trigger point (TP). The sensor precision (σ) is limited by process variation. Define the *system trigger point* (μ_S) as the mean of all sensor trigger points. The system precision (σ_S) is decided by both individual sensor precision and the number of sensors (N_S). This section first studies the tradeoff between N_S and σ, then presents the system design flow.

4.1 Trading Off Sensor Size with Number

The variability of a transistor is inversely proportional to its channel area (WL), therefore to improve system precision (σ_s) one could increase either individual sensor size (A_{sen}) or N_S. Here increasing a sensor size means upsizing all transistors in the sensor by the same ratio, and we further assume the sensor area is increased by this ratio as well. A perfect tradeoff is observed in [3], suggesting the system precision σ_S remains constant with either option if the same total sensor area (A_S) is maintained. Now we show this conjecture to be mathematically sound.

THEOREM 1. *Under the following assumptions, the variation of a sensor system (σ_S) remains unchanged if the total sensor area (A_S) remains constant:*

(i) parameter variation of one sensor follows $\sigma^2 \propto \frac{1}{\Sigma WL} \propto \frac{1}{A_{sen}}$;

(ii) parameter variation of different sensors are independent;

PROOF. Let x denote a sensor parameter with mean μ and standard deviation σ. x_i denotes the parameter of the ith sensor with mean μ_i and standard deviation σ_i.

First consider a system (S1) comprised of only one big sensor with size A_S, so the system is the sensor itself: $\mu_{S1} = \mu_0, \sigma_{S1}^2 = \sigma_0^2$. Notice that no assumption is made on the distribution of x.

Consider another system (S2) comprised of n small equally sized sensors whose area sum up to A_S. The mean of x from all sensors $\bar{x} = \sum_i^n x_i/n$ is a random variable and

$$\sigma_{\bar{x}}^2 = E(\bar{x} - E\bar{x})^2 = \frac{E(\sum_i^n x_i - E\sum_i^n x_i)^2}{n^2} \quad (1)$$

$$= \frac{\sum_i^n E(x_i - Ex_i)^2}{n^2} + \frac{\sum_i^n \sum_{j,j\neq i}^n E(x_i - Ex_i)(x_j - Ex_j)}{n^2} = \frac{\sum_i^n \sigma_i^2}{n^2} \quad (2)$$

The last equality comes from assumption (ii) on independence. From assumption (i) we have $\sigma_i^2 = n\sigma_0^2$, thus $\sigma_{S2}^2 = \sigma_{S1}^2$. Further consider another system (S3) comprised of sensors of different sizes and number from S2. With the same procedure one can show $\sigma_{S3}^2 = \sigma_{S1}^2$. Therefore σ_S only depends on the A_S. Q.E.D. □

The sensor system design consists of two related steps: designing μ_S and σ_S. Theorem 1 essentially decouples these two steps, since μ_s can be built into each sensor and σ_S can be calibrated by adjusting N_S. The most convenient A_{sen} can be chosen and the optimum is guaranteed from Theorem 1. These two steps are further described in the following.

4.2 Sensor Design with Required Trigger Point

To design a sensor with desired trigger point we begin by transistor sizing. The following discusses NBTI sensors but PBTI sensor design follows the same way. Intuitively the V_T or I_D ratio of P1 and P2 can be tuned. However both are difficult to measure. More importantly, the polling result is not solely decided by the relative strength of P1 and P2, but also depends on other transistors which are affected by process variation. For example, sensors with the same P1/P2 ratio but different N1/N2 ratio will trigger differently. Therefore we need a better metric that captures variation of all transistors to enable us to design for a specific TP.

Since the sensor is essentially an asymmetric SRAM cell, the polling tells whether '0' or '1' is more easily held by the cell. The hold static noise margin (SNM) provides exactly what we are looking for! Define SNM_0 and SNM_1 as the SNM for holding '0' and '1'. As P1 is stressed by NBTI and P0 remains unstressed, SNM_1 decreases and SNM_0 improves. Fig.3(a) shows the simulation results of an SRAM cell designed in a commercial 90nm technology.

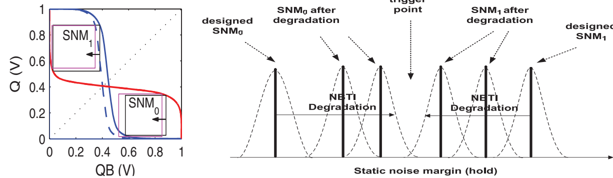

Figure 3: (a) NBTI decreases SNM_1 and increases SNM_0, eventually causing the sensor to trigger. The solid and dashed curves show the VTC curves before and after stress respectively. (b) Sensor trigger mechanism described by SNM. The solid lines are nominal values and the dashed lines illustrates the effect of process variation. Notice that SNM_0 and SNM_1 can have different standard deviations.

Following this observation we design $SNM_1 > SNM_0$ by a certain ratio $r(r>1)$ initially. Overtime NBTI offsets the difference and the sensor triggers when they become equal, as illustrated in Fig.3(b). Moreover, Section 6 will show that both SNM_0 and SNM_1 change almost linearly with ΔV_T. Therefore, once the degradation threshold is specified, r can be found by simulation or table look-up.

4.3 System Design with Required Precision

A study on how N_S affects the system precision is carried out in [9]. In reality directly obtaining the mean lifetime of all sensors after they trigger is impractical as the degradation must have already exceeded the pre-defined threshold. Fortunately both SNM_1 and SNM_0 are normally distributed [12, 13], so (SNM_0-SNM_1) also follows a normal distribution, for which the mean equals the median. So μ_S can be found when half of sensors have triggered.

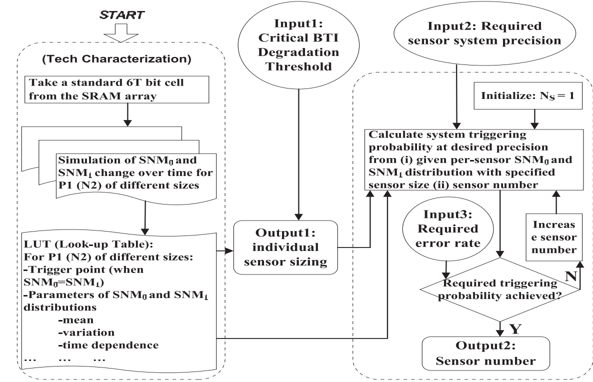

Figure 4: Sensor system design methodology. Steps in the left box only need to be done once for a given SRAM design per technology. Steps in the right box can be performed in less than 20 lines of Matlab code.

The sensor TP can be adjusted by r, and its variation is decided by the SNM_0 and SNM_1 distributions at TP. The system TP equals the mean of all sensor trigger points. Once the sensor precision is known, the system precision σ_S, which is a design specification, can be calibrated by N_S according to Theorem 1. The system design flow is shown in Fig.4 and will be exemplified in section 6.

5. WHAT HAPPENS AFTER TRIGGERING

The use of sensors goes far beyond just issuing an 'abandon chip' signal. For example V_{DD} increase and forward body biasing can be used to mitigate BTI [6, 10]. In particular, for SRAM array we can replace the defect cells with the sensors or other redundant cells, or switch the cell contents [11]. Since both NBTI and PBTI degrade SRAM cell read stability, read assist methods can be applied.

We do not necessarily want to wait until the circuit fails to apply the above techniques, especially for aging mechanisms like BTI that can at least partially recover themselves. Dynamic reliability management [8] has been proposed on the architecture level and can be applied through the entire circuit lifetime. The proposed sensing system can be employed to predict a single or multiple critical points during the circuit lifetime, thus providing vital information for high level reliability management.

Since BTI partially recovers itself when the stress bias is removed, the sensors can be revived after rest for some time. This can be exploited to reuse sensors. For example, to provide more continuous degradation information, instead of deploying multiple sensor systems for multiple critical points, we may only need two sensor systems and activate them alternatively. These are left for future work.

6. SIMULATION RESULTS

The following designs and simulations are based on a commercial 90nm bulk technology. We only target NBTI as currently it is still the dominant degradation. Since both SNM_0 and SNM_1 are normally distributed and remain so after NBTI degradation [12, 13], their mean values can be approximated by nominal values. The mean μ_k and deviation σ_k of $SNM_k (k = 0,1)$ are functions of NBTI degradation stress ΔV_T and SNM ratio r. ΔV_T can be translated directly into stress time. In the following, we go through the major steps in Fig.4 to design a sensor system that predicts the 112mV ΔV_T NBTI degradation with 4mV precision. These numbers are relatively large and only for illustration purposes.

We first focus on steps in the left box in Fig.4. The goal here is to derive the look-up table (LUT). Starting from a standard SRAM cell, we sweep P1 width to find out how the distributions of SNM_0 and SNM_1 shift. For PMOS of different sizes, the mean of ΔV_T due to NBTI is the same, but variation may differ [12]. While this could be easily incorporated into $\sigma_k(\Delta V_T)$, it is observed in [13] that this additional variance is overwhelmed by the initial variation

Table 1: Sample Look-up Table in Fig.4 (only f=2 is filled)

f	μ_0(mV)	μ_1(mV)	v_0	v_1	$\sigma_0(mV)$	$\sigma_1(mV)$
2	309.0	355.7	0.174	-0.243	11	10
1.9	...	...	...	...	...	...

at t=0. Based on this observation and the lack of these technology parameters, we assume the normal distributions keep their initial variance as they shift, i.e., $\sigma_k(\Delta V_T) = \sigma_k(0)$.

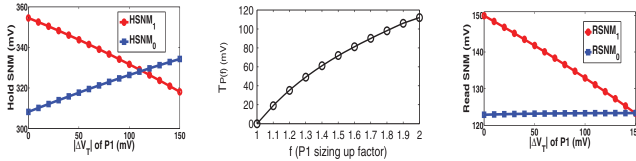

Figure 5: (a) SNM$_0$ and SNM$_1$ mean value change with ΔV_T of P1 when W$_{P1}$=2W$_{P2}$. (b) Degradation trigger point as a function of f. (c) Read SNM0 and SNM1 vs ΔV_T when f=2.

Another variable affecting μ and σ is the SNM ratio r. Although r can be affected by all transistors in the sensor, for simplicity we only size up P1 from the original SRAM cell, and denote f=W$_{P1}$/W$_{P2}$ (r is a function of f). Fig.5(a) shows that with f=2, μ_0 and μ_1 converge at ΔV_T=112mV, the desired trigger point. Even though f only denotes the sizing up factor of P1, other transistors are implicitly captured in SNM. Interestingly, both μ_0 and μ_1 change almost linearly with ΔV_T. The errors are less than 0.2%(for SNM$_0$) and 0.3%(SNM$_1$) with linear fitting. The linear behavior is observed throughout our simulations with different f. Denote $v_0(f)$ and $v_1(f)$ as the fitting slopes of μ_0 and μ_1, the trigger point

$$TP(f) = \frac{\mu_1(f,\Delta V_T=0) - \mu_0(f,\Delta V_T=0)}{|v_1(f)| + |v_0(f)|} \qquad (3)$$

In Fig.5(a) $v_0(f) = 0.174$ and $v_1(f) = -0.243$.

μ, σ and v are all we need for f=2. Repeating this process, we can fill the LUT in Fig.4 for other f as shown in Tab.1. The LUT would incorporate more parameters if SNM does not change linearly or σ changes with ΔV_T. Fig.5(b) plots $TP(f)$ in our design. The LUT can be obtained through SNM simulations, NBTI models or a one-time technology characterization.

While hold stability decides polling results, read stability is needed for both sensor and normal data reading since we want sensors reconfigurable as functional SRAM cells at any point. Fig.5(c) shows how NBTI affects read static noise margins (RSNM). RSNM$_0$ depends much more on P2 than P1 thus changes very slowly. The sensitivity of RSNM$_1$ is much smaller compared to the hold SNM, because read only depends weakly on the pull up PMOS but much more strongly on the pull down and access NMOS which do not experience NBTI (but PBTI). Nonetheless, the read noise margins remain positive, ensuring read capability during the entire lifetime.

Parameterized cell layout can be designed for sensors of different sizes and f. The sensors maintain the same height as original SRAM cells. The SRAM cell designed for this technology is around $1.7\mu m^2$. The sensor area overhead roughly equals $0.058(f-1)$. For example, if we design for TP=50mV (which is still more than 10% of the original V$_T$) f is found to be 1.3 from Fig.5(b) and the sensor is only 1.7% larger in area than an SRAM cell. The increased PMOS size is essentially the guardband that would be built into all SRAM cells in a worst case based margining approach. The area overhead ratio is (cell number)/(sensor number)×2 (2 PMOS gates per cell). If we build 1Kb such sensors for a 1Mb SRAM, the area overhead is roughly 0.0017% plus control signals, versus 3.4% of the worst-case design, an almost 2000× reduction.

Finally we calculate N_S to achieve the required 4mV sensing precision: $P(trigger) = P(SNM_0 > SNM_1) = P(SNM_0 - SNM_1 > 0)$ (P denotes the event probability). (SNM$_0-$SNM$_1$) is also normally distributed due to the normally distributed SNM$_0$ and SNM$_1$. $P(trigger)$ can be calculated from ΔV_T and N_S:

$$P(trigger) = \Phi\left(\frac{(\mu_0-\mu_1) + \Delta V_T\cdot(v_0-v_1)}{\sqrt{(\sigma_0^2+\sigma_1^2)/N_S}}\right) \qquad (4)$$

Φ is the cdf of the standard normal distribution. We first calculate

Table 2: Error Rate for System Precision=4mV and f=2

sensor num.	100	500	1000	1500	1500	1500	5000
precision(mV)	4	4	4	4	2	1	1
error rate(%)	26.3	1.23	0.0401	1.46e-3	3.06	2.82	4.74

$P(trigger)$ at ΔV_T=(112-4)mV=108mV of one sensor. The trigger is false positive as the designed TP(112mV) is not reached yet. Plug values from Tab.1 and N_S=1 in Eq.(4) yielding $P(trigger)$=0.46. $P(trigger)$ drops to 0.006 with N_S=500. $P(trigger)$ at 116mV (false negative) can be calculated similarly, or skipped due to the symmetry of normal distributions. Therefore with 500 sensors and 4mV precision, the system error rate is 0.006×2=1.2%, meaning with 98.8% confidence level the system triggers within the required precision. Tab.2 shows diminishing returns for large N_S. Interestingly the results are on par with [9] where using 1000 sensors achieves 10% precision with 95% confidence level for oxide breakdown.

Even if the σ of SNM changes due to NBTI caused ΔV_T or others reasons like technology improvement, the system TP will not change, as long as the mean values remain the same. However, $P(trigger)$ at other points would change so the system precision and error rate need recalibration with updated Tab.1.

7. CONCLUSIONS AND FUTURE WORK

We have presented an on-chip BTI sensor system. The sensors are embedded in SRAM arrays but can track both NBTI and PBTI degradation for combinational and memory circuits. Physical layout and deployment are discussed. We show that the sensors introduce very small area and control overhead and minimum perturbation to the SRAM layout. They can even improve SRAM yield since they can function as SRAM cells. When SRAM cells fail due to variation or aging, the sensors can act as replacements. By introducing static noise margins to characterize the triggering of sensors, process variations from all sources are captured and sensor precision is better calibrated. On the system side, the related impacts of individual sensor parameters and the total sensor number are investigated, and a perfect tradeoff is mathematically proven under certain assumptions. We derive a complete design methodology from this tradeoff. With simulation results in a commercial technology, we demonstrate how the system parameters should be designed to meet a user specification. The number of sensors required is consistent with other work. The BTI sensors can be used for high level reliability management, and techniques to mitigate BTI degradation, especially for SRAM, are also discussed.

8. ACKNOWLEDGMENT

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