Dynamic Write Limited V_{MIN} for Nanoscale SRAMs

DATE 11

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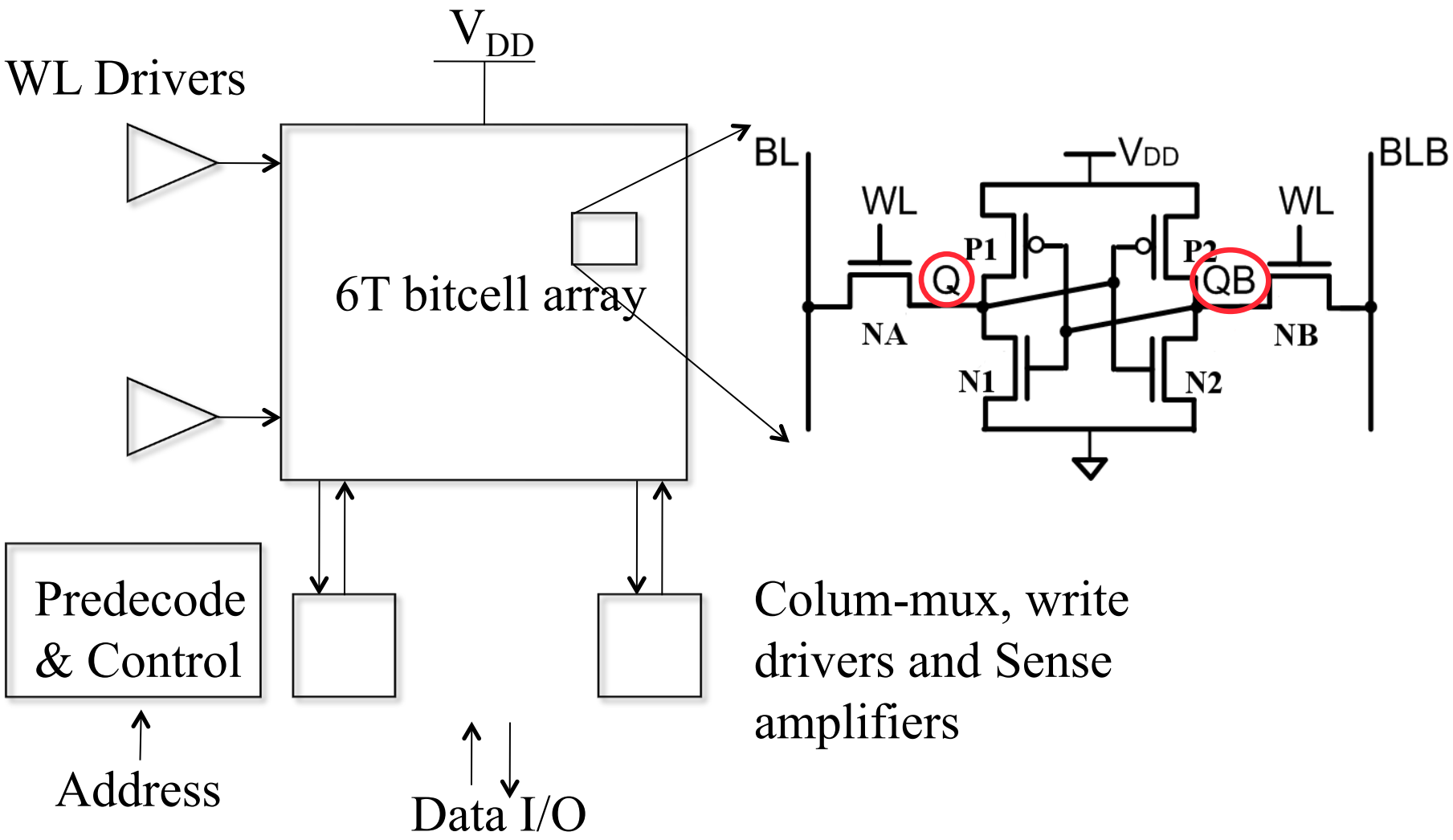
Overview

- **Background and motivation**
- Metrics
  - Dynamic writability metric: $T_{WL\text{-}CRIT}$
  - Dynamic write V_{MIN}: DWV_{MIN}
- Factors affecting DWV_{MIN}
  - WL pulse characteristics
  - Memory size
  - No: of cycles prior to first read
  - Bitcell parasitics
- Effect of Write Assist
- Conclusions

Background & Motivation



Background & Motivation

Low standby and dynamic power → reduce SRAM supply voltage (V_{DD})

V_{MIN} = Min. V_{DD} at which SRAM can hold, read and write correctly

SNM assumes DC → optimistic or pessimistic for R-W failure and V_{MIN} prediction

V_{MIN} prediction based on dynamic stability needed.

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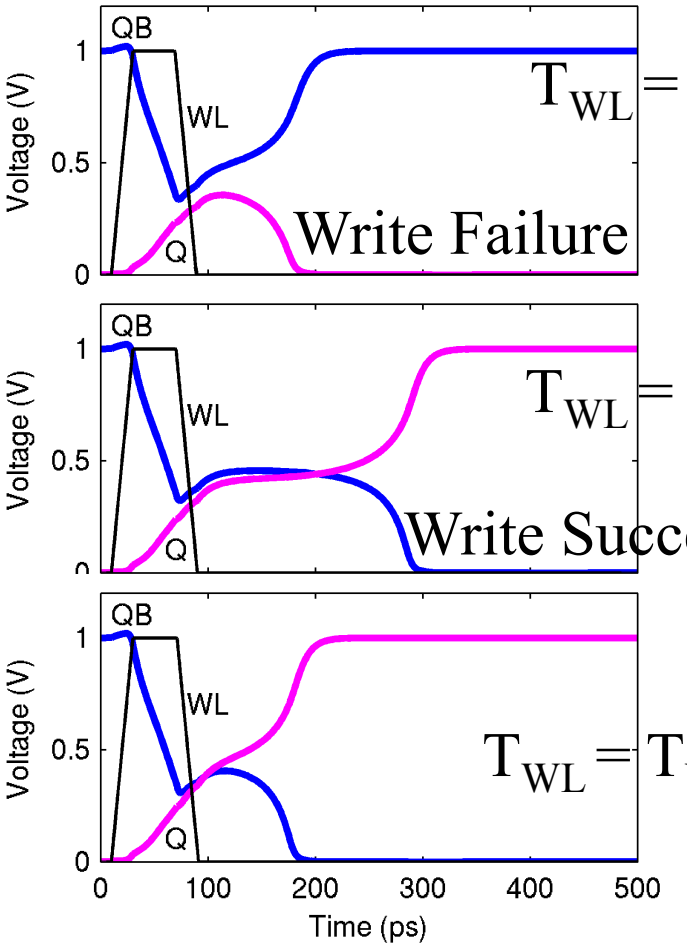
$T_{WL\text{-}CRIT}$

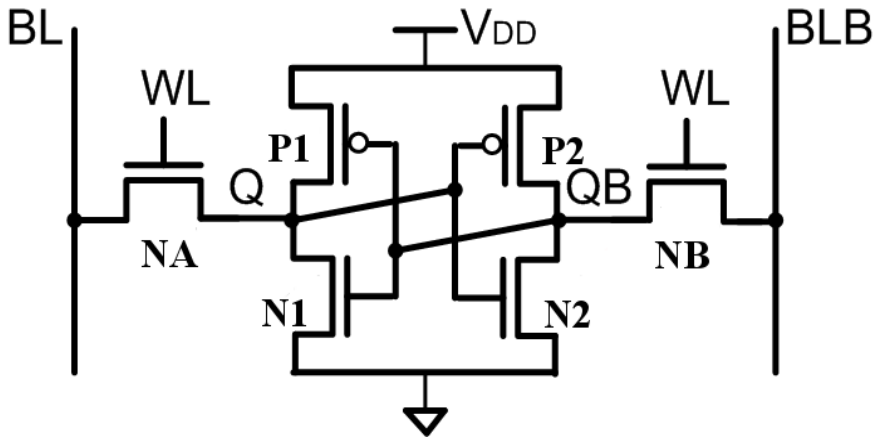
$T_{WL\text{-}CRIT}$ = Minimum WL pulse width for successful write



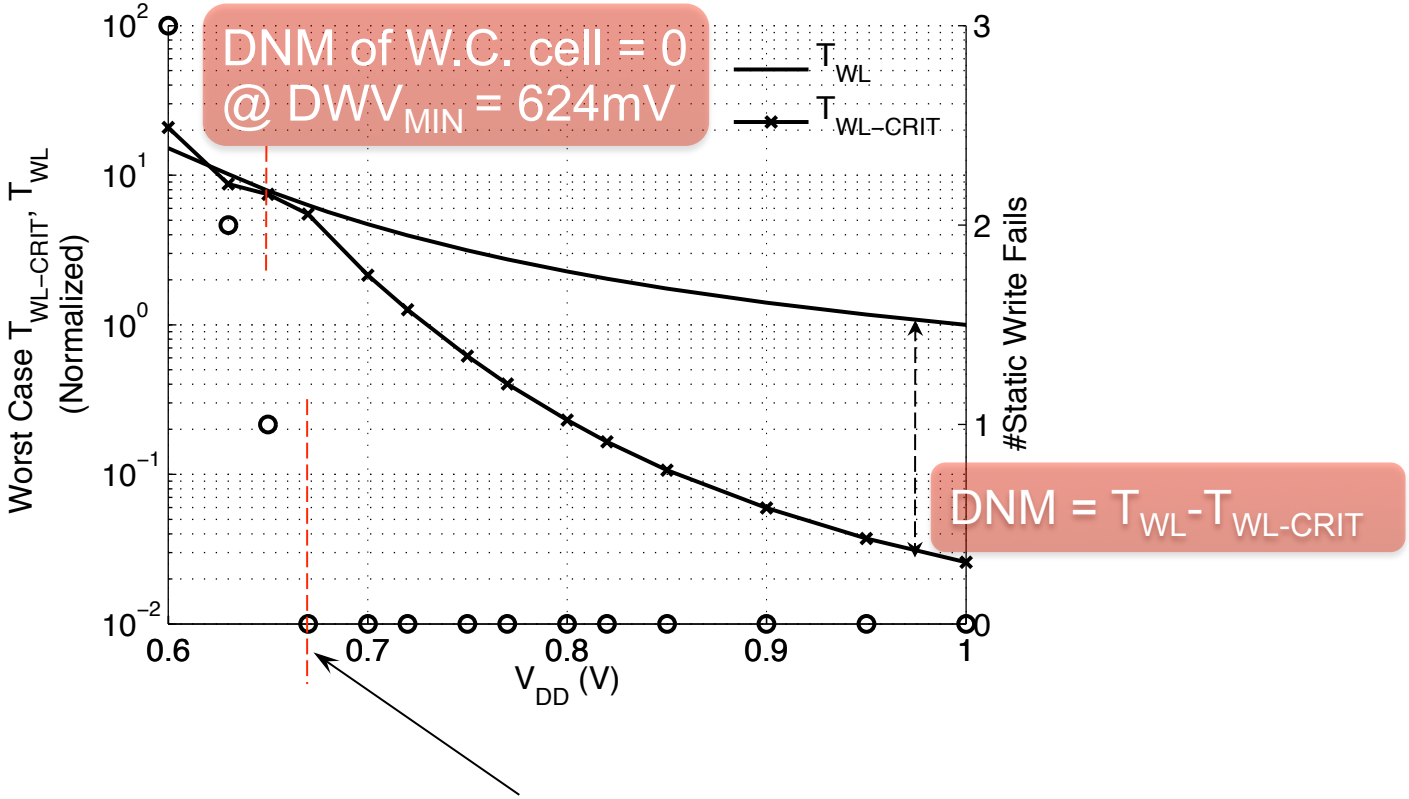
$T_{WL} = T_{WL\text{-}CRIT}$ - 1ps

$T_{WL} = T_{WL\text{-}CRIT}$

$T_{WL} = T_{WL\text{-}CRIT}$ + 1ps



DWV_{MIN}



Static Failures start ➔ Static V_{MIN} @ 670 mV

Static Failure ➔ Cannot write with ∞ WL

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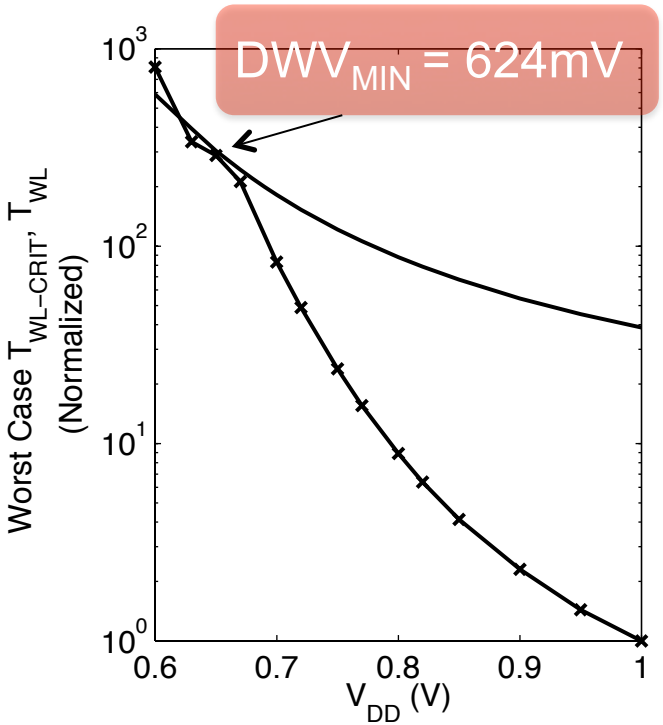
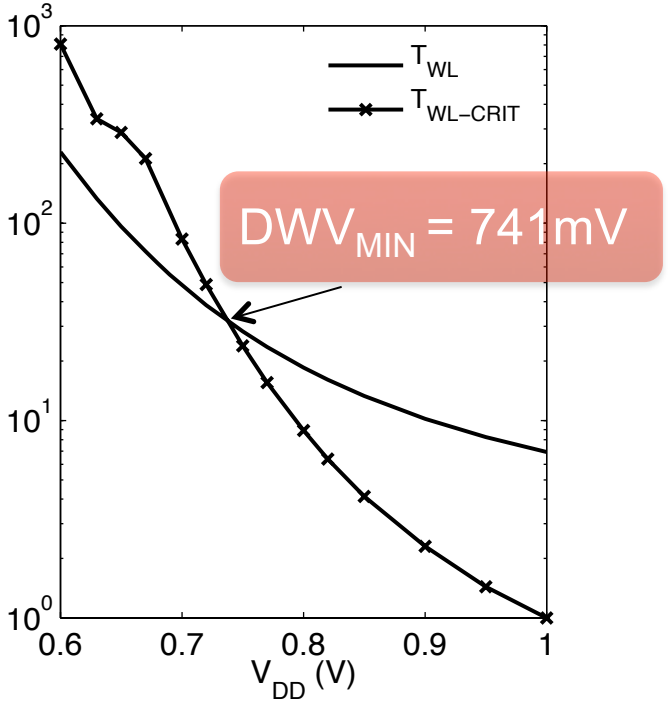
Factor 1: WL pulse characteristics

WL pulse generated using replica timing path

More aggressive WL pulse enough for developing fixed ∂V_{BL}





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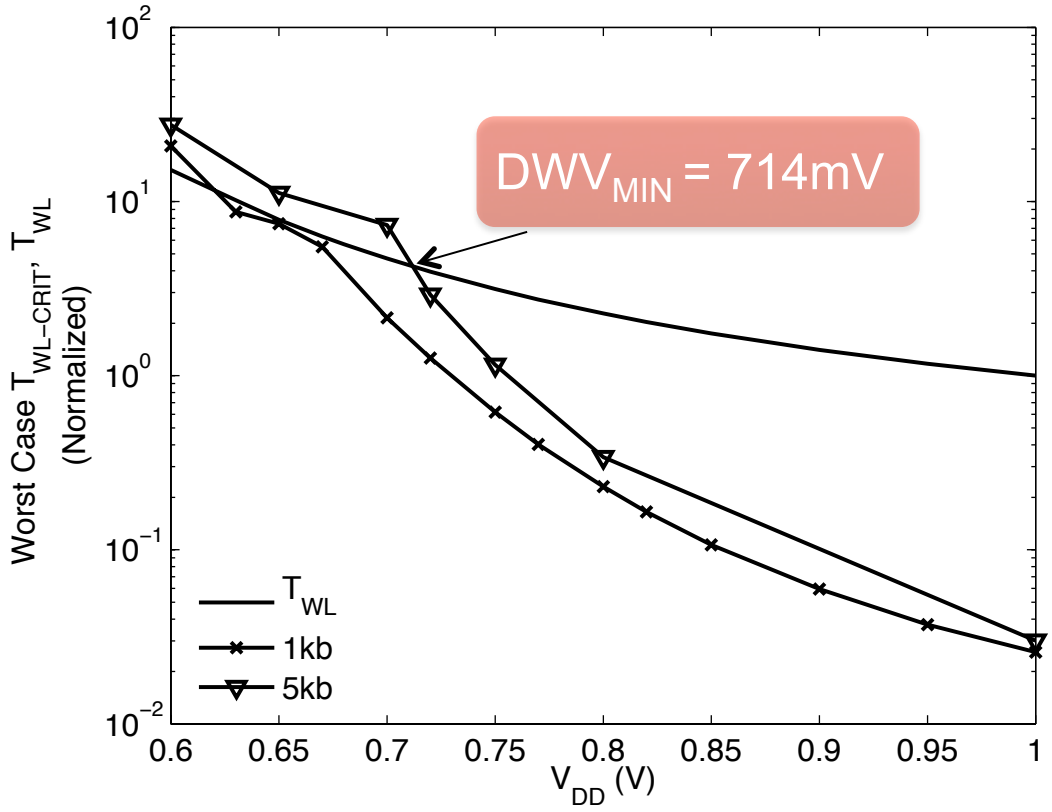
Factor 2: Memory size

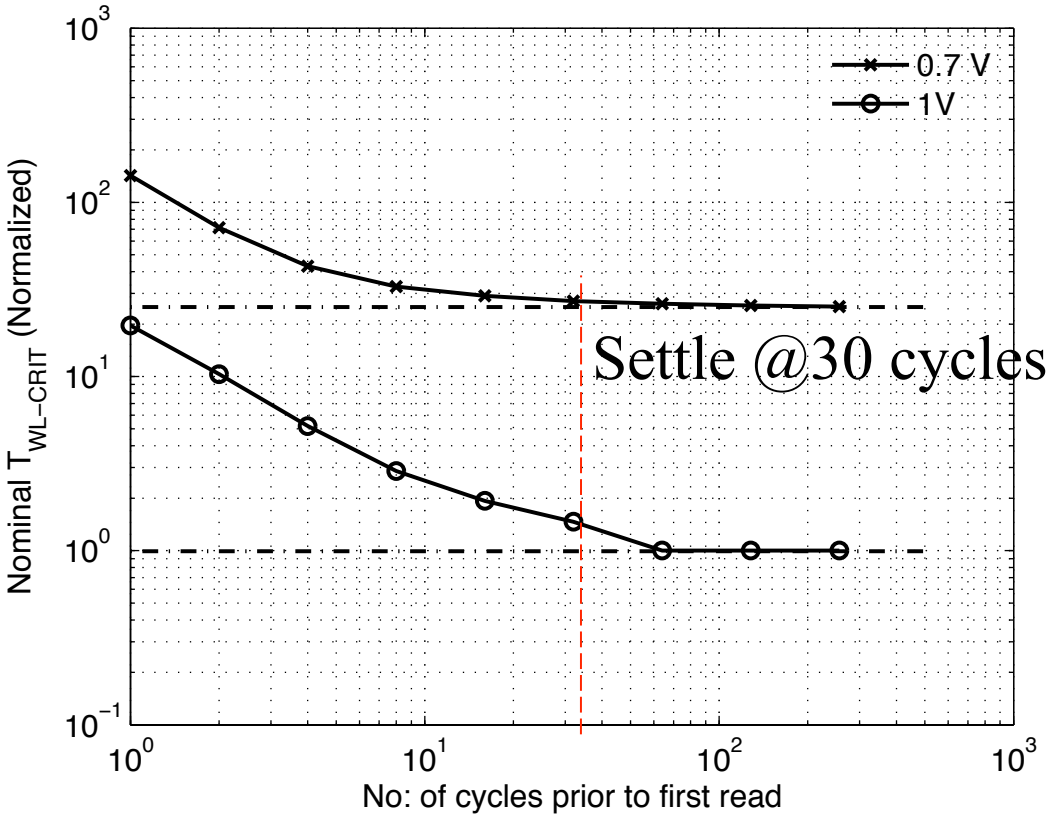


Larger Capacity

Worst case cell farther out in tail of DNM distribution

Higher DWV$_{MIN}$

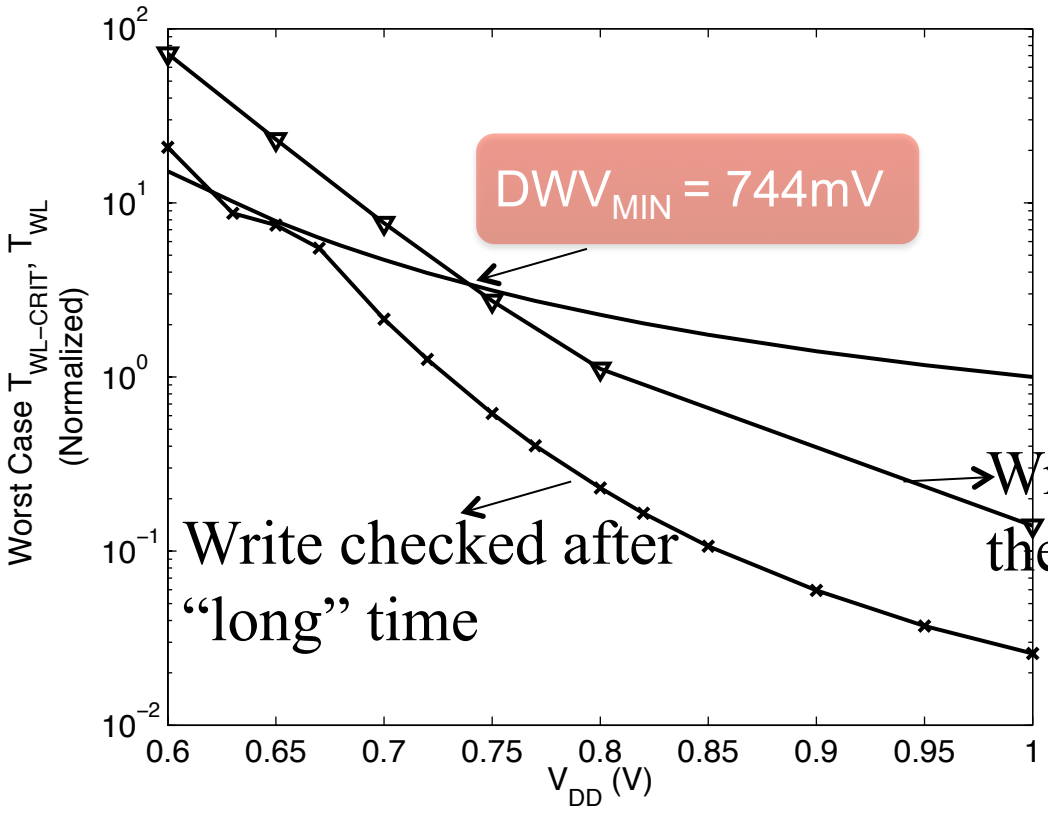
Factor 3: Cycles prior to first read



$T_{WL-CRIT}$ depends on failure definition

Stricter ➔ higher value

Factor 3: Cycles prior to first read



Stricter Failure Criterion

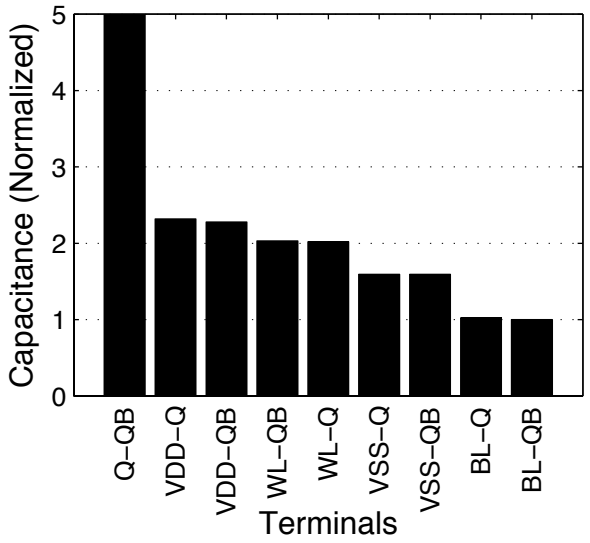
↓

Higher W.C. $T_{WL-CRIT}$

↓

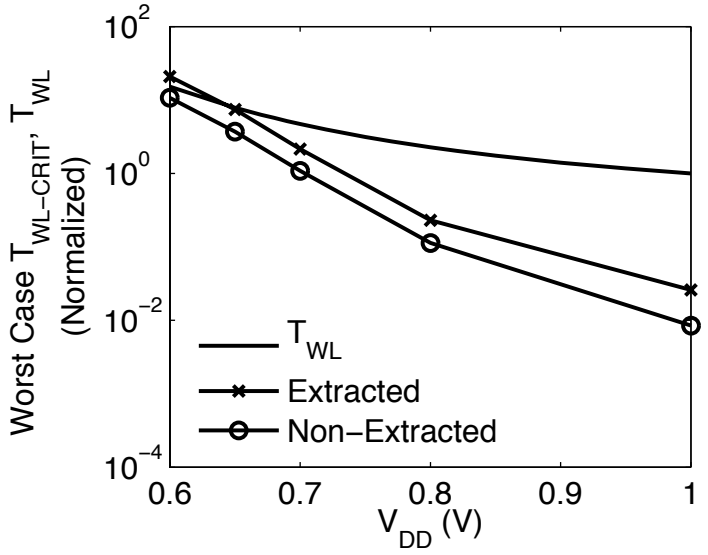
Higher DW_{VMIN}

Factor 4: Bitcell parasitics



Inter-storage node capacitance dominates

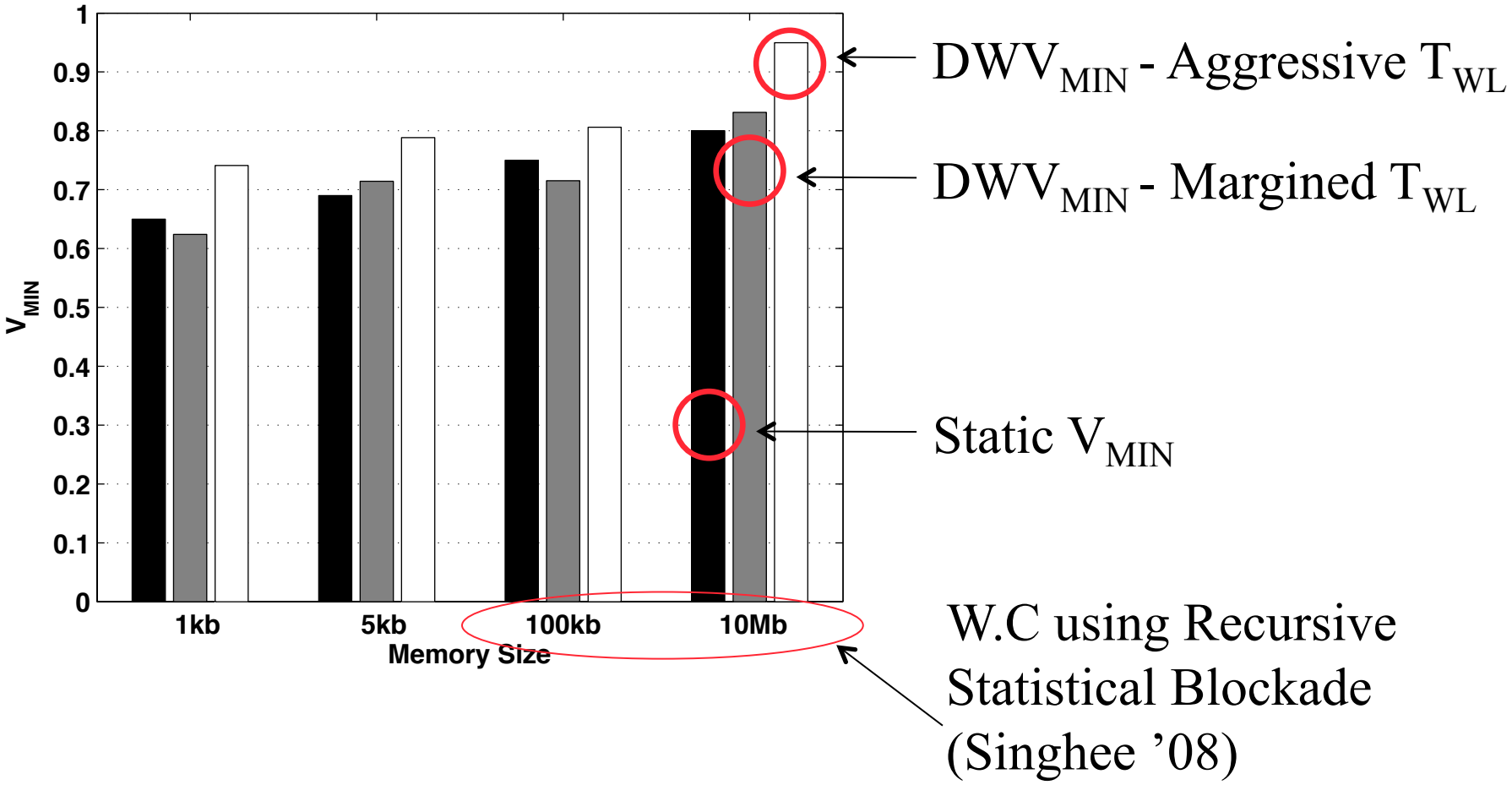
Higher $C_{Q\text{-}QB}$ ➔ harder to flip



Ideal bitcell ($C_{Q\text{-}QB} = 0$) has lower DWV_{MIN} than extracted one

Static vs. Dynamic V_{MIN}

DWV_{MIN} dominates Static V_{MIN} if T_{WL} is aggressive



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- **Effect of Write Assist**
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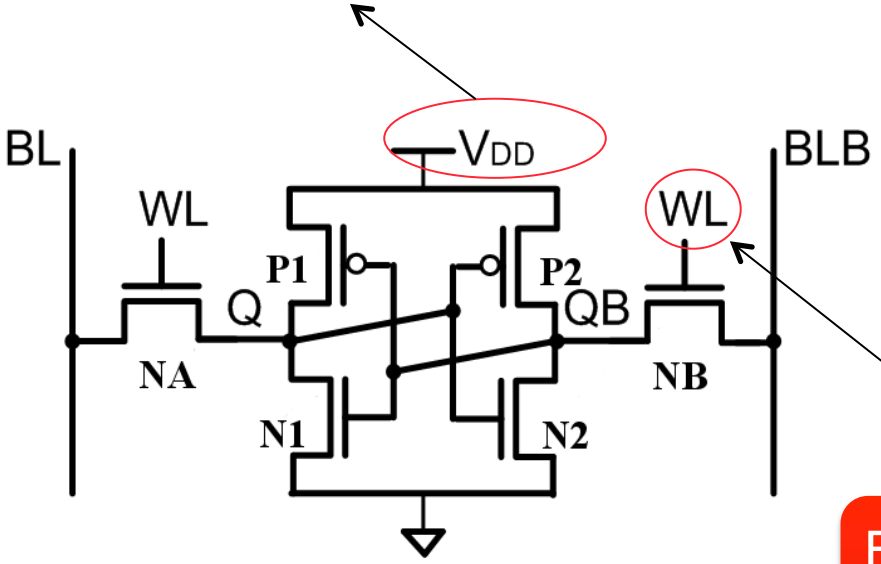
Write assists for improving DNM

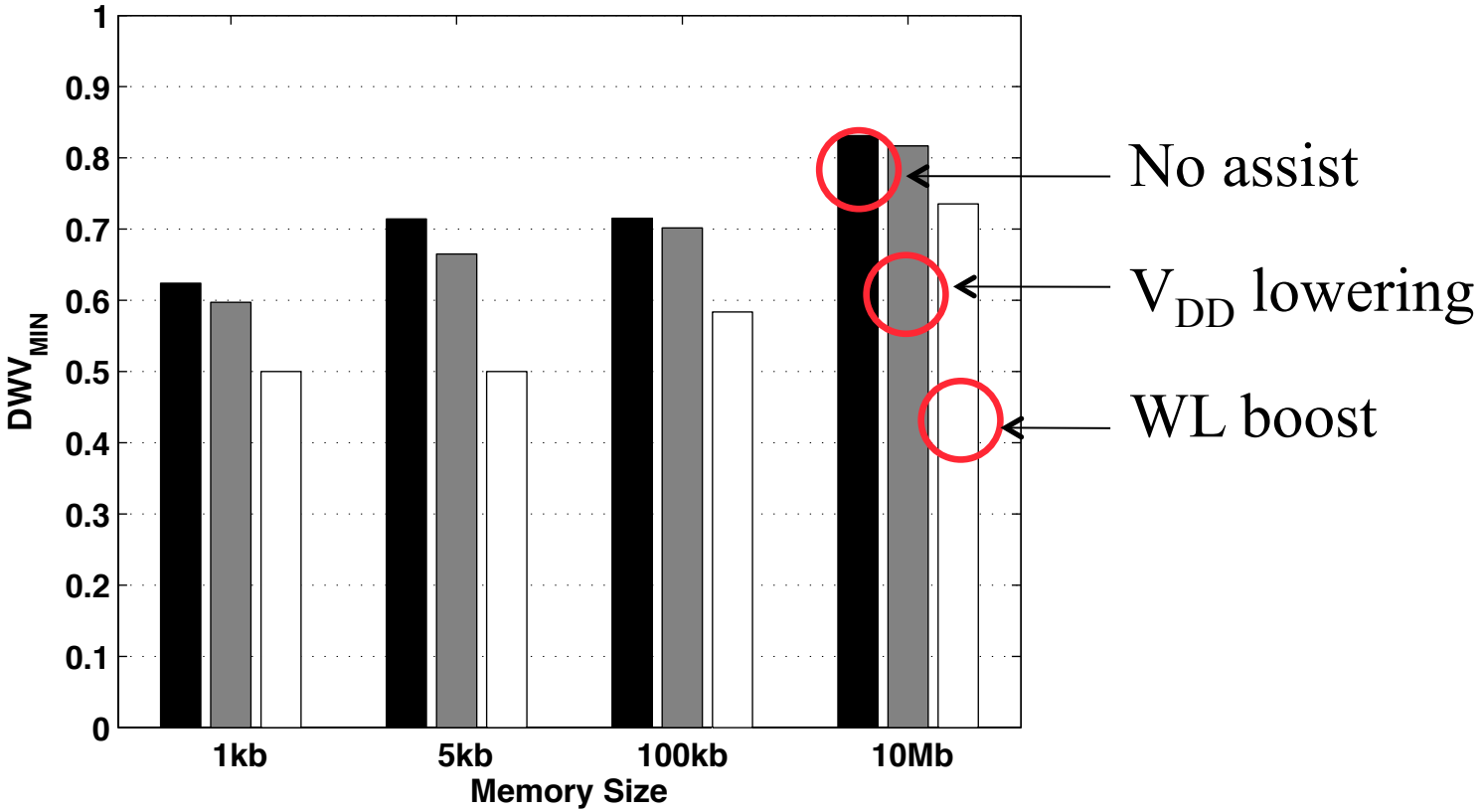
Collapse V_{DD} ➔ Weaken cell feedback



Boost WL ➔ Increase injected current

Effect of Assists on DWV_{MIN}

WL boost better than V_{DD} lowering for reducing DWV_{MIN}



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Conclusions

- Defined V_{MIN} based on dynamic stability for write-limited SRAM.
- Investigated factors affecting DWV_{MIN}.
- Analyzed impact of write assists on DWV_{MIN}.
- Future work
  - Further investigate factors affecting dynamic stability alone.
  - Attempt to determine and model a relationship between dynamic and static metrics and V_{MIN}.

Thank You!

Questions?

BACKUP SLIDES

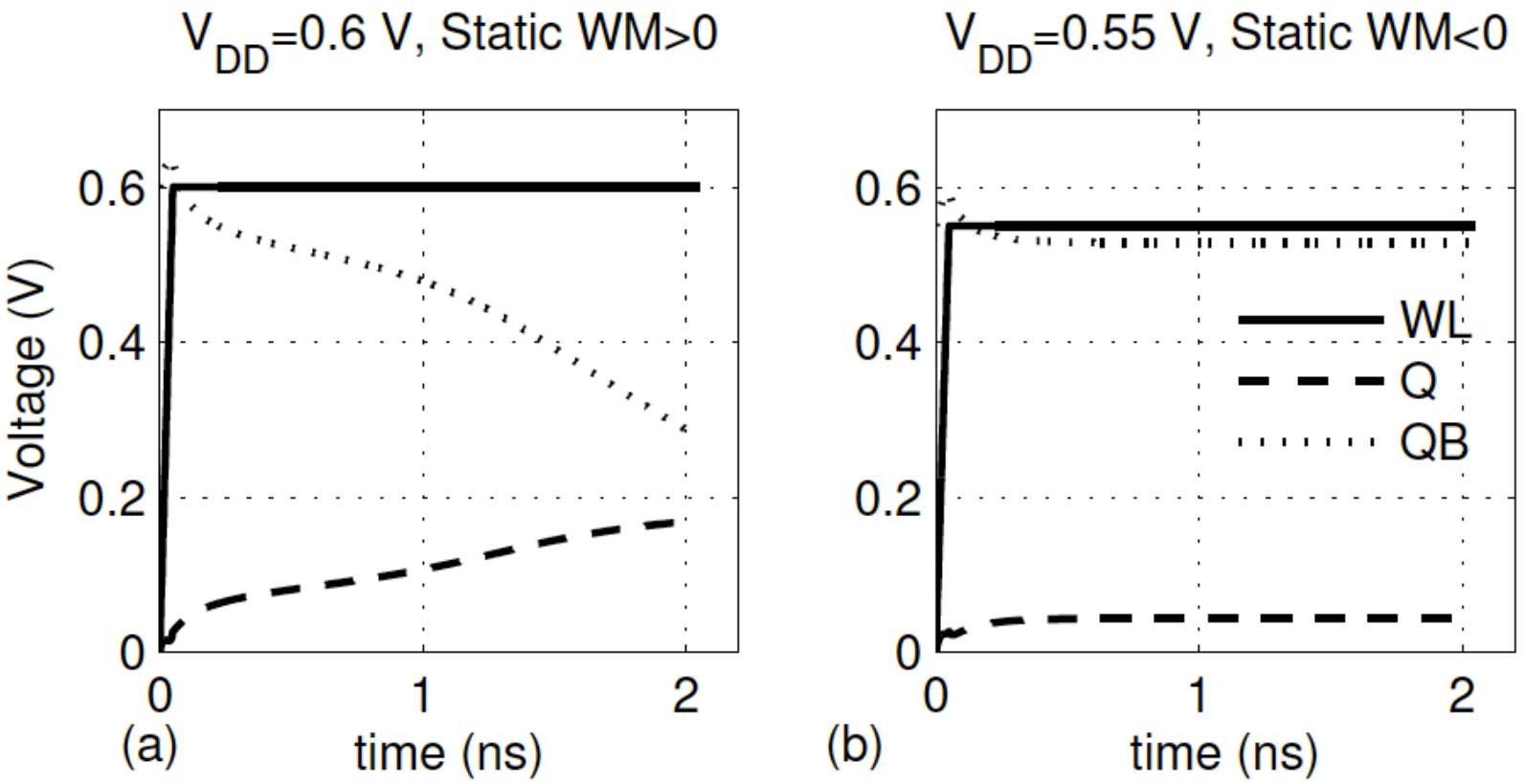
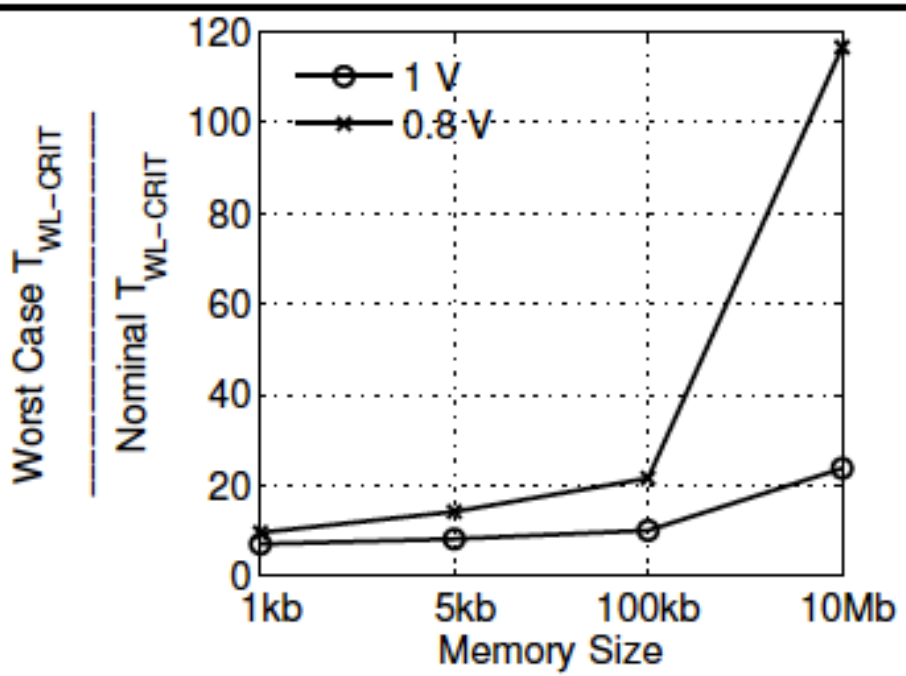
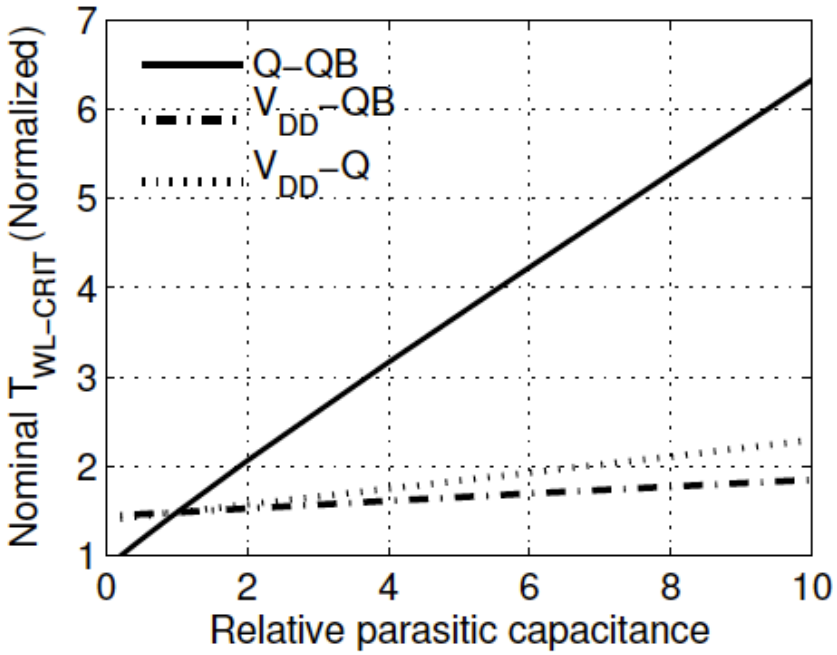

V_{DD}=0.6 V, Static WM>0
V_{DD}=0.55 V, Static WM<0
Voltage (V)
0.6
0.4
0.2
0
0
1
2
time (ns)
(a)
(b)
WL
Q
QB

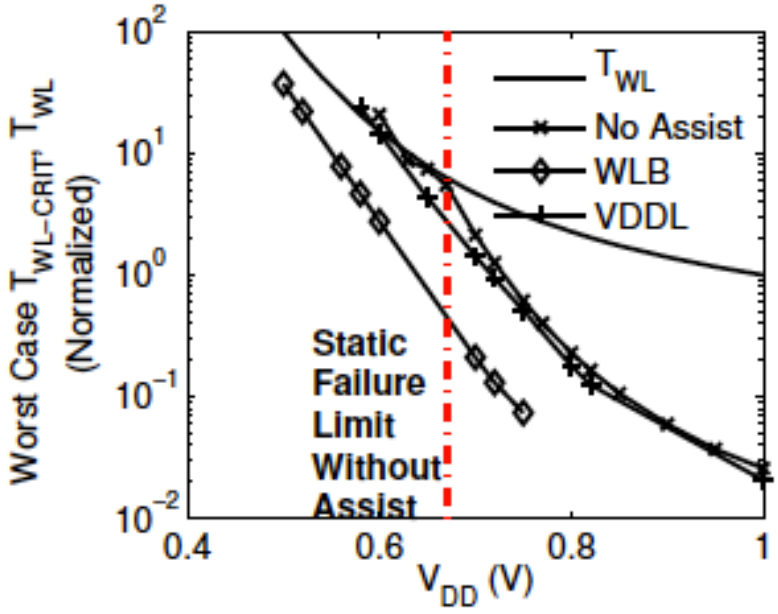
TABLE II

V_T OFFSETS FOR STATIC AND DYNAMIC WRITE FAILS

	PD0	PD1	PU0	PU1	PG0	PG1
1 V	0.0286	0.0332	-0.0245	-0.1294	-0.0258	0.1263
0.6865 V	0.0286	0.0332	-0.0245	-0.1294	-0.0258	0.1263




Q–QB
V_{DD}–QB
V_{DD}–Q
Nominal $T_{WL-CRIT}$ (Normalized)
Relative parasitic capacitance
1
2
3
4
5
6
7
0
2
4
6
8
10


Worst Case $T_{WL-CRIT}$, T_{WL} (Normalized)
10^2
10^1
10^0
10^{-1}
10^{-2}
0.4
0.6
0.8
1
V_{DD} (V)
T_{WL}
No Assist
WLB
VDDL
Static Failure Limit Without Assist