Modeling and Analysis of Power Supply Noise Tolerance with Fine-grained GALS Adaptive Clocks

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Robust
Low
Power
VLSI

Outline

- Problem: Power supply noise

- Existing solution

  - Traditional adaptive clocking scheme

  - Drawbacks

- Proposed solution: Fine-grained GALS adaptive clocking

- Quantification of benefits

  - Experimental setup

  - Simulation results

- Summary

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Problem: Power Supply Noise

Chip

Package

Board

Package De-cap

BGA Package

Bulk Capacitor

Chip

PCB De-cap

VRM
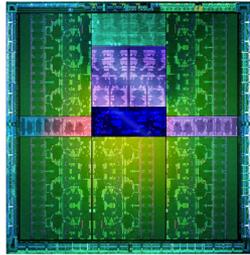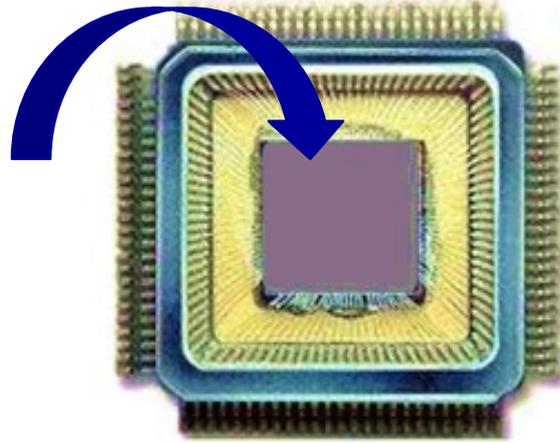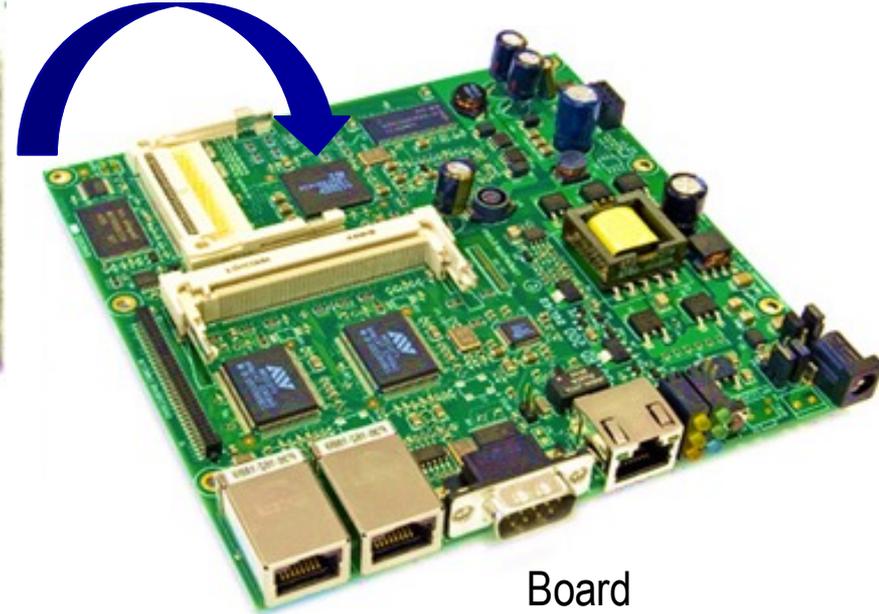
Power

Ground
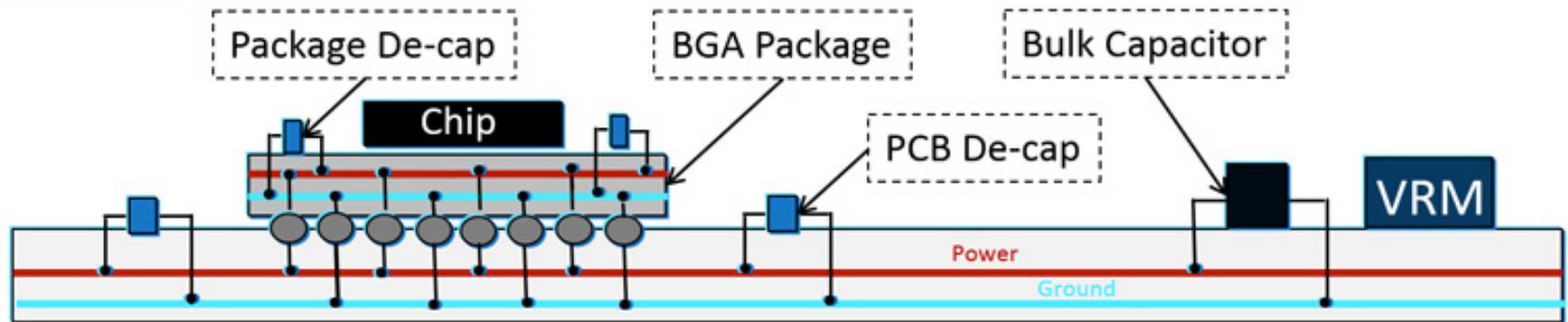
Problem: Power Supply Noise
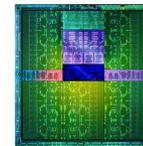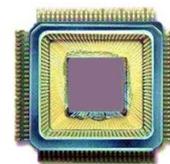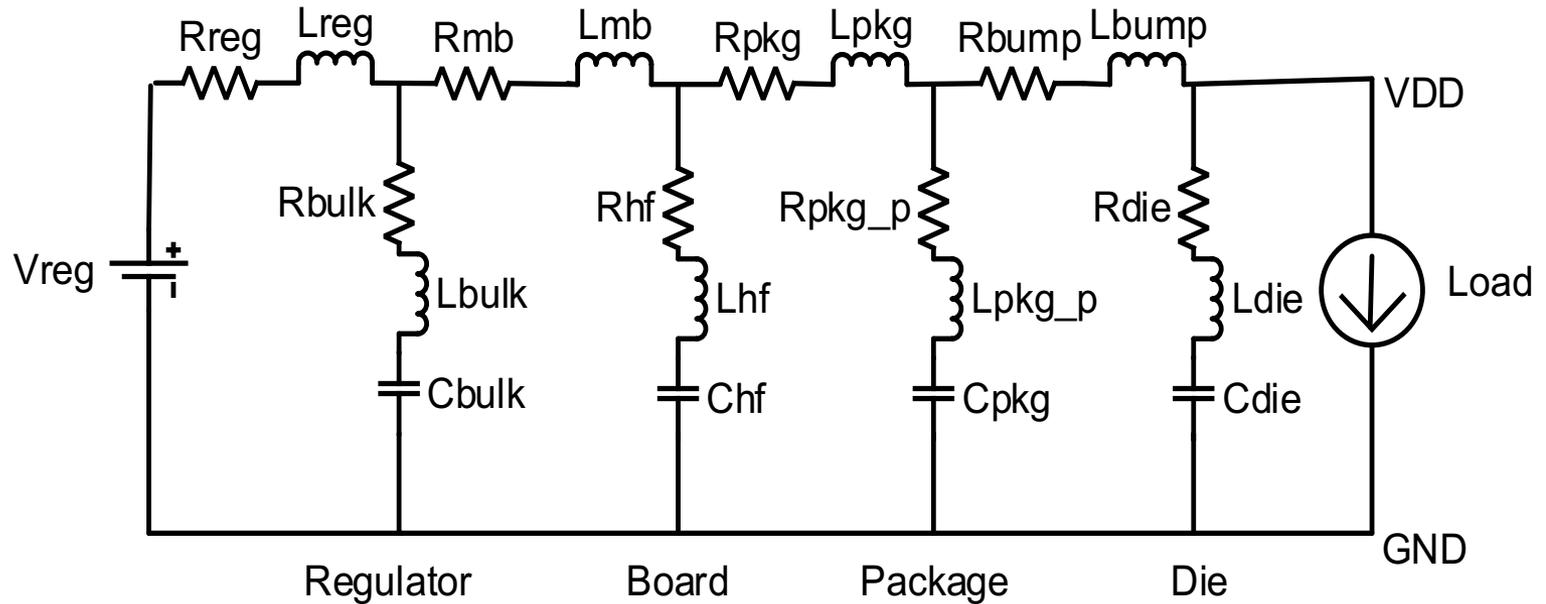
Parasitics ➔ power supply noise !!!

Problem: Power Supply Noise

- Resistive component ➜ IR drop
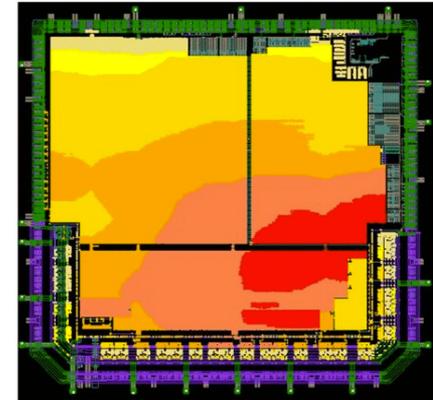
- Reactive component ➜ LdI/dt droop
  First, second, third droop . . .

Problem: Power Supply Noise

Nominal

Droop

Data path   Slows down
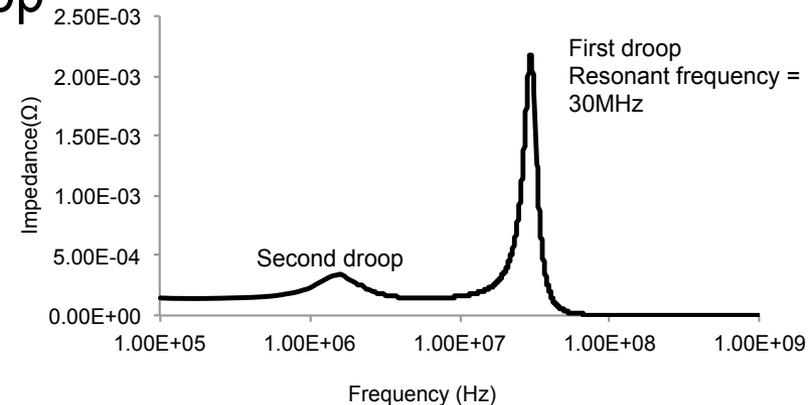
Clock

Frequency remains same
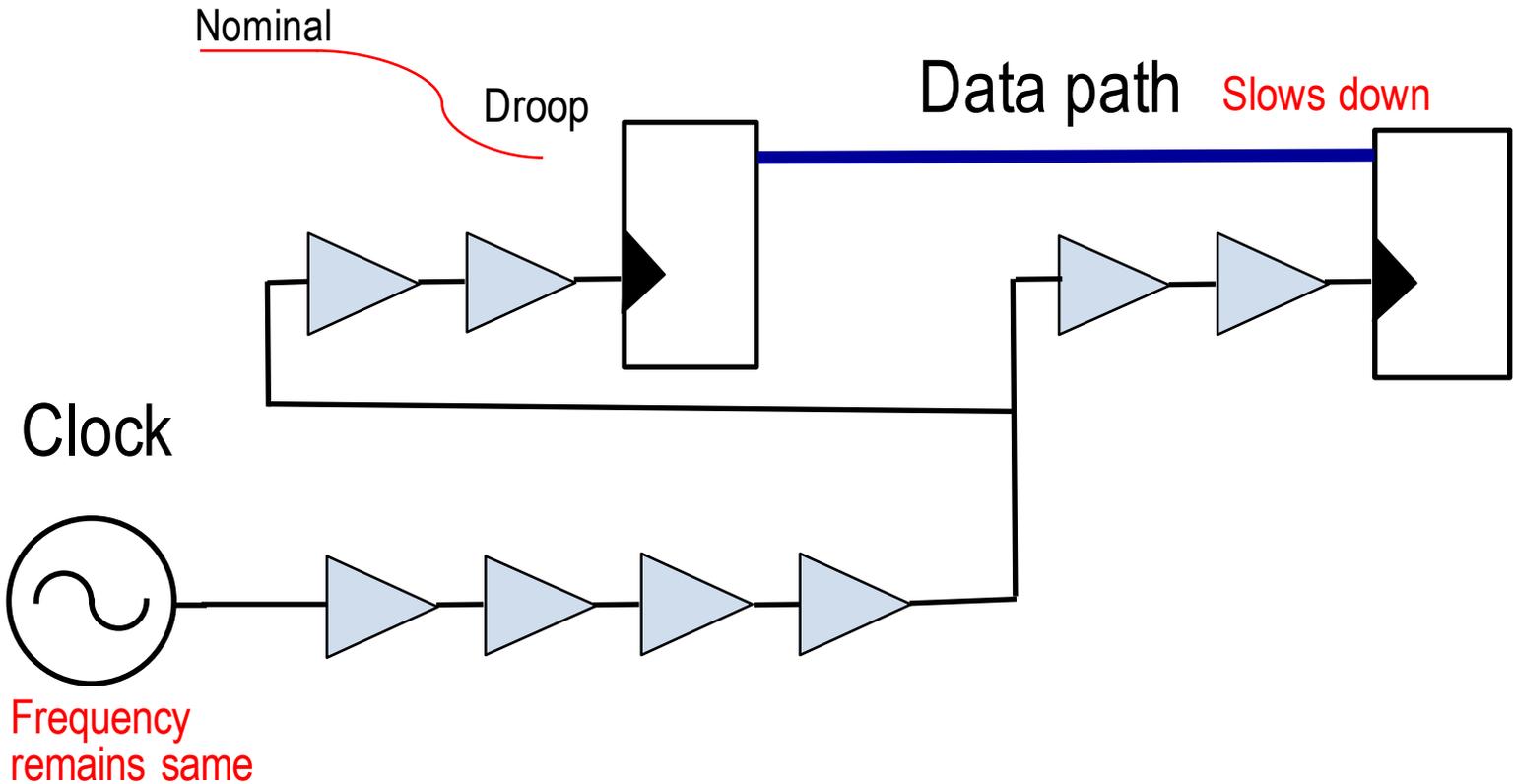
Supply noise ➜ timing errors ➜ performance degradation.

Operate at frequency that can handle worst-case noise !!!

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# Existing Solution: Traditional Adaptive Clocking

- Adaptive clocking [1][2]

Voltage rail
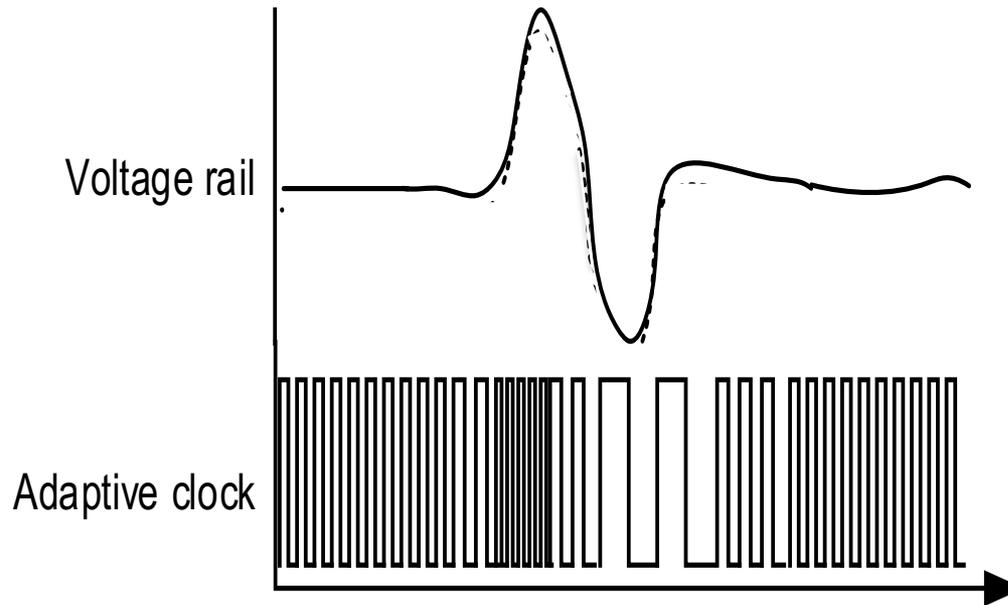
Adaptive clock

Frequency tracks voltage !!!

Existing Solution: Traditional Adaptive Clocking

- Fixed clocking vs. Adaptive clock

Voltage rail

$F_{max-adaptive\ clock}$

$F_{max-fixed\ clock}$

Fixed clock

Tolerates worst-case noise

Adaptive clock

Frequency tracks voltage noise
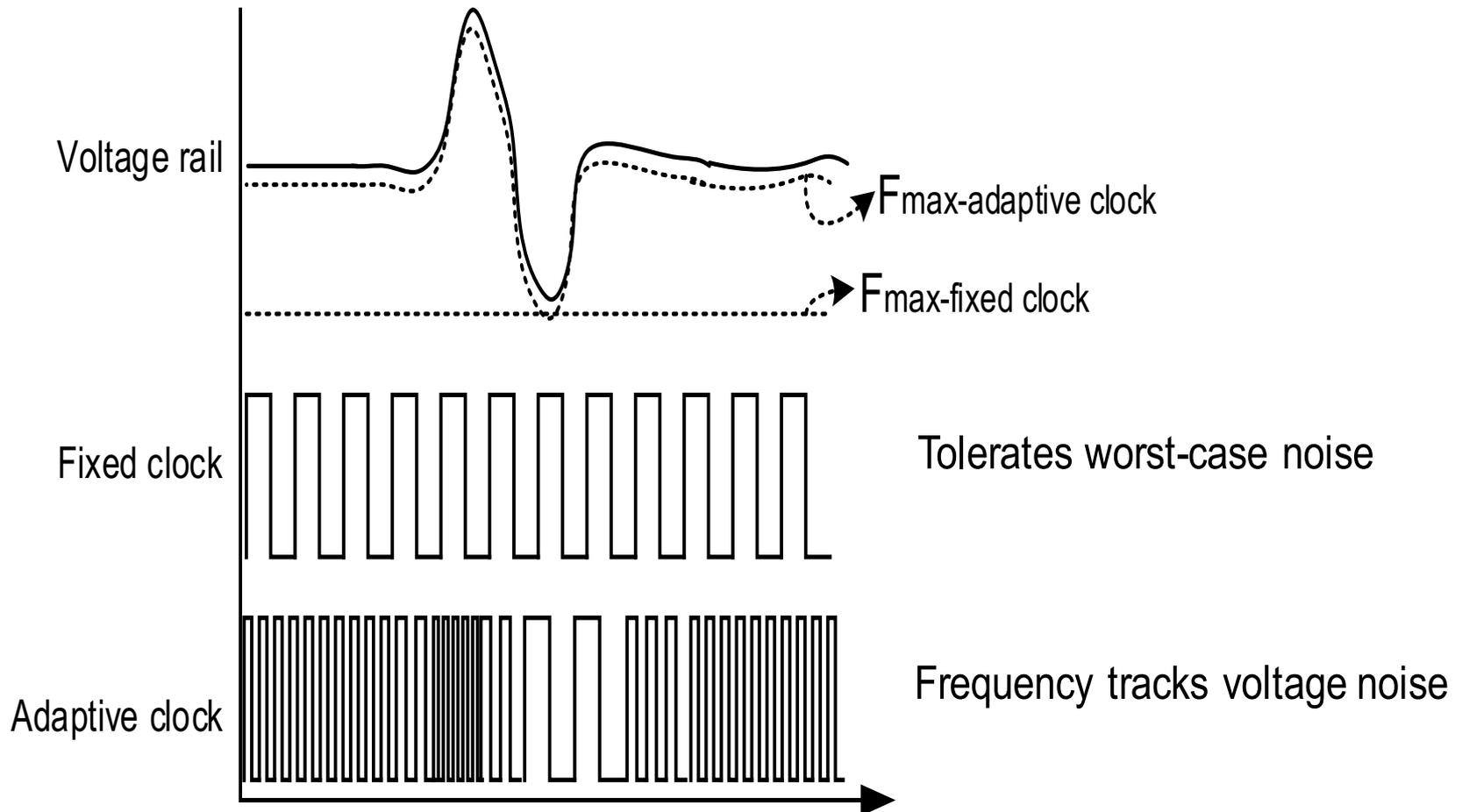
Metric: Uncompensated Voltage Noise (UVN)

Uncompensated voltage noise UVN = $V_{mean} - V_{req}$

V_{mean} : available voltage, averaged over a clock cycle

V_{req} : required voltage (for operation of circuits at required frequency)

When $V_{mean} > V_{req,}$ no problem !!!

When $V_{mean} < V_{req}$ ➔   additional margin for failure-free operation (UVN)

Lower UVN ➔ lower margin

Lower UVN is better!!!

Existing Solution: Traditional Adaptive Clocking

- Fixed clocking vs. Adaptive clock

Fixed clock
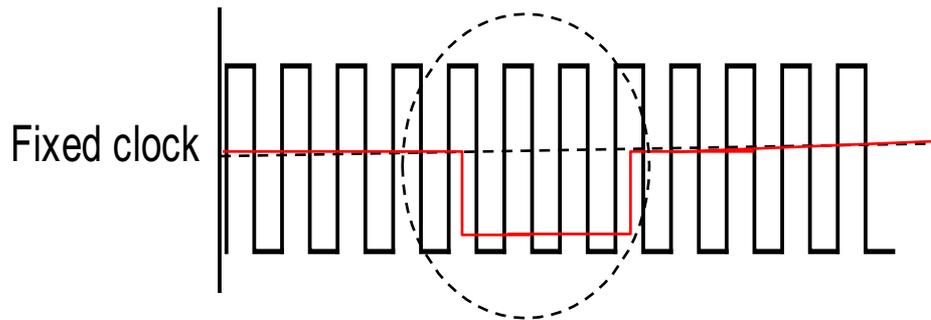
Adaptive clock

Voltage droops: voltage available (V_{mean})

Voltage corresponding to fixed frequency (V_{req})

**UVN = V$_{mean}$ – V$_{req}$**
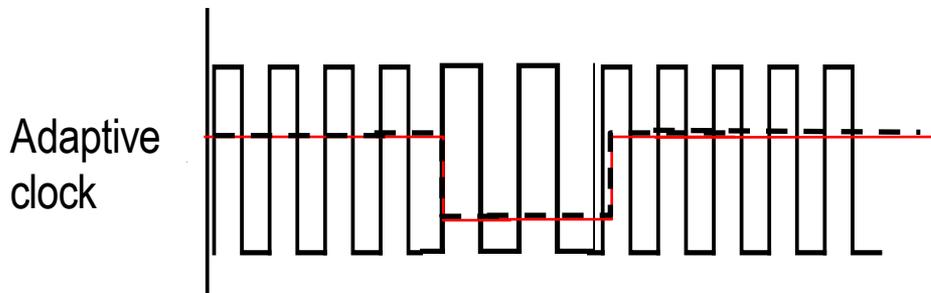
Voltage droops: voltage available (V_{mean})

Voltage corresponding to adaptive frequency (V_{req})

**UVN = 0 (expected)**

Adaptive clocking is a great solution !!!

Drawbacks: Traditional Adaptive Clocking

- Large chips with a few clock domains
- But each clock domain is still many mm^2
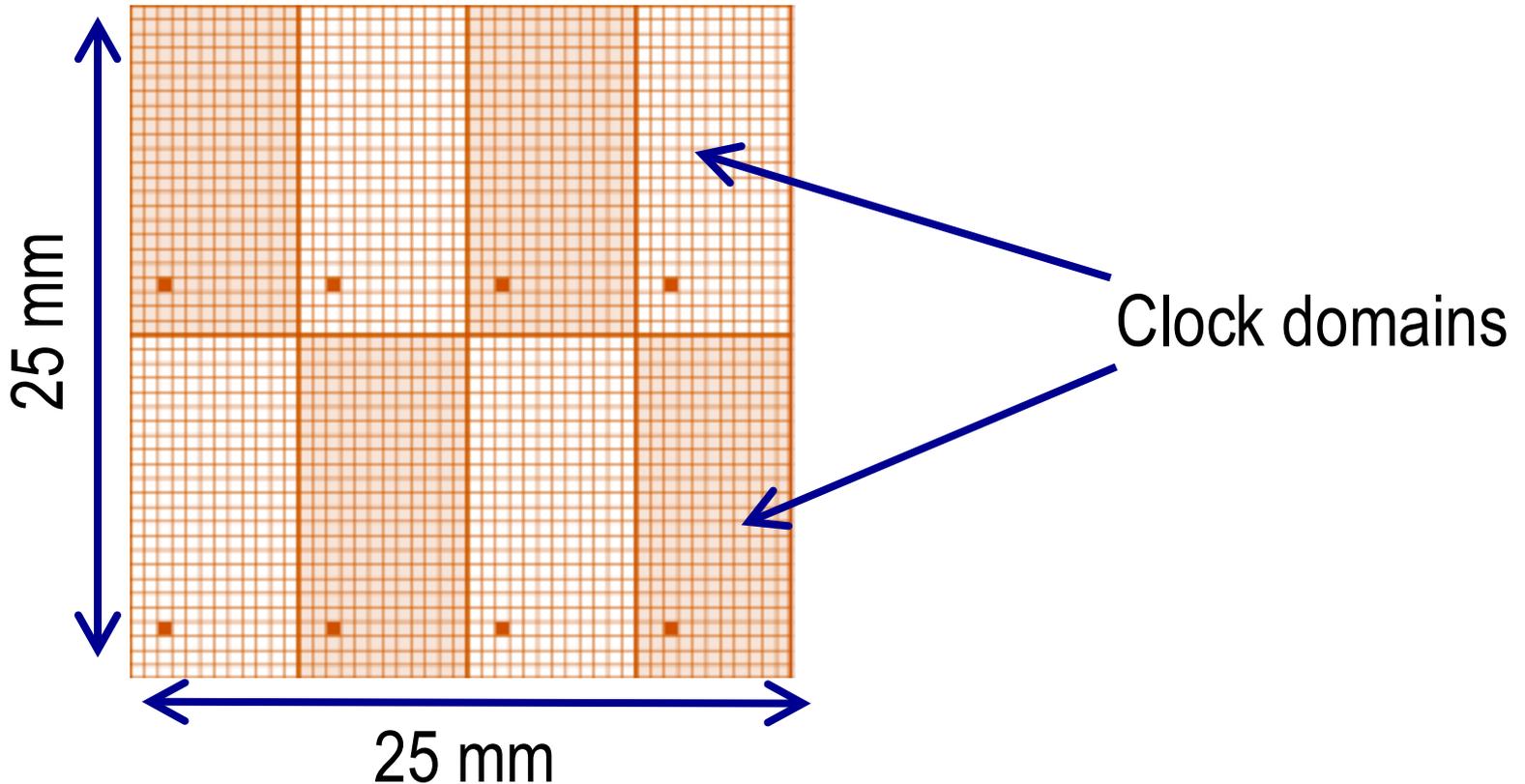
25 mm (vertical)

25 mm (horizontal)

Clock domains

Drawbacks: Traditional Adaptive Clocking

Drawback #1: Effect of Clock-tree Insertion Delay

Clock

Root

Insertion Delay

Leaf

Drawbacks: Traditional Adaptive Clocking

Drawback #1: Effect of Clock-tree Insertion Delay

Voltage

Clock – root

Clock – leaf

Δt

Δt
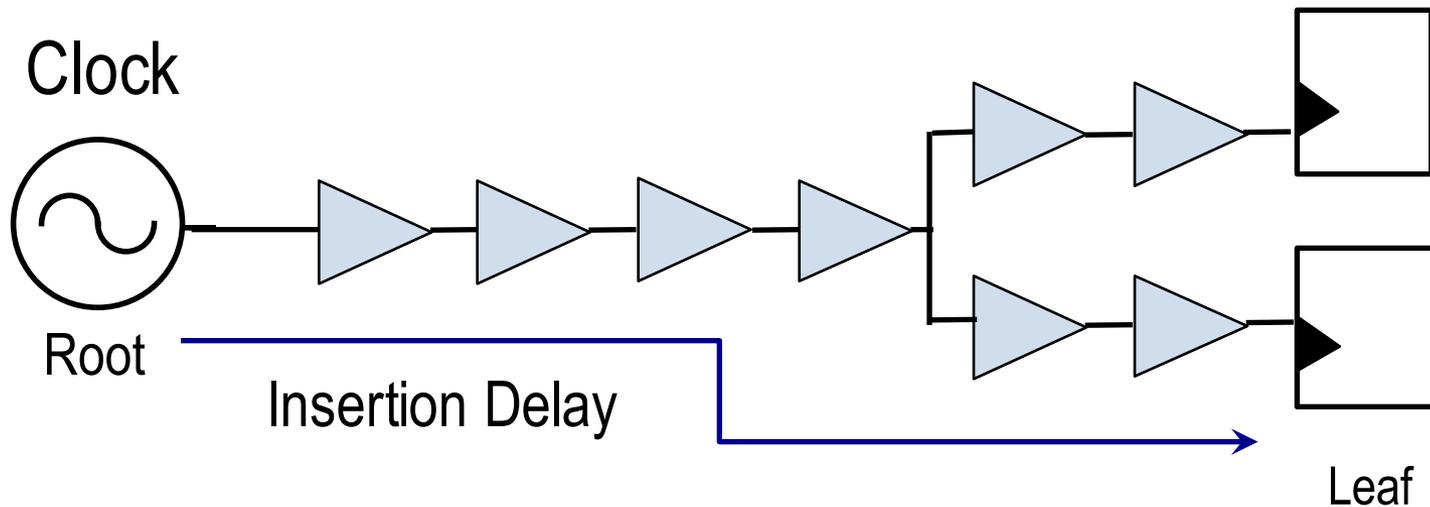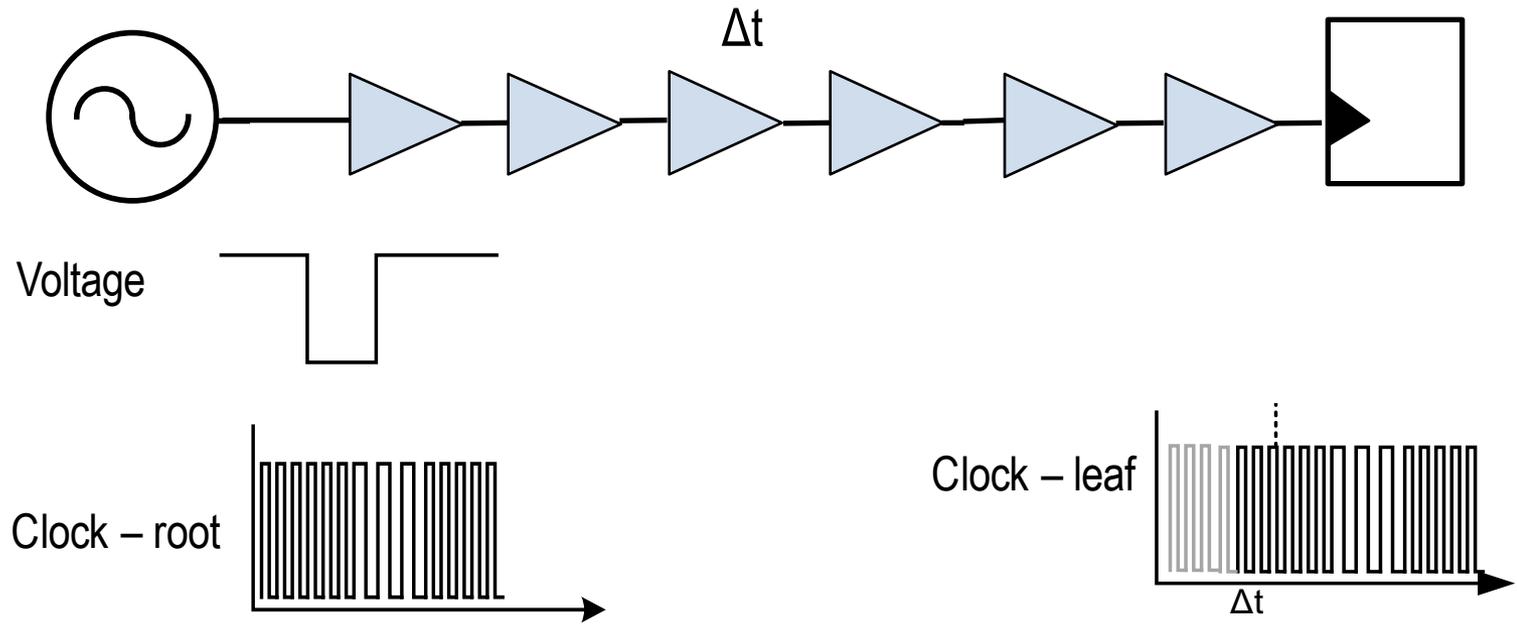
Adaptive clock responds to supply noise

Δt time for the stretched pulses to reach the load (~ 1 -2 ns)

Higher UVN: additional margin for failure-free operation !!!

Drawbacks: Traditional Adaptive Clocking

Drawback #2: Effect of Spatial Workload Variations

Current variations across chip ➔ Variations in voltage fluctuation across chip
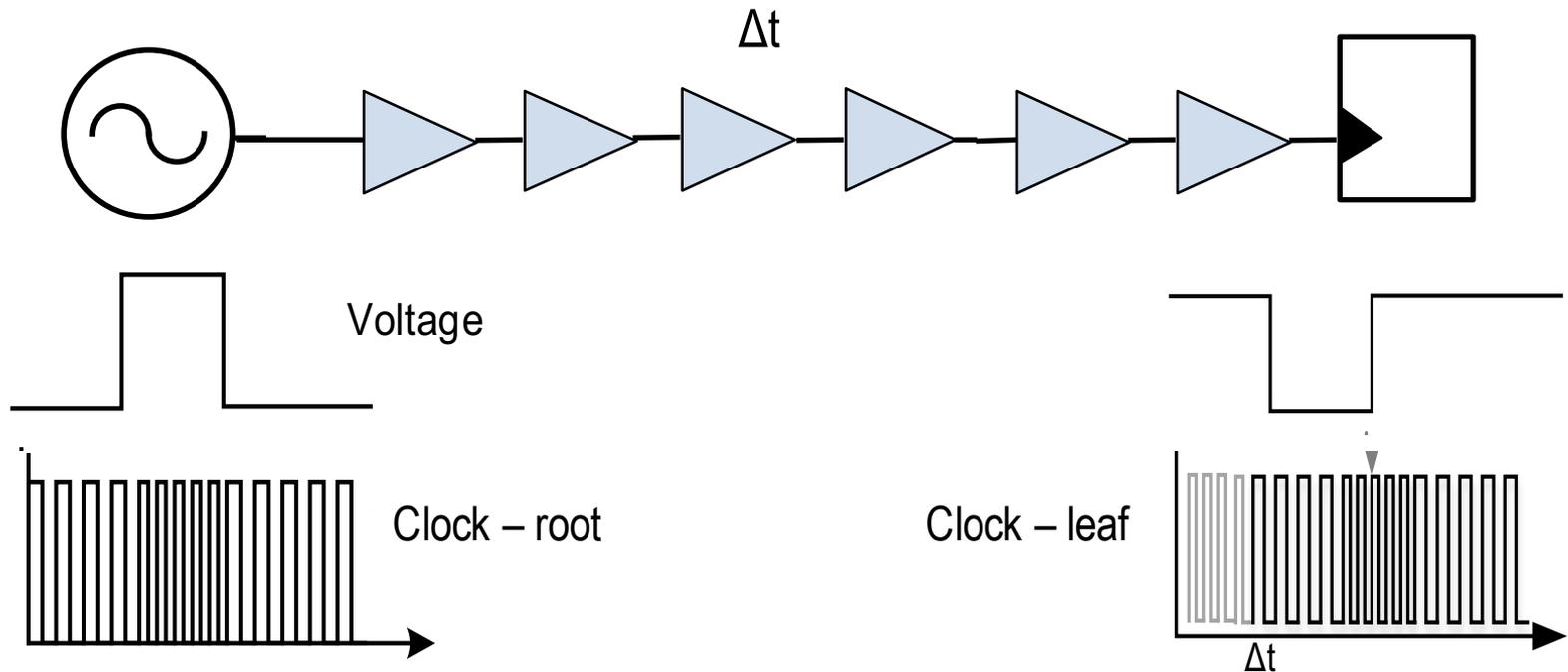
Δt

Voltage

Clock – root

Clock – leaf

Δt

Higher UVN, additional margin for failure-free operation !!!

Drawbacks: Traditional Adaptive Clocking

25 mm (vertical)

25 mm (horizontal)
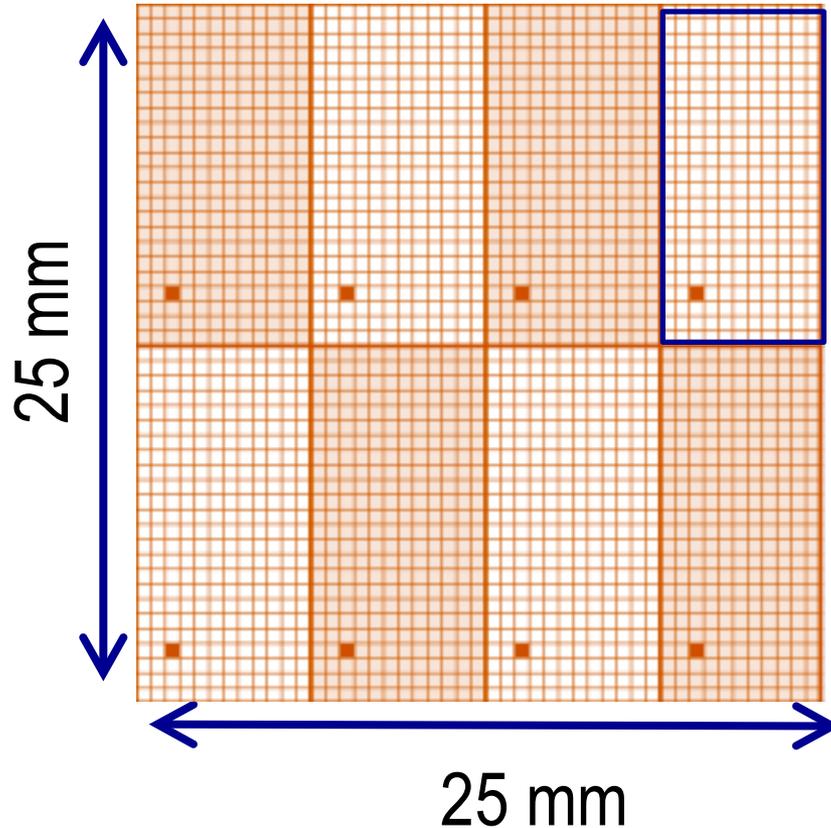
- Higher clock domain area
  - Effect of clock-tree insertion delay is higher
 - Spatial difference in voltage fluctuations is higher
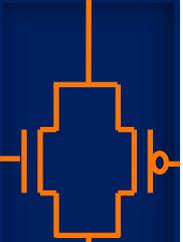
Outline

- Problem: Power supply noise
- Existing solution
    - Traditional adaptive clocking scheme
    - Drawbacks
- **Proposed solution: Fine-grained GALS adaptive clocking**
- Quantification of Benefits
    - Experimental setup
    - Simulation results
- Summary

Proposed Solution: Fine-grained GALS Adaptive Clock
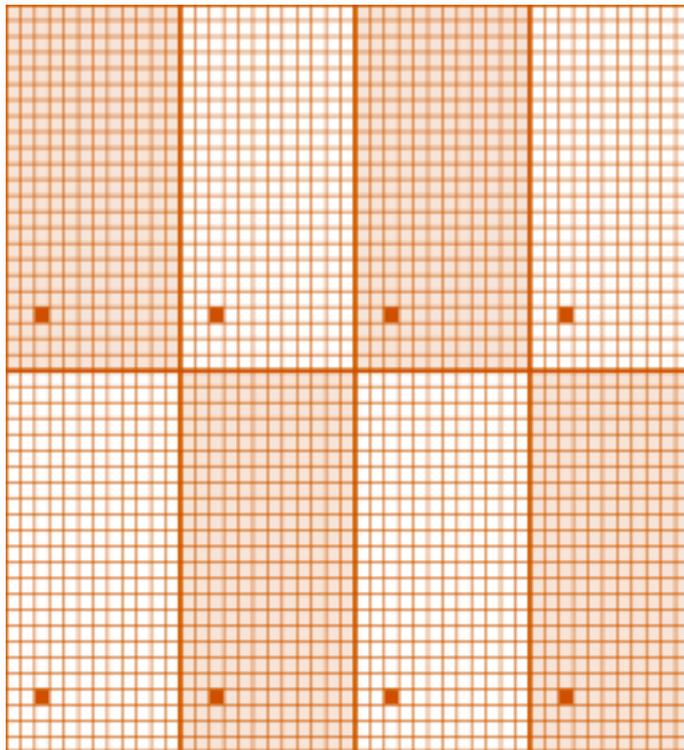
Traditional adaptive clock

Clock domain many mm^2
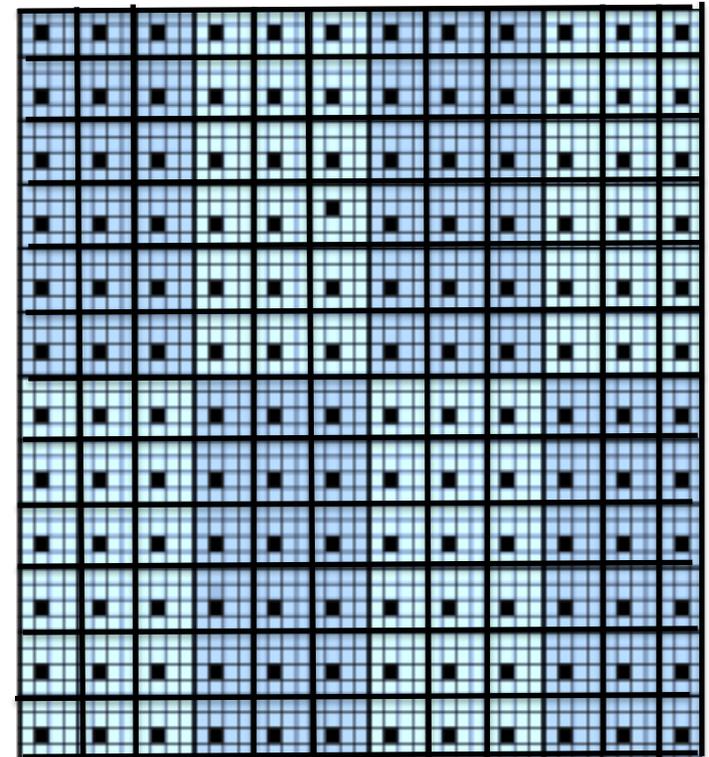
Fine-grained GALS adaptive clock

Clock domain as small as a mm^2

# Proposed Solution: Fine-grained GALS Adaptive Clock
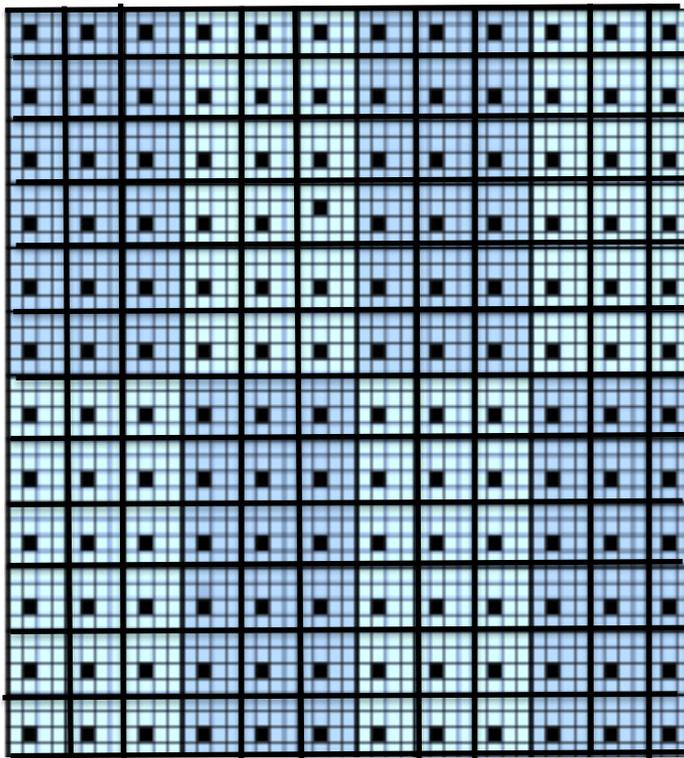
A) Asynchronous boundary crossing:

- B. Keller et. al
- Pausible bisynchronous FIFO design
- Easily integrated to standard tool flows
- Average latency 1.34 cycles

B) Myriad local clocks

- Ring oscillators: mW range power

Proposed Solution: Fine-grained GALS Adaptive Clock

- Lower clock domain area
  - Lower insertion delay (few 100 ps).
 - Lower variation in voltage fluctuation.


Voltage
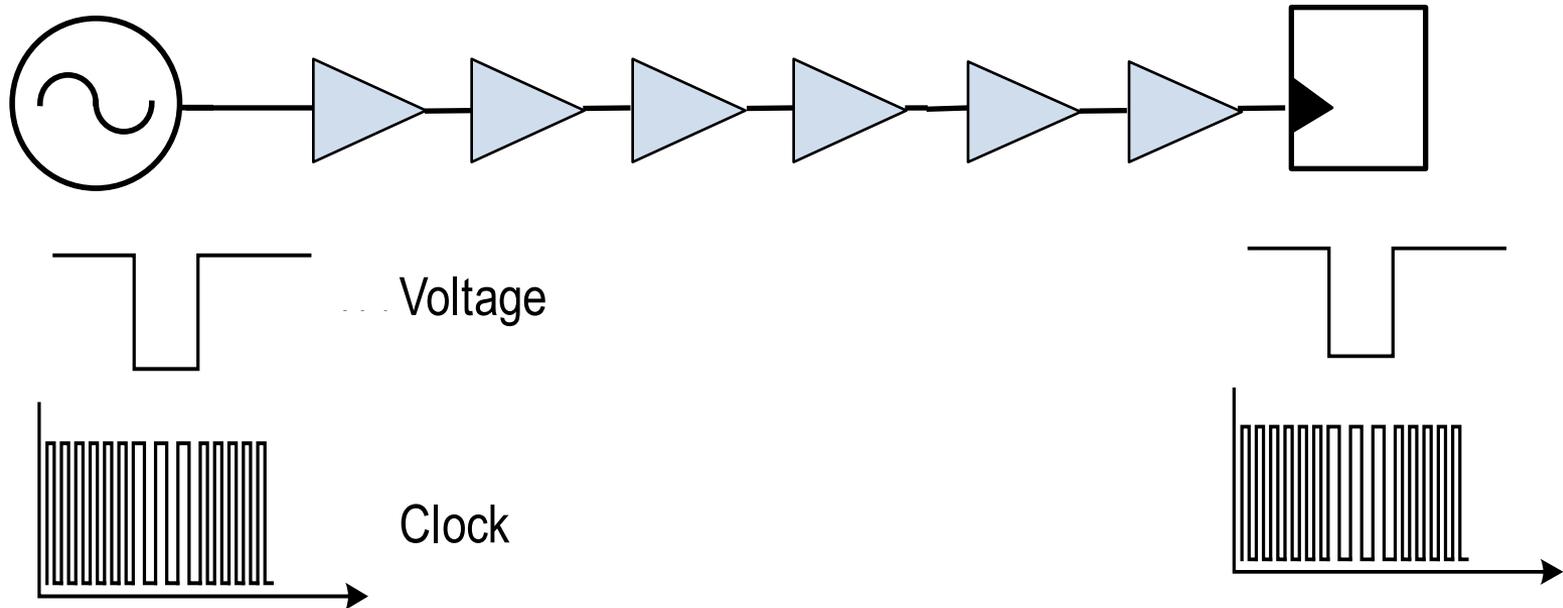
Clock

Fine-grained GALS adaptive clocks ➜ lower UVN (lower margin)!!!

Outline

- Problem: Power supply noise

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  - Drawbacks

- Proposed solution: Fine-grained GALS adaptive clocking

- **Quantification of Benefits**

  - Experimental setup

  - Simulation results

- Summary
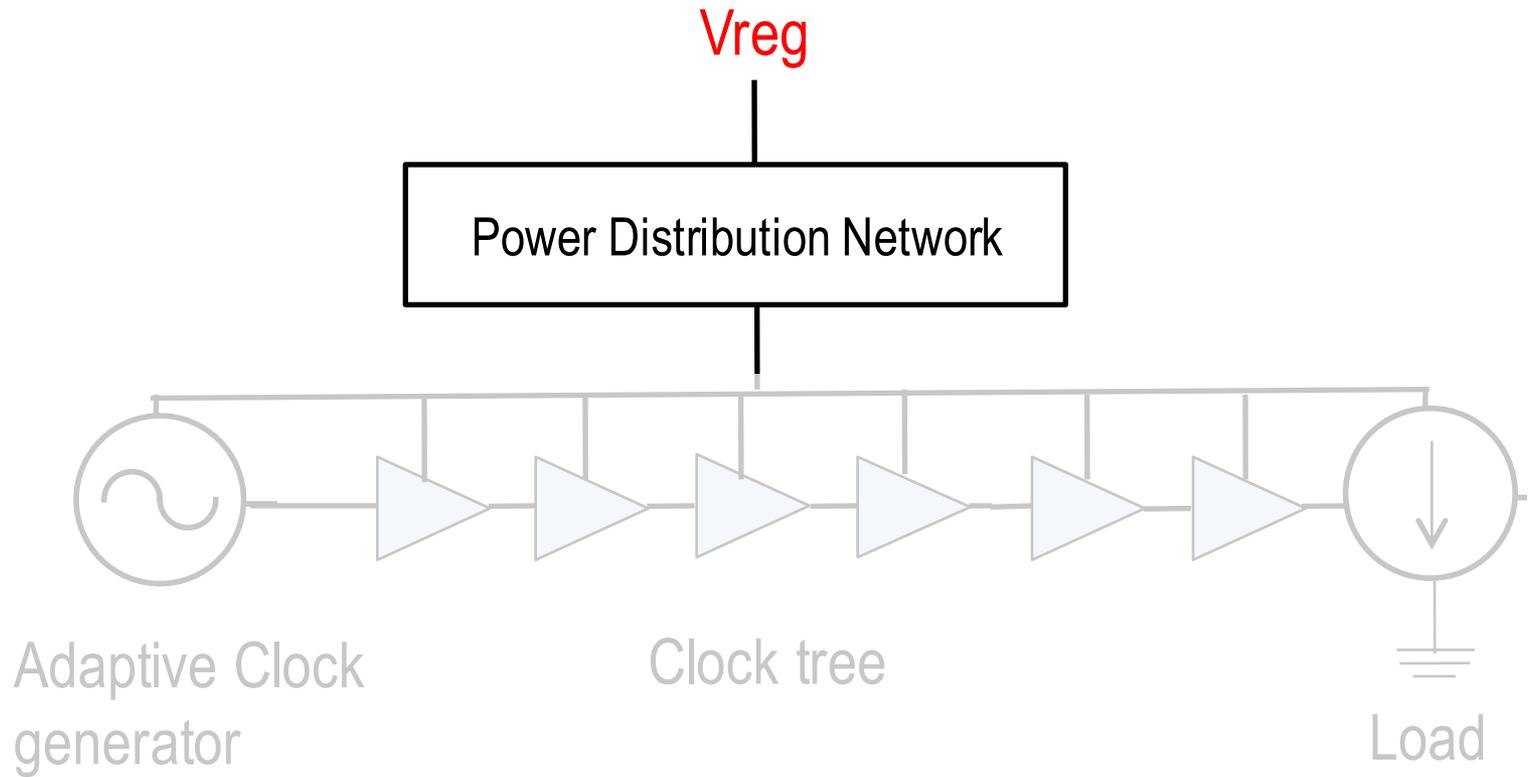
Experimental Setup

Experimental Setup

Vreg

Power Distribution Network

PCB, Package, On-chip

Rmb Lmb Rpkg Lpkg Rbump Lbump
Rhf Rpkg_p Rdie
Lhf Lpkg_p Ldie
Chf Cpkg Cdie
Board Package Die

Adaptive Clock generator

Clock tree

Load

Experimental Setup

Vreg

Power Distribution Network

PCB, Package, On-chip

V_{DD}

Adaptive Clock generator

Clock tree

Load

Experimental Setup

Vreg

Power Distribution Network

V_{DD}

Adaptive Clock generator

Clock tree

Load

Experimental Setup

Vreg

Power Distribution Network

V_{DD}

Adaptive Clock generator

Clock tree

Load

Traditional Adaptive Clocking
- Long clock-tree ➔ upto 2 ns
- Set PDN area to many mm^2

Fine-grained GALS Adaptive Clocking
- Short clock-tree ➔ low as 300 ps
- Set PDN area to just a mm^2

Details: Experimental Setup

Vreg

Power Distribution Network

V_{DD}

Adaptive Clock generator

Clock tree

Load
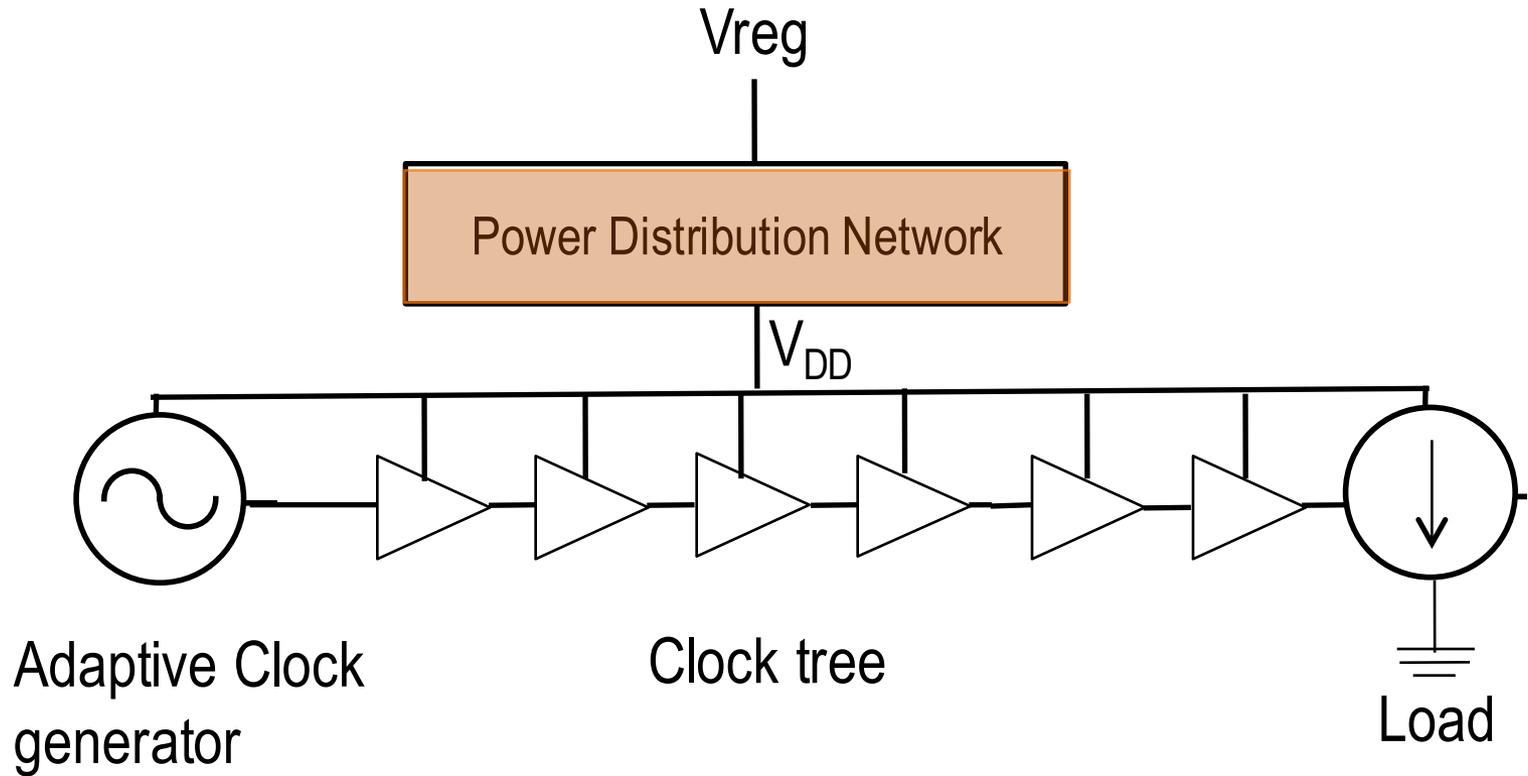
# Power Distribution Network

Simple lumped PDN model
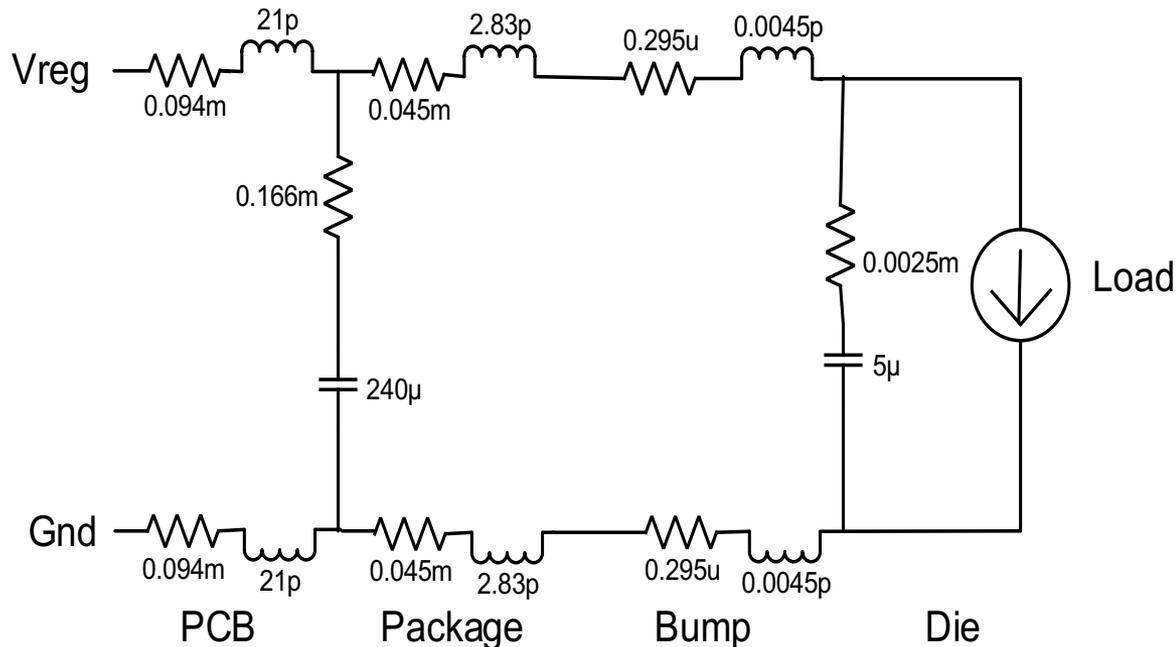
- Cannot model spatial voltage variations
- Need distributed PDN – Voltspot [3]

# Power Distribution Network

Distributed PDN model using Voltspot

Vreg

PCB + Package resistance

Gnd

Distributed package inductace

Distributed on-chip grid + C4 pads

Distributed load + decaps
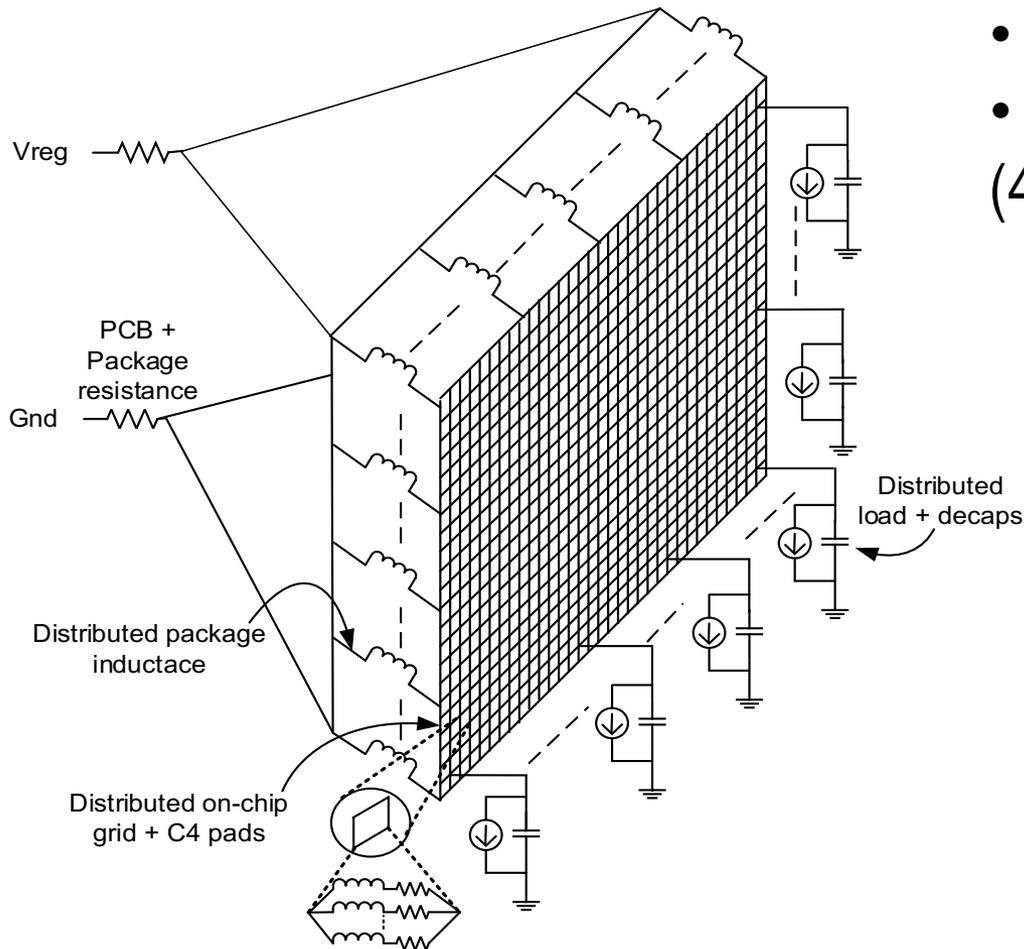
- Total chip area
- PDN divided into an array (47 x 47)

Details: Experimental Setup

Vreg

Power Distribution Network

V_{DD}

Adaptive Clock generator

Clock tree

Load
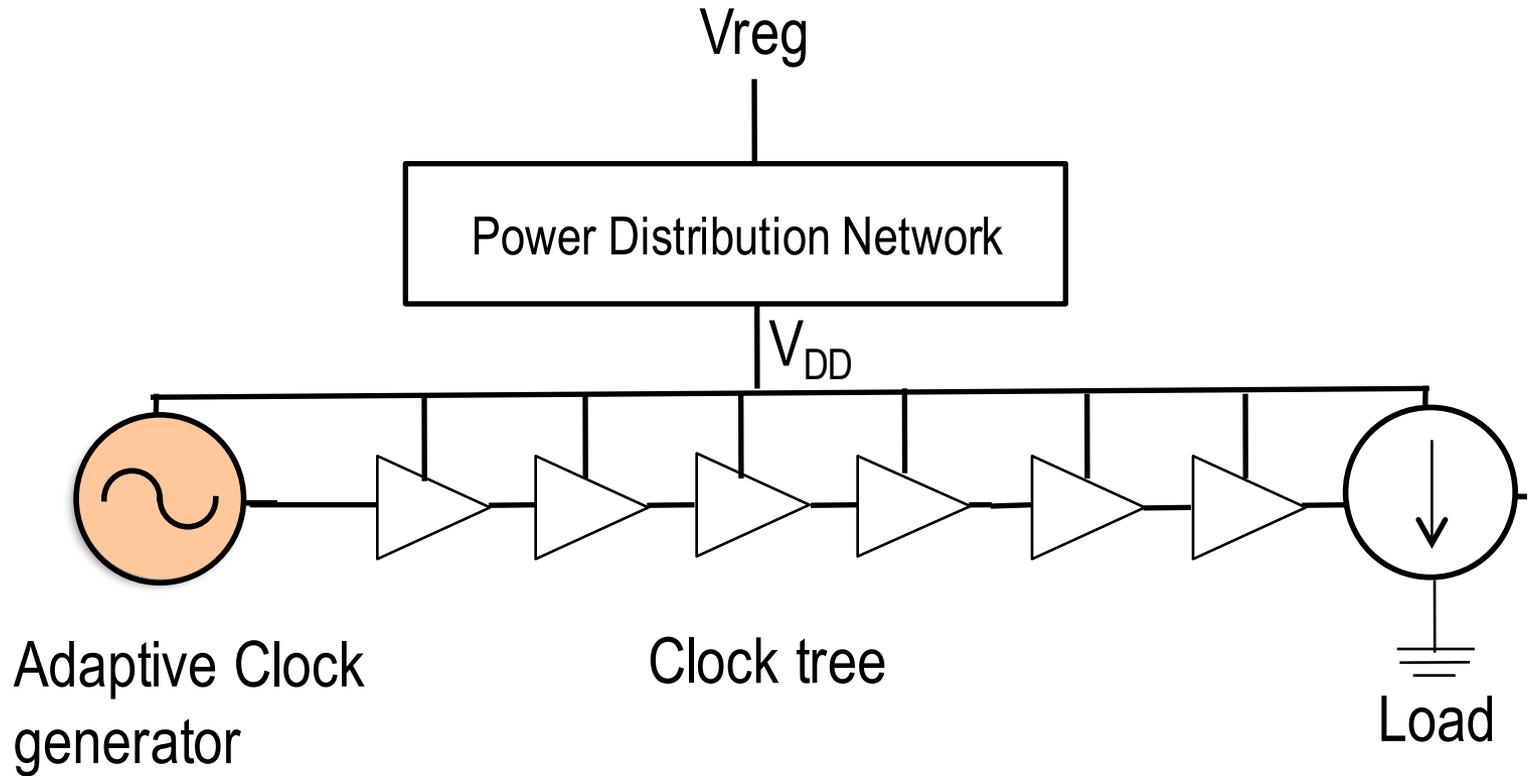
Adaptive Clock Generator
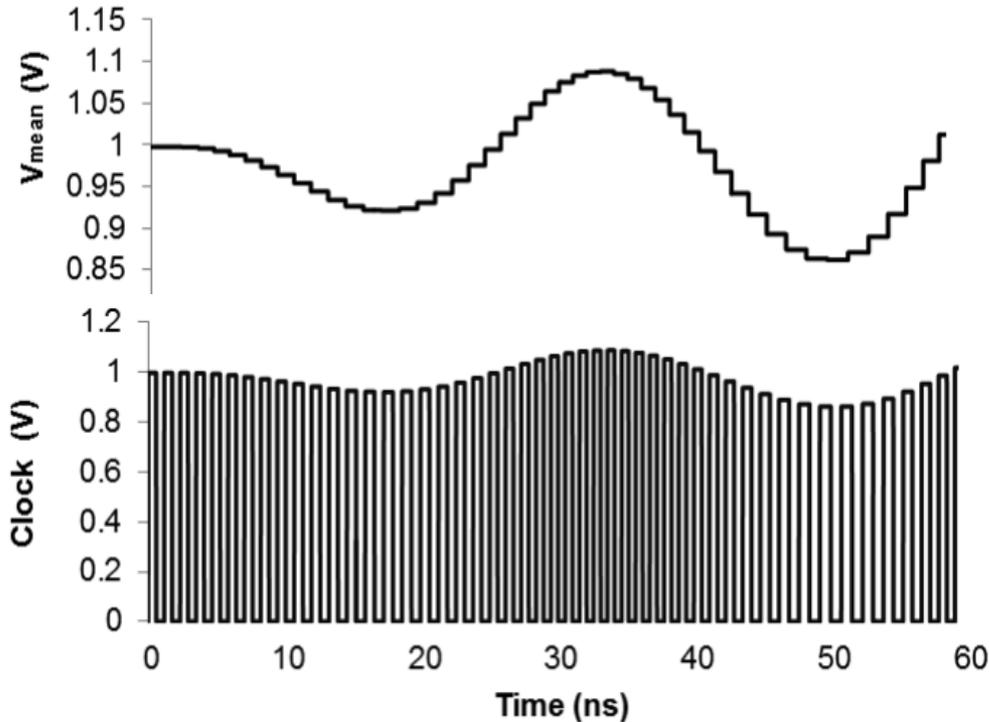
- Verilog-A model
- Voltage averaged over a cycle : V_{mean}
- Voltage vs. frequency (VF) curve

How is VF curve generated?

- Critical path: longest circuit path on an SoC
- Emulate critical path using 45 nm PDK kit
- Simulate for max frequency vs. voltage ➔ VF curve

Details: Experimental Setup

Vreg

Power Distribution Network

V_{DD}

Adaptive Clock generator
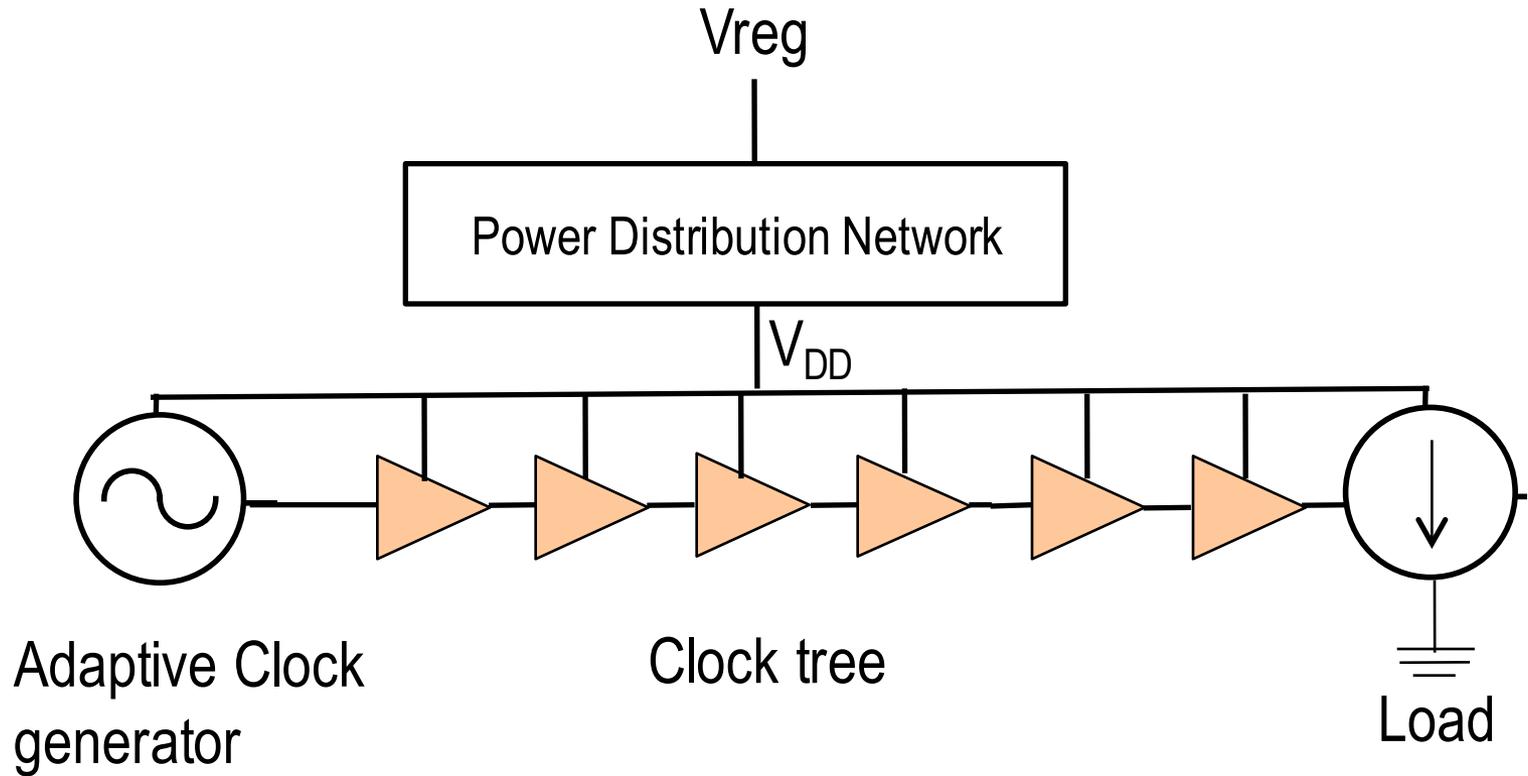
Clock tree

Load

Clock-tree

- Global and local clock distribution
- Insertion delay vs. voltage

Delay $= -22.9V^6 + 130.3V^5 - 301.7V^4 + 361.9V^3 - 232.8V^2 + 73.1V - 6.6$
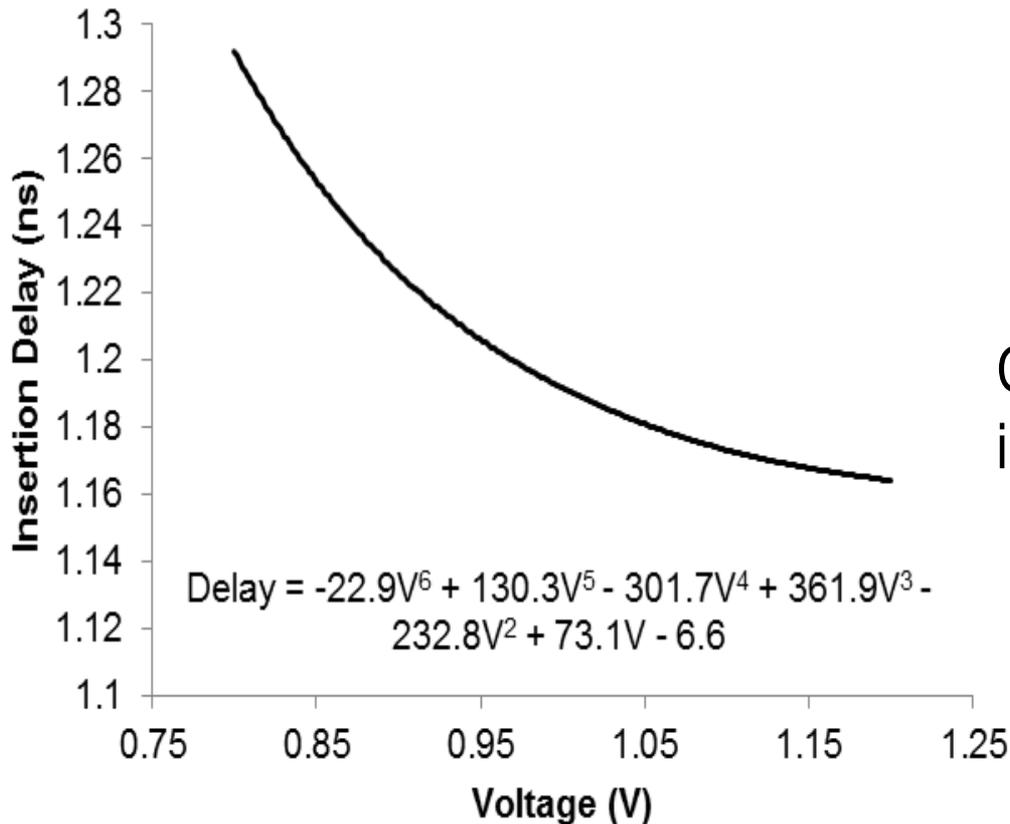
Curve fit polynomial used in Verilog-A model

Details: Experimental Setup

Vreg

Power Distribution Network

V_{DD}

Adaptive Clock generator

Clock tree
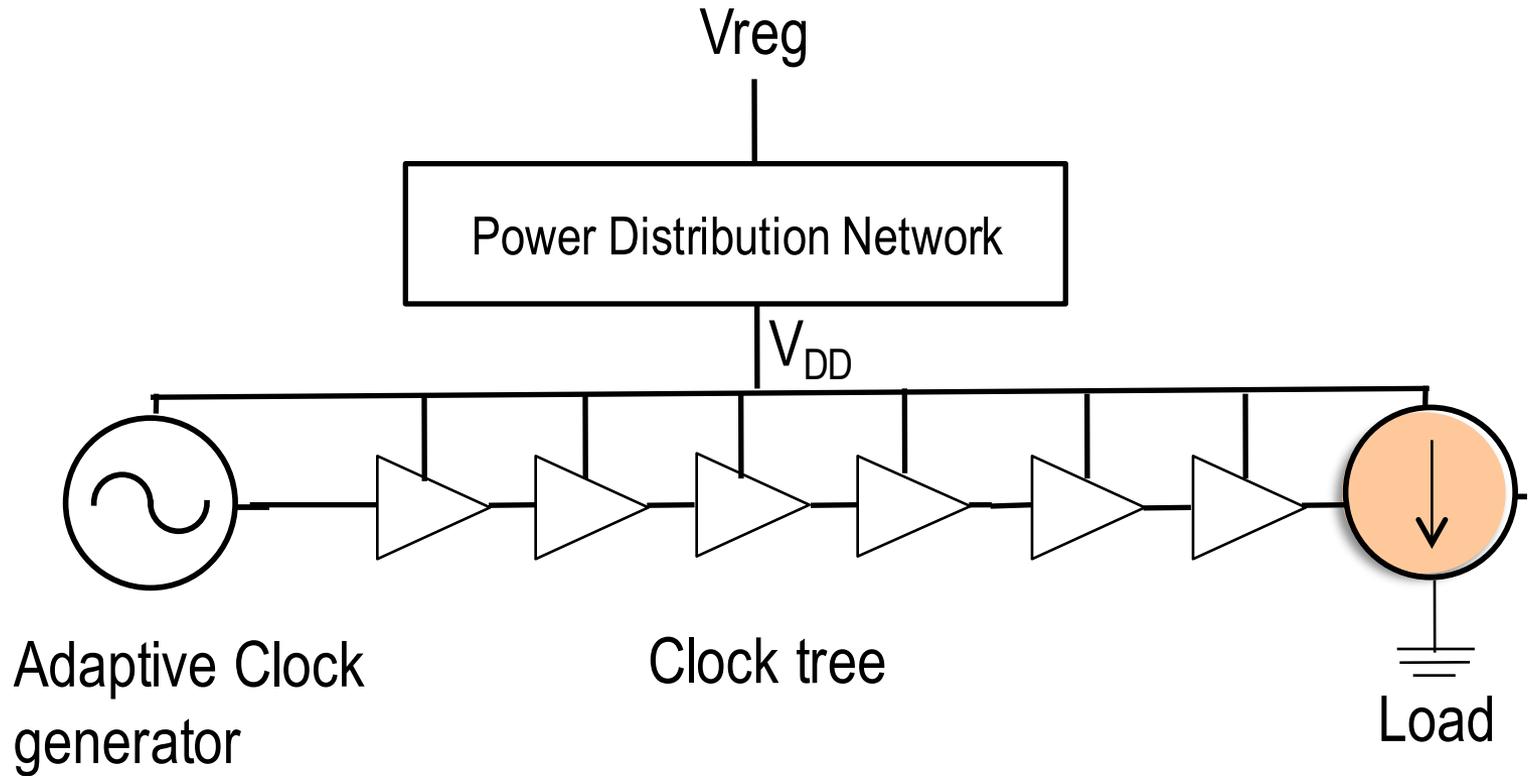
Load

Workload

- Current switching activity ➜ voltage rail fluctuation
- Resonating current profile have worst effect of supply noise
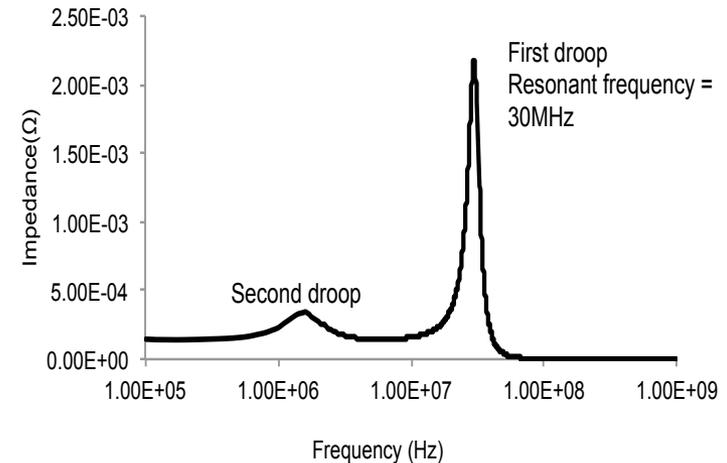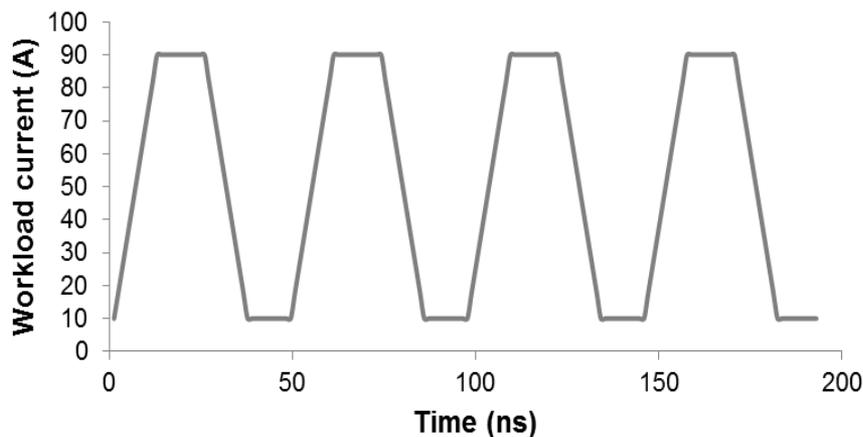
- Frequency of interest : 10 – 40 MHz (Resonance at 30 MHz)
- Current slew rate: 10 A to 90 A over 10 clock cycles
- System frequency : 850 MHz, supply voltage = 1 V

Simulation Results

A.   Effect of Clock-tree Insertion Delay

- Uniform current distribution throughout PDN area

- Sweep workload frequency: 10 - 40 MHz, insertion delay: 0.3 -1.5 ns
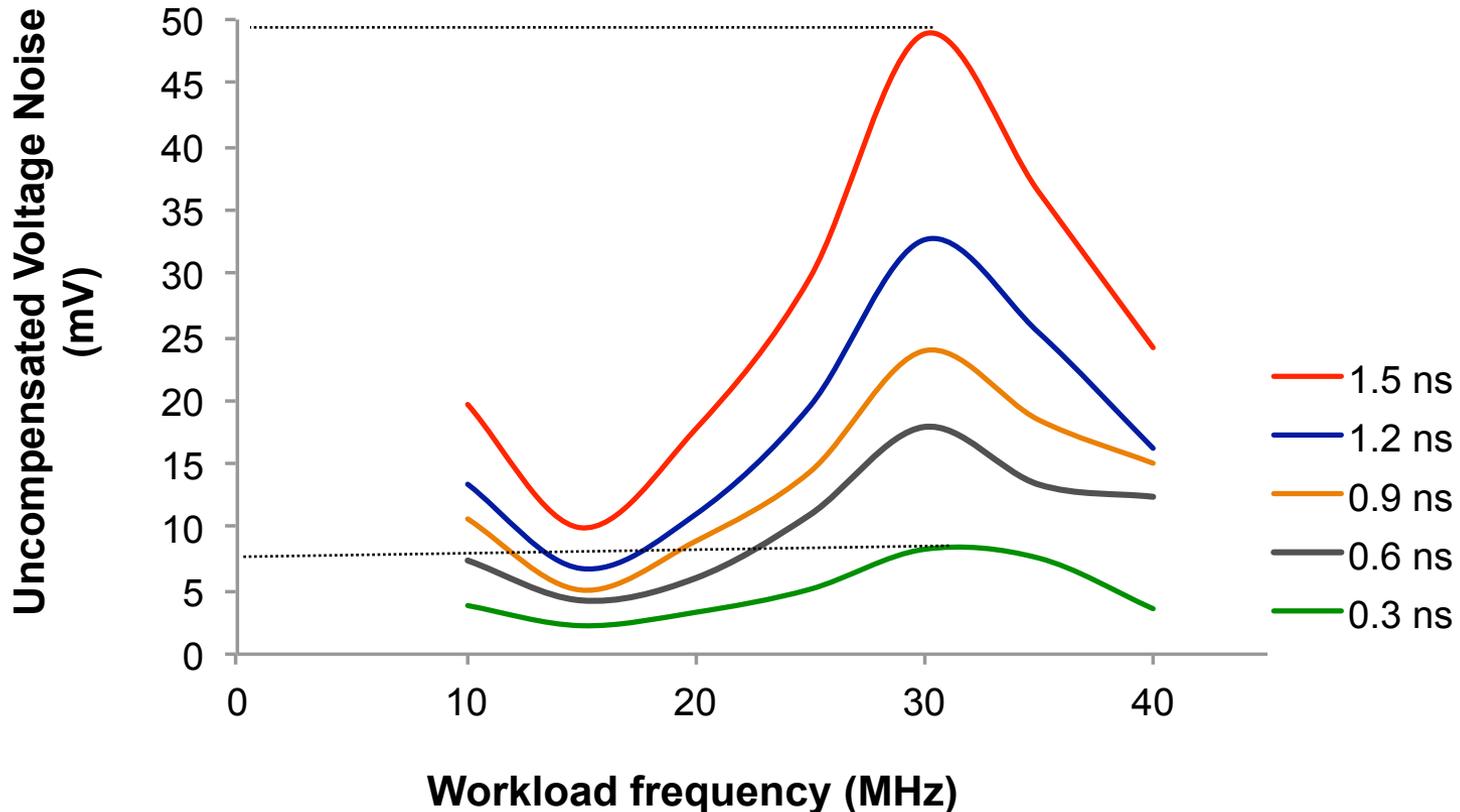
Simulation Results
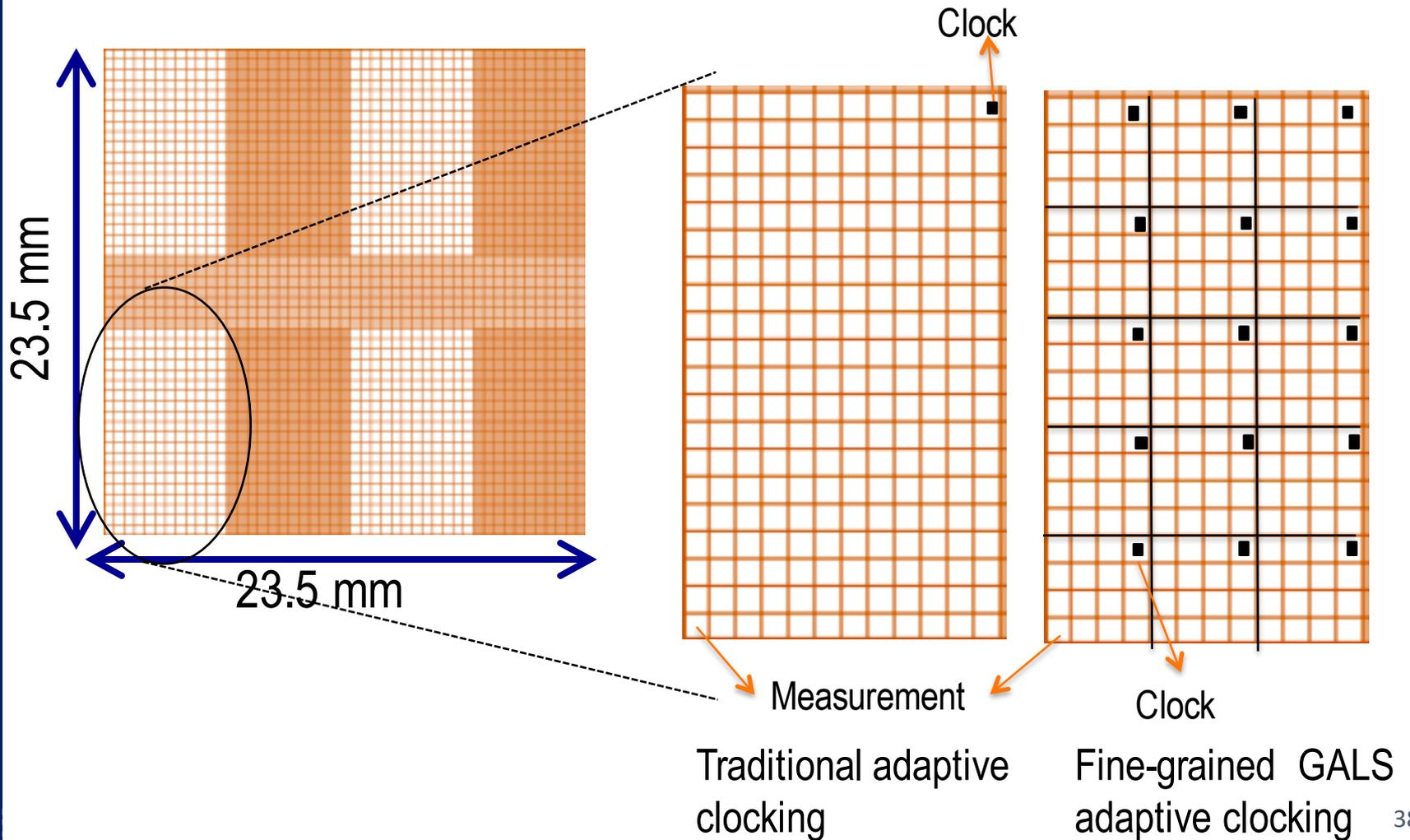
B. Effect of Spatial Workload Variations

Traditional adaptive clocking

Fine-grained GALS adaptive clocking

Simulation Results

B. Effect of Spatial Workload Variations

Traditional adaptive clocking

Fine-grained GALS adaptive clocking
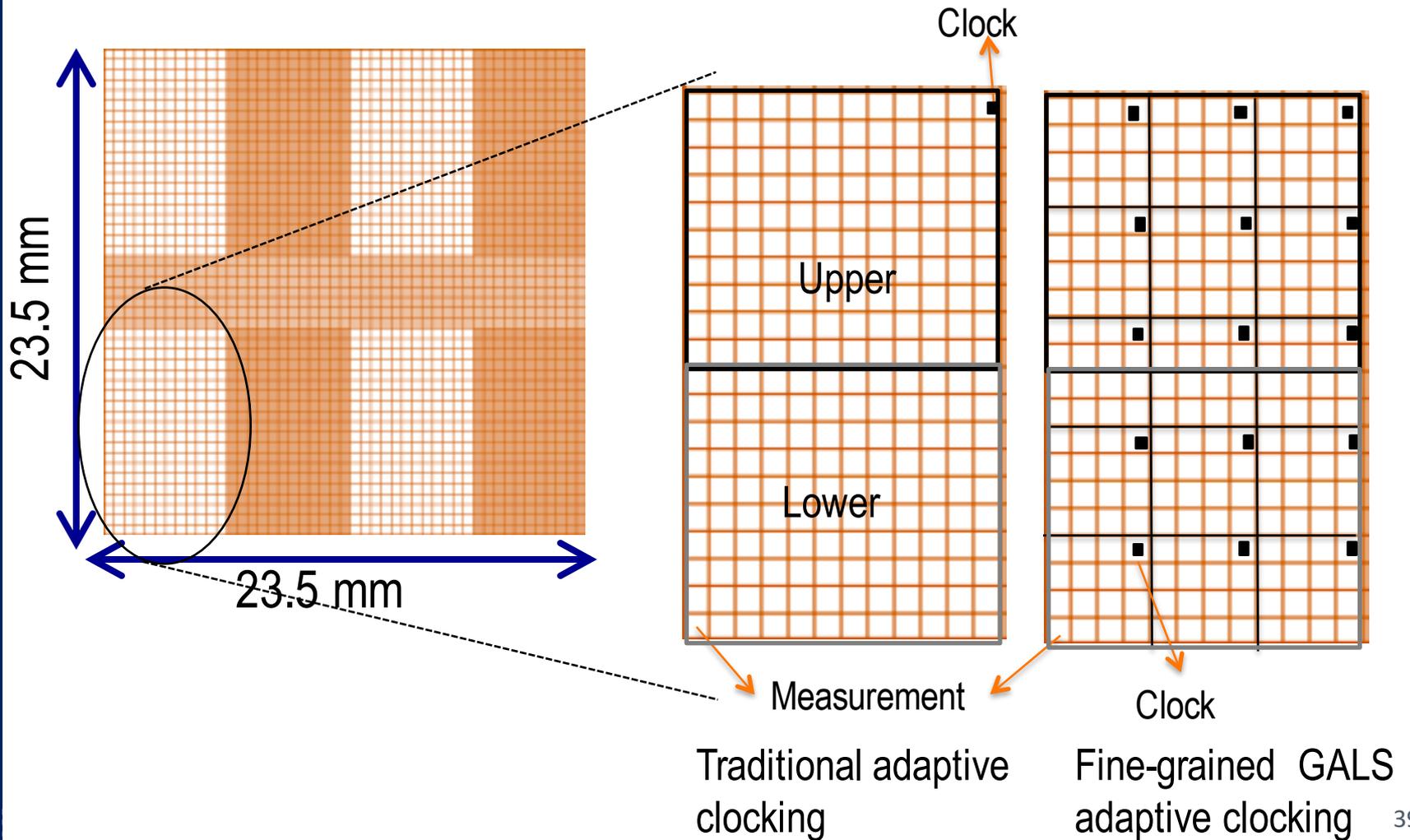
Simulation Results

B. Effect of Spatial Workload Variations:

- Lower half : 80% of power (top half: 20%)
- Workload frequency: 30 MHz
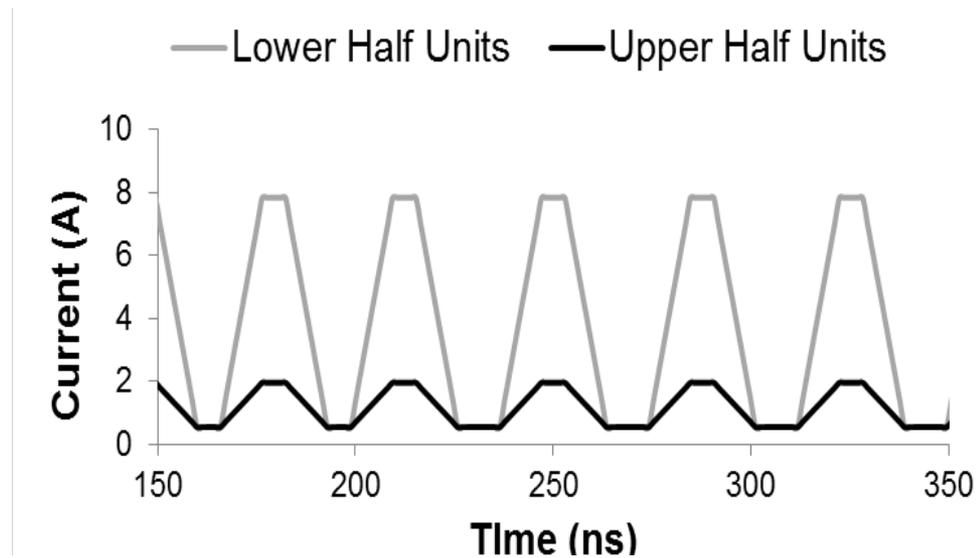
Simulation Results
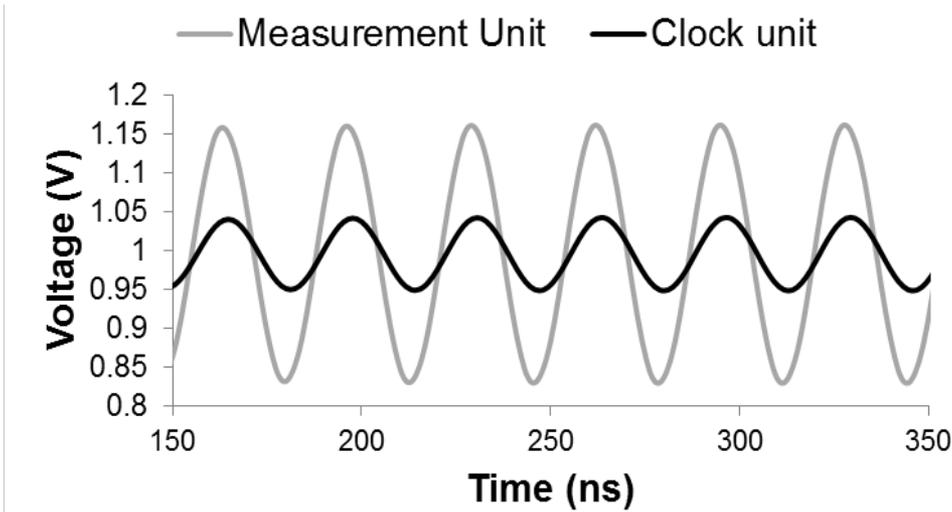
Traditional Adaptive Clocking

Uncompensated voltage noise = 111 mV
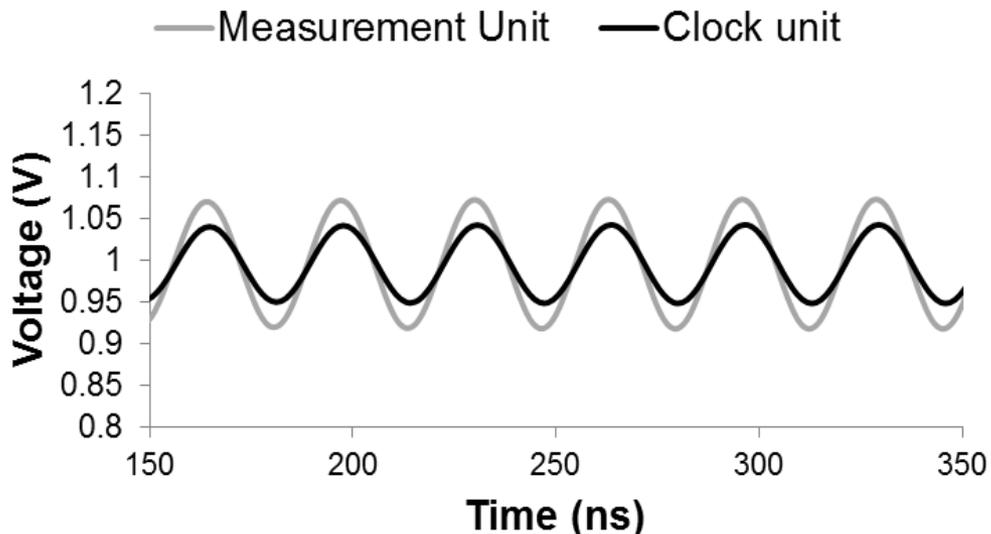
Fine-grained GALS Adaptive Clocking

Uncompensated voltage noise = 33 mV
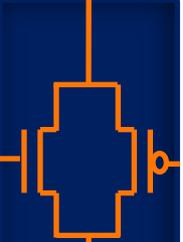
Summary

- Model and analyze power supply noise tolerance

    - Traditional adaptive clocking

    - Fine-grained GALS adaptive clocking

- Effects of clock-tree insertion delay, spatial workload variations.

- UVN savings of ~78 mV

- Equivalent to power saving of ~15% for same performance (@1 V)

- Overheads

    - Myriad local clocks

    - Good candidates are digitally-controlled / ring oscillators

    - Only a few mWs of power (<1%).

- Future work

    - Overall savings dependent on the GALS partition size.
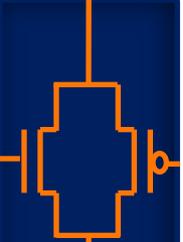
References

1. A. Grenat, S. Pant, R. Rachala, and S. Naffziger, "5.6 Adaptive clocking system for improved power efficiency in a 28nm x86-64 microprocessor," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014 IEEE International, vol., no., pp.106-107, 9-13 Feb. 2014

2. N. Kurd, P. Mosalikanti, M. Neidengard, J. Douglas, and R. Kumar, "Next Generation Intel¯ Core™ Micro-Architecture (Nehalem) Clocking," in Solid-State Circuits, IEEE Journal of , vol.44, no.4, pp.1121-1129, April 2009

3. R. Zhang, K. Wang, B. H. Meyer, M. R. Stan, and K. Skadron, "Architecture implications of pads as a scarce resource," in Computer Architecture (ISCA), 2014 ACM/IEEE 41st International Symposium on , vol., no., pp.373-384, 14-18 June 2014

Thank You!