Stepped Supply Voltage Switching for Energy Constrained Systems

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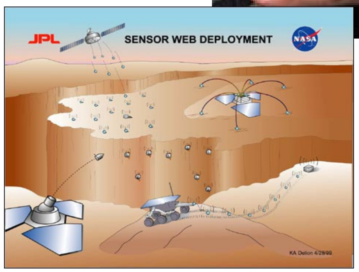
Low Power Systems

- Contemporary Applications
  - Cellphones
  - Tablets

- Emerging Applications
  - Wearable and Implantable Medical Systems
  - Environmental Sensors

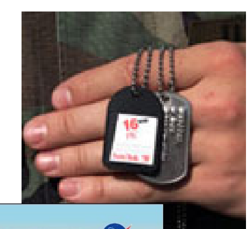
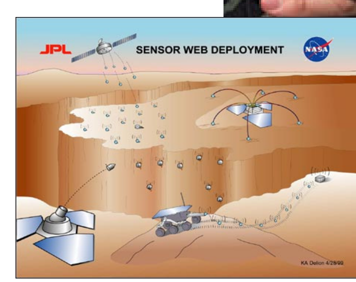


Low Power Systems

- Limited Battery Life


- Low Power Modes:
  - Power Gating
  - Retention Mode
  - Dynamic Voltage Scaling (DVS)

- Cost associated with going into and coming out of a low power mode

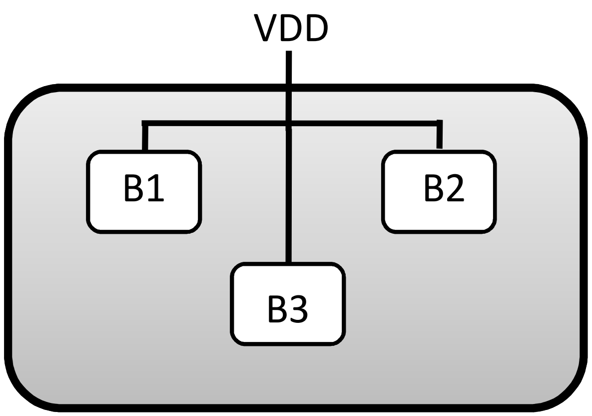



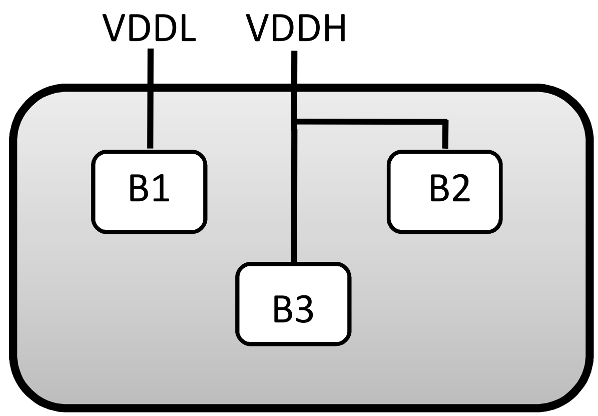
Overview

- Introduction
- Stepped Supply Voltage Switching (SVS): Introduction and Theoretical Analysis
- Simulation & Measurement Results
- Noise Reduction using SVS
- Conclusions

DVS Variants

Voltage supply of a block should track the block's *required* delay





Single-VDD DVS

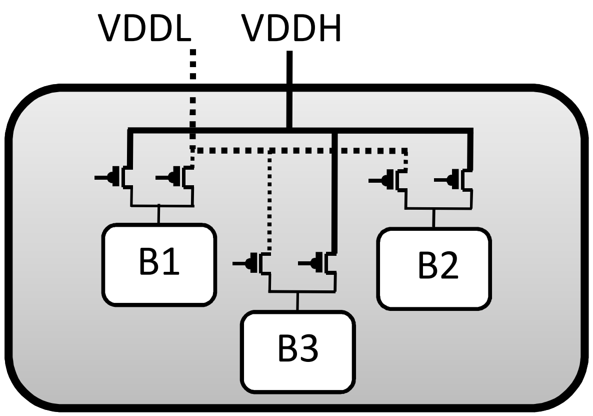
- VDD of entire chip is varied
- Lot of block level slack is wasted
- DC-DC converter controls VDD
- Varying the supply is slow

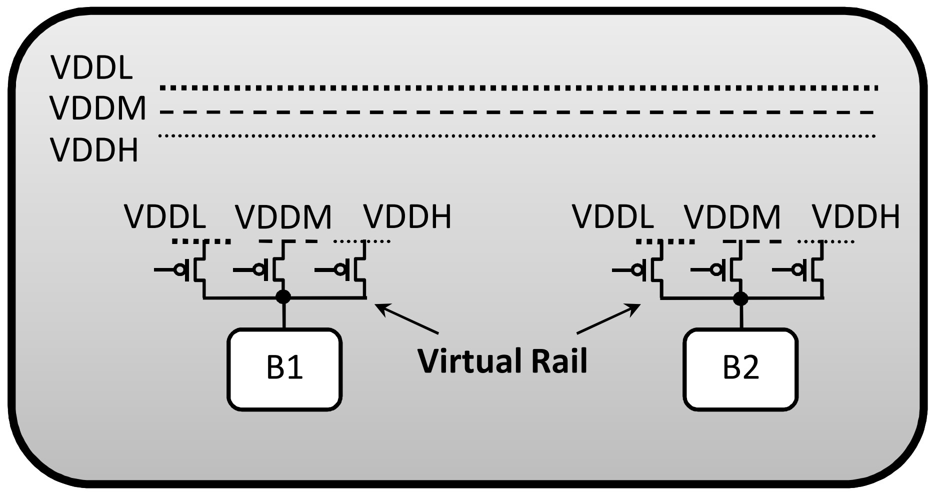
Multi-VDD DVS

- VDD of entire "voltage domain" is varied
- *Static VDD-Block scheduling*
- DC-DC converter(s) controls VDDL and VDDH
- Varying the supply is slow

DVS Variants: Panoptic DVS

- Dynamic VDD-block scheduling
- Number of supplies can be greater than 2

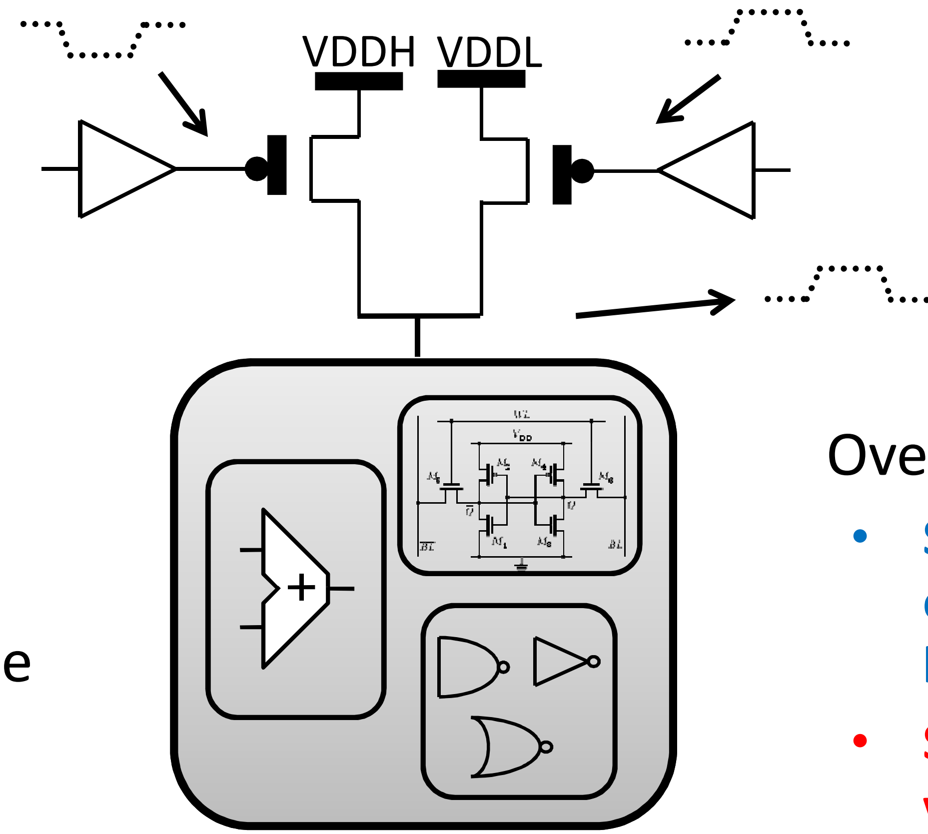




- Varying the supply to a block is fast

Ref: Putic "Panoptic DVS: A fine-grained dynamic voltage scaling.." ICCD 2009

Overhead of Switching the Virtual Supply Rail



Applicable for:

- Power Gating
- Retention Mode
- PDVS

Overheads include:

- Switching the control signals for headers
- Switching the virtual supply rail (VDD switching E)

Overheads lower the benefits of DVS.

So, can we lower the VDD Switching Energy?

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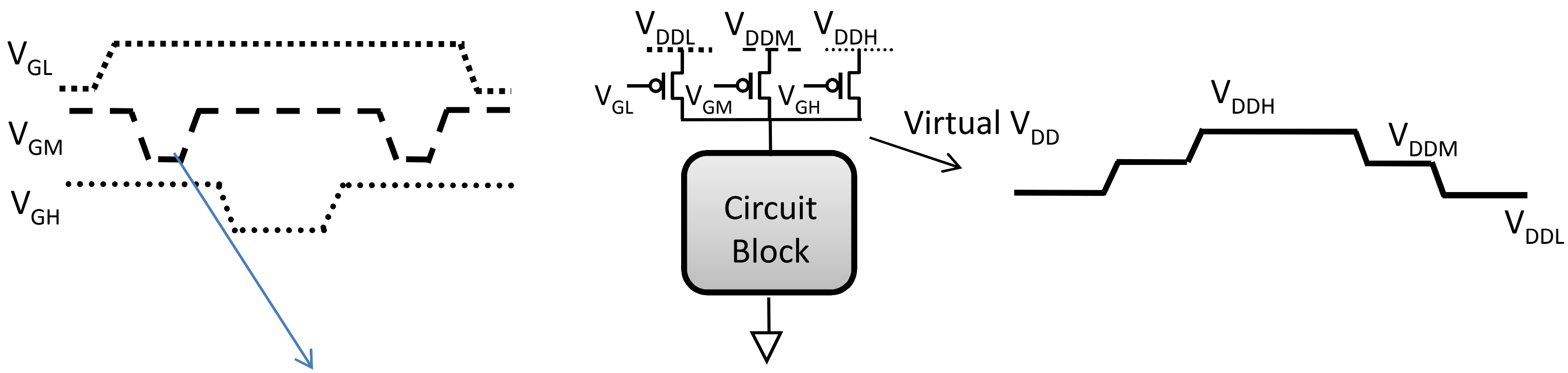
Stepped Supply Voltage Switching (SVS)

- We use SVS to lower the VDD switching energy during:
  - Power gated mode to VDDH
  - VDDL to VDDH
- PDVS systems already have the extra VDDM rail
  - Thus, no need to add dedicated rail for implementing SVS



VDDM control voltage is pulsed while going from VDDL to VDDH

Theoretical Analysis

Energy Consumed from a supply of voltage V in charging a capacitor C by ΔV = C * V * ΔV

For direct VDDL to VDDH transition:

- $E_{VDDL\ to\ VDDH}$ = C * VDDH * (VDDH - VDDL) (1)

For VDDL to VDDM to VDDH transition

- $E_{VDDL\ to\ VDDM}$ = C * VDDM * (VDDM - VDDL) (2)
- $E_{VDDM\ to\ VDDH}$ = C * VDDH * (VDDH - VDDM) (3)

$E_{saved,\ L\ to\ H}$ = (1) – { (2) + (3) } = C (VDDH – VDDM) (VDDM - VDDL) (4)

Theoretical Analysis (cont.)

Energy Consumed from a supply of voltage V in charging a capacitor C by $\Delta V = C * V * \Delta V$

For direct VDDH to VDDL transition:

- $E_{VDDH\ to\ VDDL} = C * VDDL * (VDDL - VDDH)$ (5)

For VDDH to VDD to VDDL transition

- $E_{VDDH\ to\ VDDM} = C * VDDM * (VDDM - VDDH)$ (6)
- $E_{VDDM\ to\ VDDL} = C * VDDL * (VDDL - VDDM)$ (7)

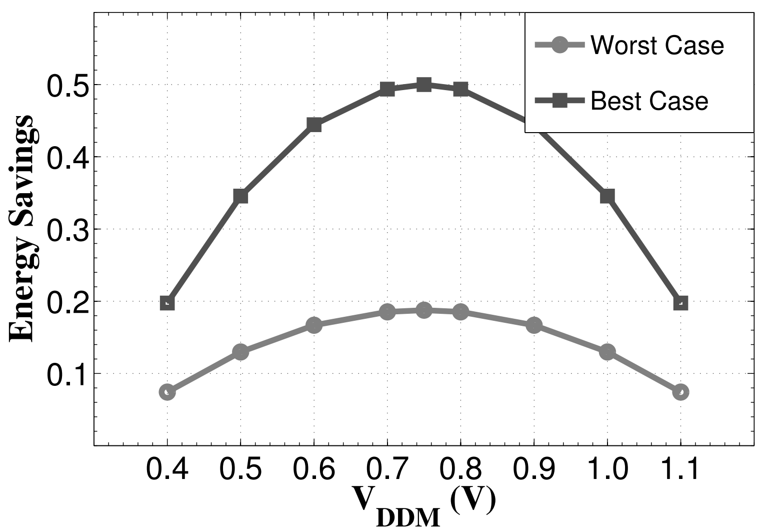
$E_{saved,\ H\ to\ L} = (5) – \{ (6) + (7) \} = C\ (VDDH – VDDM)\ (VDDM - VDDL)$ (8)

$\mathbf{E_{saved,\ total} = (7) + (4) = 2 * C\ (VDDH – VDDM)\ (VDDM - VDDL)}$ **(9)**

Theoretical Energy Savings

- Largest when VDDM is midway between VDDL and VDDH

- % Energy Saving
  - 1 intermediate step (i.e. VDDL to VDDM to VDDH) : **50%**
  - 2 intermediate steps (i.e. VDDL to VDDM1 to VDDM2 to VDDH) : **66%**



Energy saved (normalized) vs V_{DDM}
(V_{DDL} = 0.3V V_{DDH} = 1.2V)

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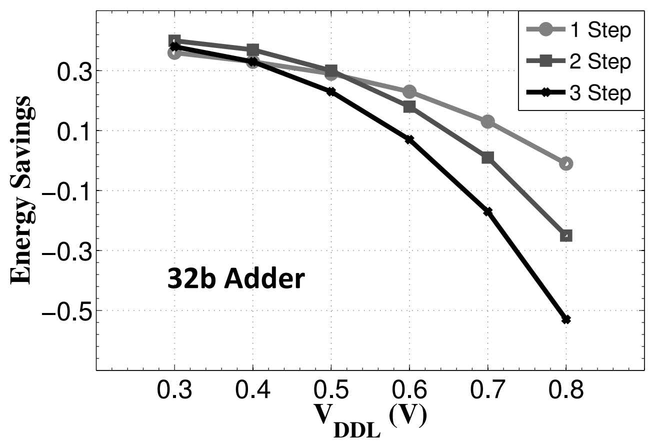
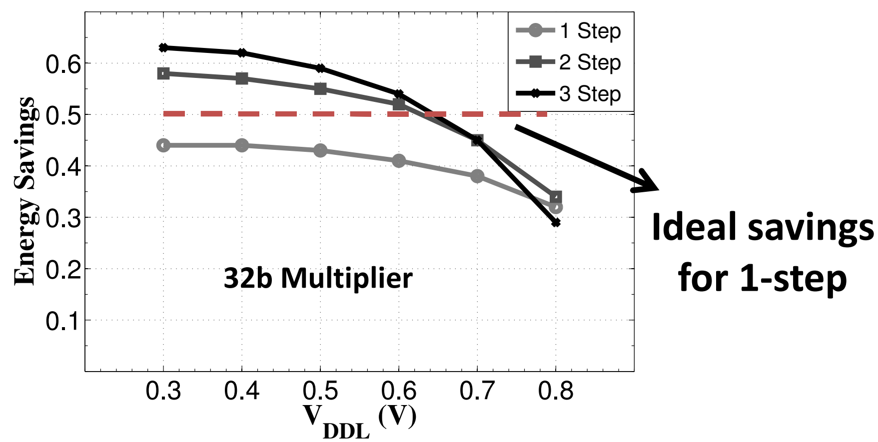
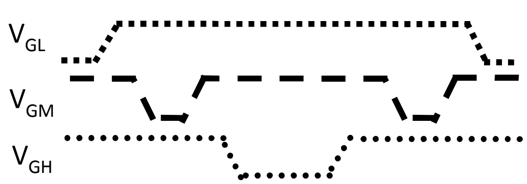
Energy savings using SVS: Simulations

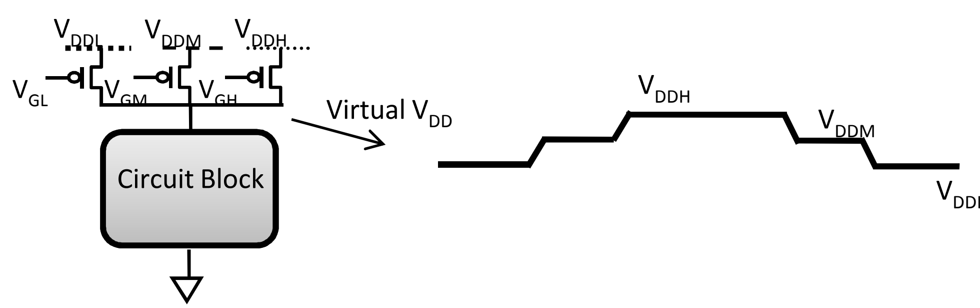
- VDDH = 1.2V, VDDL is varied
- Saving is lower than ideal because of:
  - Energy consumed in switching intermediate supply headers (e.g. V_{GM})
  - This overhead increases in % as VDDL increases
- **45% at 0.3V and 30% at 0.8V in the one-step multiplier case (ideal is 50%)**







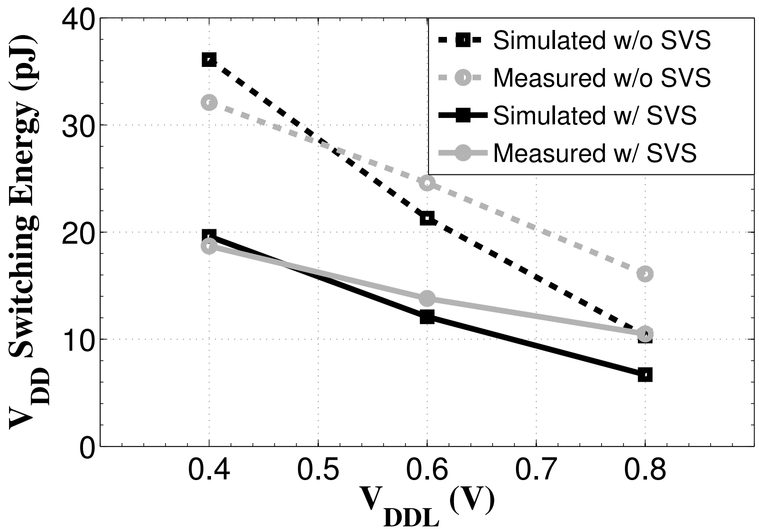
Waveforms for 1-step SVS

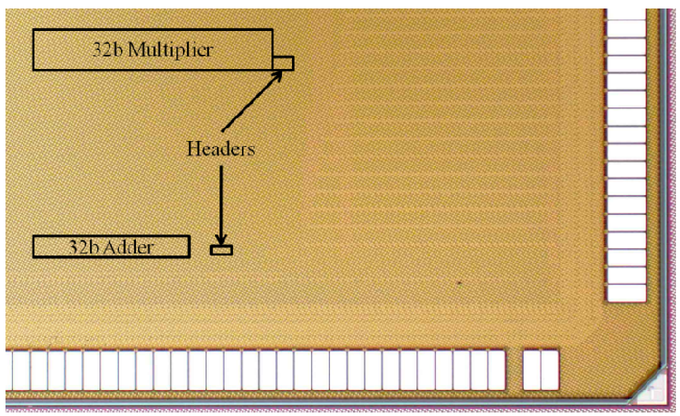


Energy savings using SVS: Measurements

- VDDH= 1.2V, for 32b multiplier
- VDDL is varied, VDDM is kept midway
- Measured and simulated trends match closely

- As before, benefits fall as VDDL rises, and header toggling energy starts dominating





Die photo of 90nm test-chip

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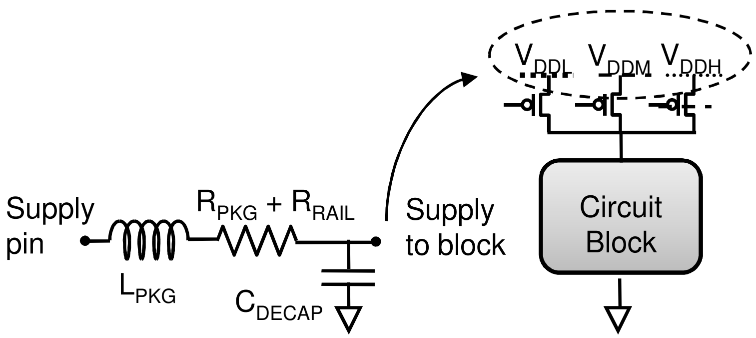
SVS and Power Supply Noise

- Noise = Ldi/dt
- SVS reduces noise by:
  - Reducing the energy consumed in the transition (decrease in "di")
- For a system using PDVS, the benefit comes with no need for additional circuitry



V_{DDL}	V_{DDL} to V_{DDM} to V_{DDH} (With SVS)	V_{DDL} to V_{DDH} (Without SVS)
0.3V	80 mV	137 mV
0.6V	55 mV	105 mV
0.9V	33 mV	58 mV

Setup:
- V_{DDH} = 1.2V, V_{DDM} midway between V_{DDL} and V_{DDH}
- 32b adder along with L_{PKG} = 10nH, R_{PKG} + R_{RAIL} =20ohm and C_{DECAP} =10pF

SVS lowers noise by 40%

Conclusions

- V_{DD} switching energy and power supply noise are critical metrics in systems using DVS and power gating
- SVS leverages existing DVS infrastructure, thus is low in overhead
- V_{DD} switching energy is lowered by a factor of 45% for a 32b multiplier, and by 35% for a 32b adder
- Power supply noise is reduced by 40% as compared to conventional power gating or DVS

Thanks!