Serial Sub-threshold Circuits for Ultra-Low-Power Systems

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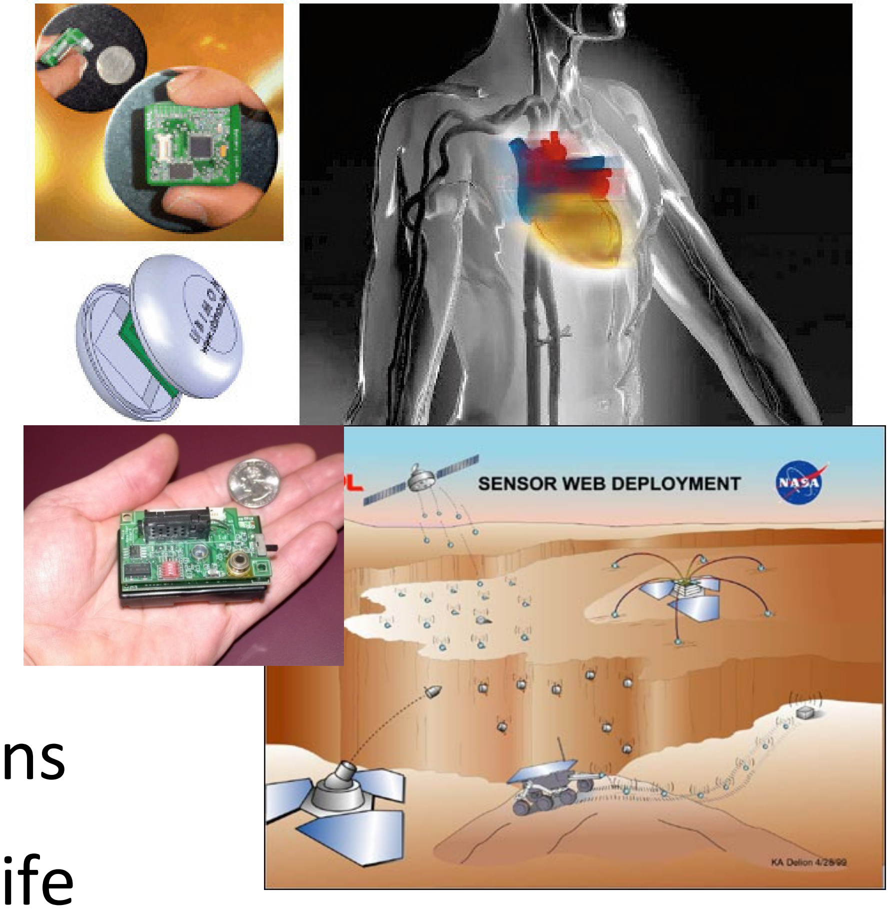
Outline

- **Ultra Low Power (ULP) Systems and Sub-threshold**
- **ULP Sub-V_T Systems: Rethink the Topology**
- **Serial vs Parallel Systems @ Equal VDD**
- **Serial vs Parallel Systems @ Equal Speed**
- **Serial Components in Parallel Systems**

Ultra Low Power Systems

- RFID tags
- Wireless Micro-sensors
- Implantable, Wearable Medical Devices



Key features:

- Small Form Factor
- Remote, Inaccessible Locations

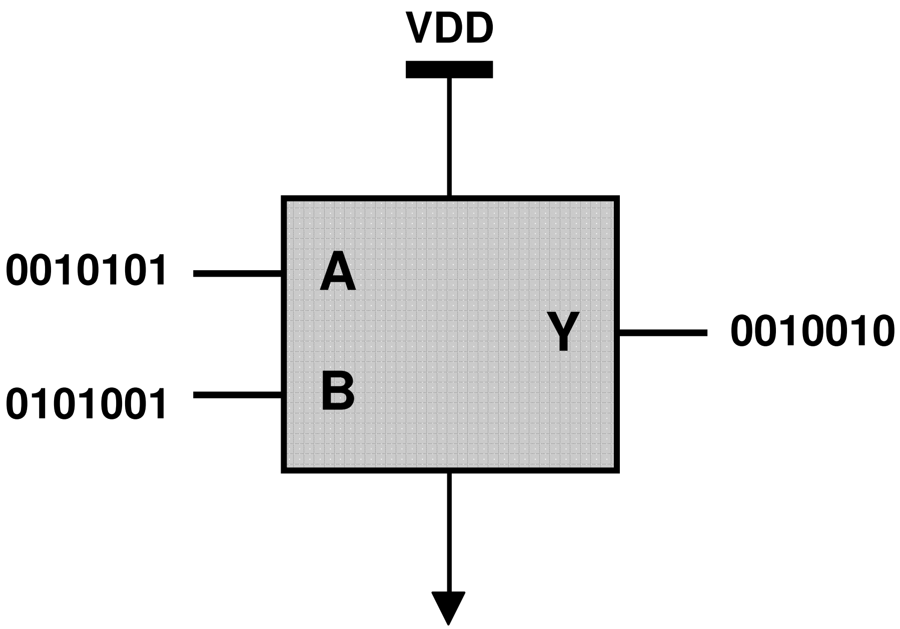
Thus, must have Long Battery Life

=> Low E consumption

ULP Systems: DESIGN FOR SLEEP

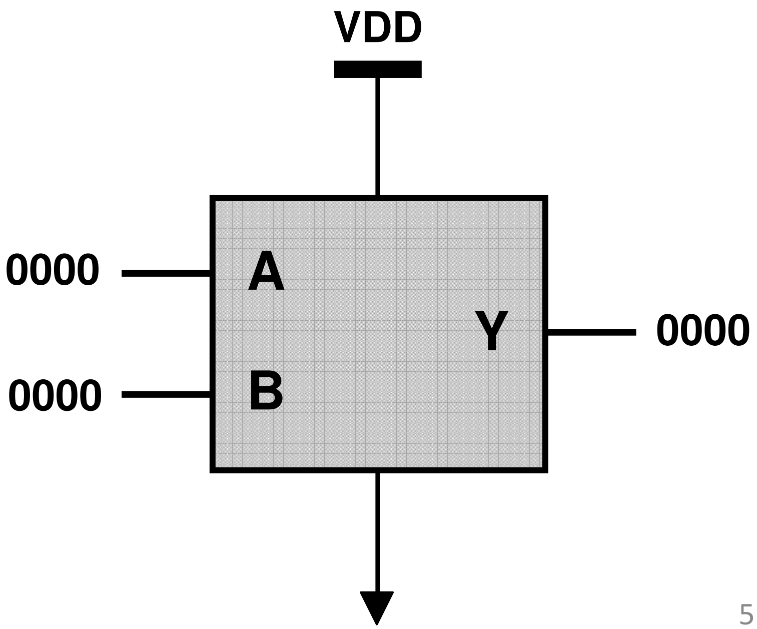
- Long Sleep Times:
  - 0.25 sec: Heart Rate
  - 1 Minute: Blood Pressure
  - 1 Hour: Temperature
  - 1 Day: Structural Health
- Total E = Active E + Sleep E
- **DESIGN FOR SLEEP MODE: Focus on Reducing Leakage**

Active and Sleep Modes



ACTIVE MODE Energy Components:

- Dynamic Energy = $\mathbf{C \cdot V^2}$
- Leakage Energy = $\mathbf{V \cdot I_{lkg\_active} \cdot Delay}$
- I_{lkg_active} -> Active Mode Leakage

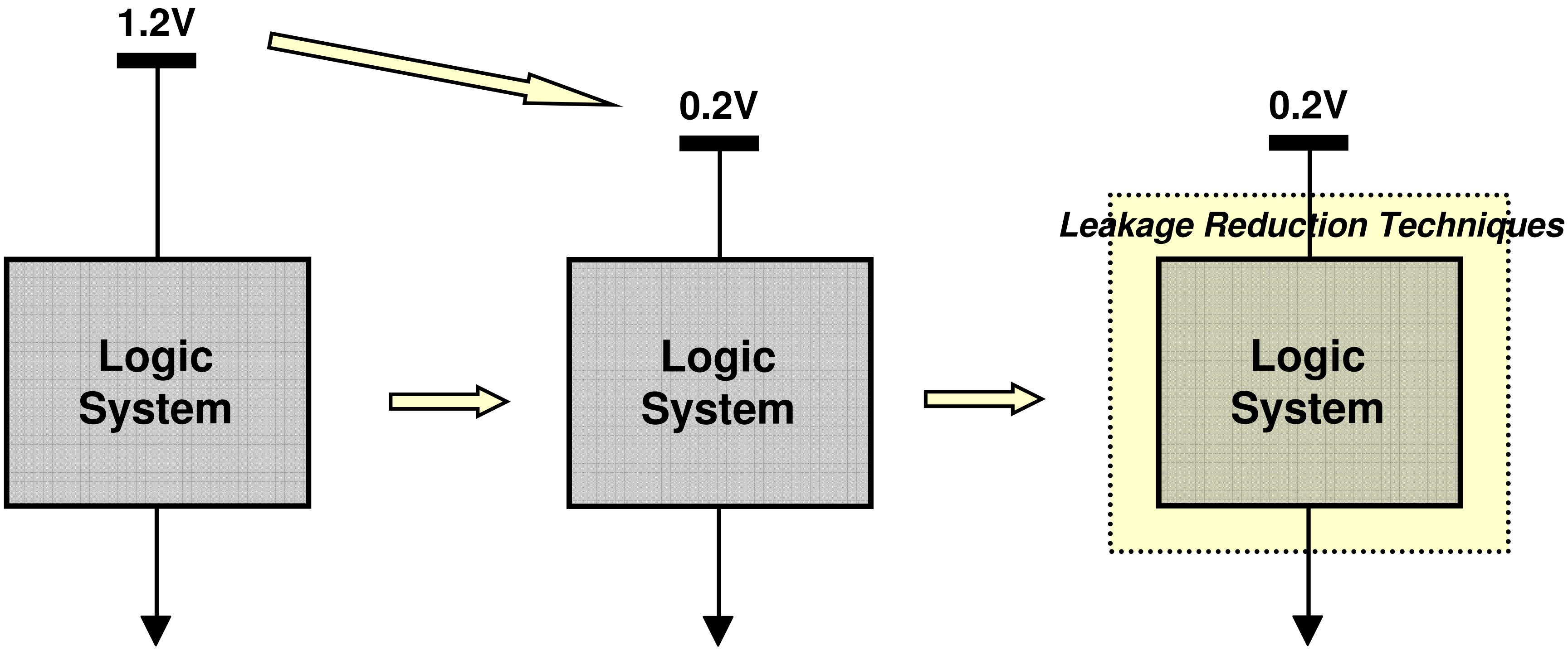


SLEEP MODE Energy Components:

- Sleep Mode Leakage Energy

  = $\mathbf{V \cdot I_{lkg\_sleep} \cdot Sleep\_Time}$
- I_{lkg_sleep} -> Sleep Mode Leakage

Lower VDD => Lower Energy, Leakage: Sub-V_T



Strong-Inversion Design:

- High Active E & Leakage

Lowering VDD, Lowers:

- **Dynamic Energy ~ V^2**
- **Leakage Current ~ exp (V)**

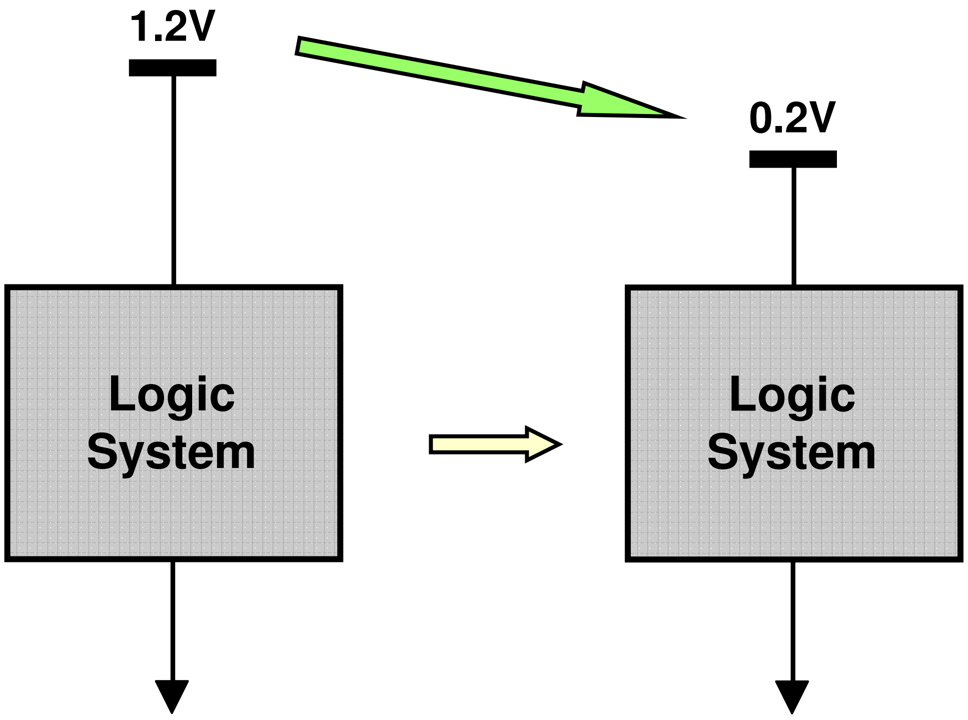
Leakage Reduction:

- Power Gating
- Rev Body Bias

DESIGN FOR SLEEP : Rethink the Topology

ULP systems put a much tighter constraint on leakage….

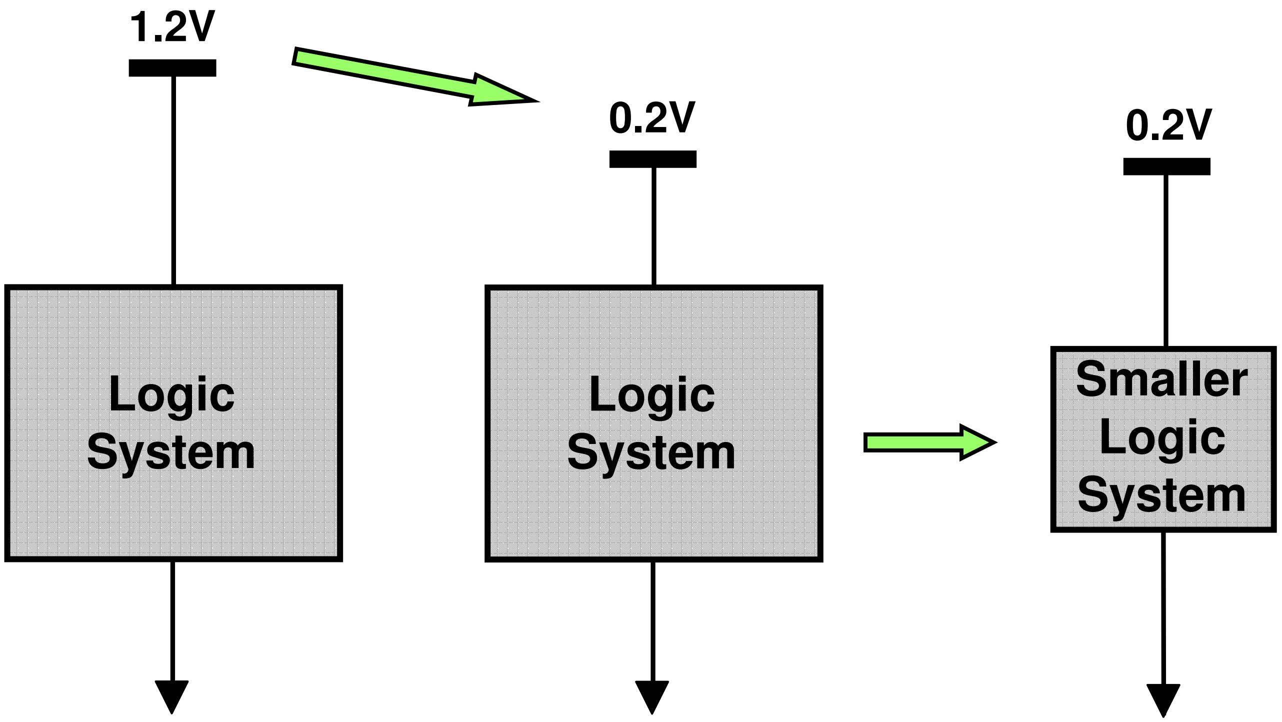
Much more so than Conventional Digital Systems



While going into Sub-V_T ,

Should the topology remain the same?

ULP Systems need a Small, Less Leaky Topology



WHY:

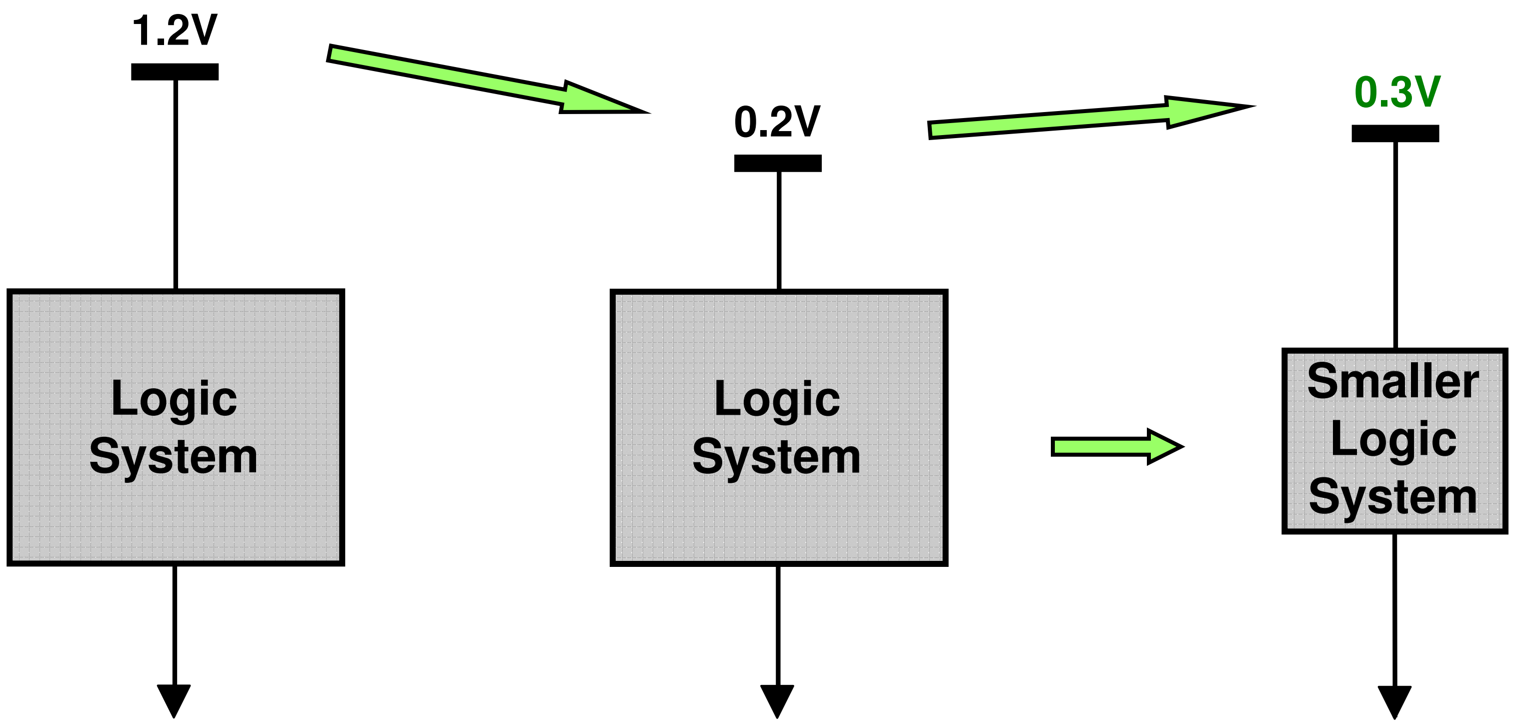
DESIGN FOR SLEEP !

TRADEOFF:

Slower Operation

How can this be overcome?

Making the Small, Slow Topology Faster



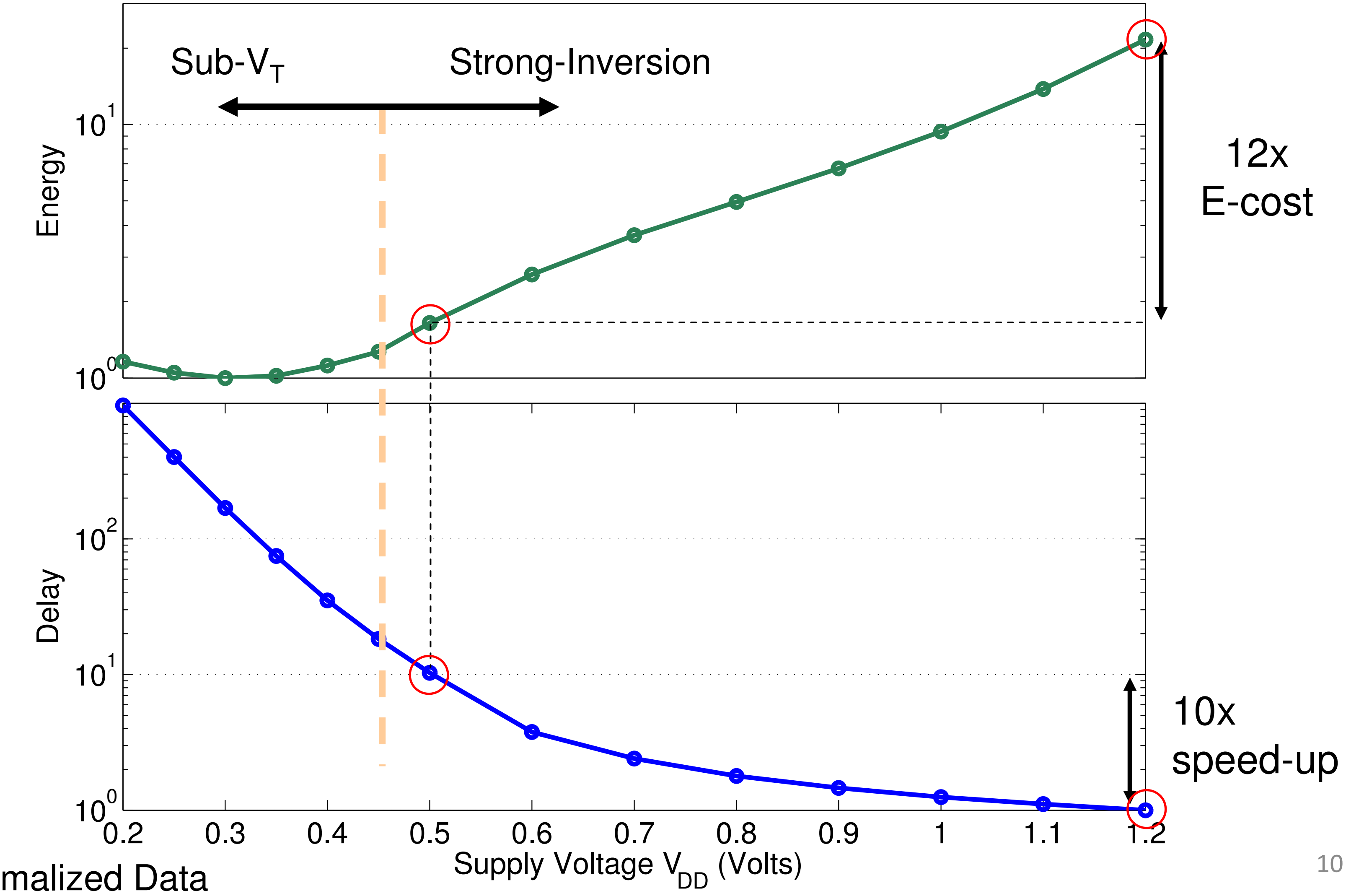
Fast, Not E-efficient

E-efficient, but Slow

As Fast, and still E-efficient

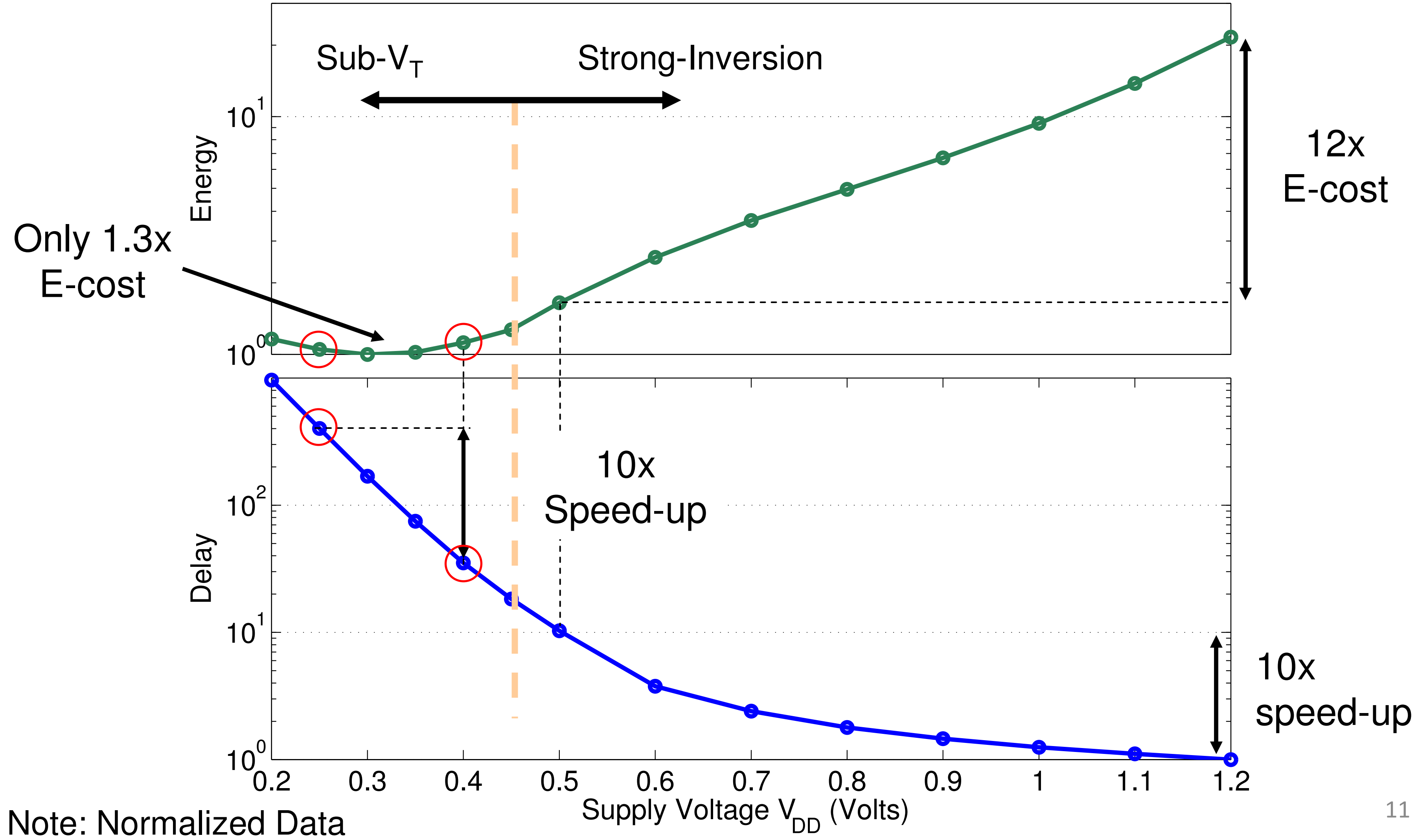
But why more E-efficient even after the VDD increase ?

Sub-V_T: Helps Increase Speed @ Very Little Energy-Cost



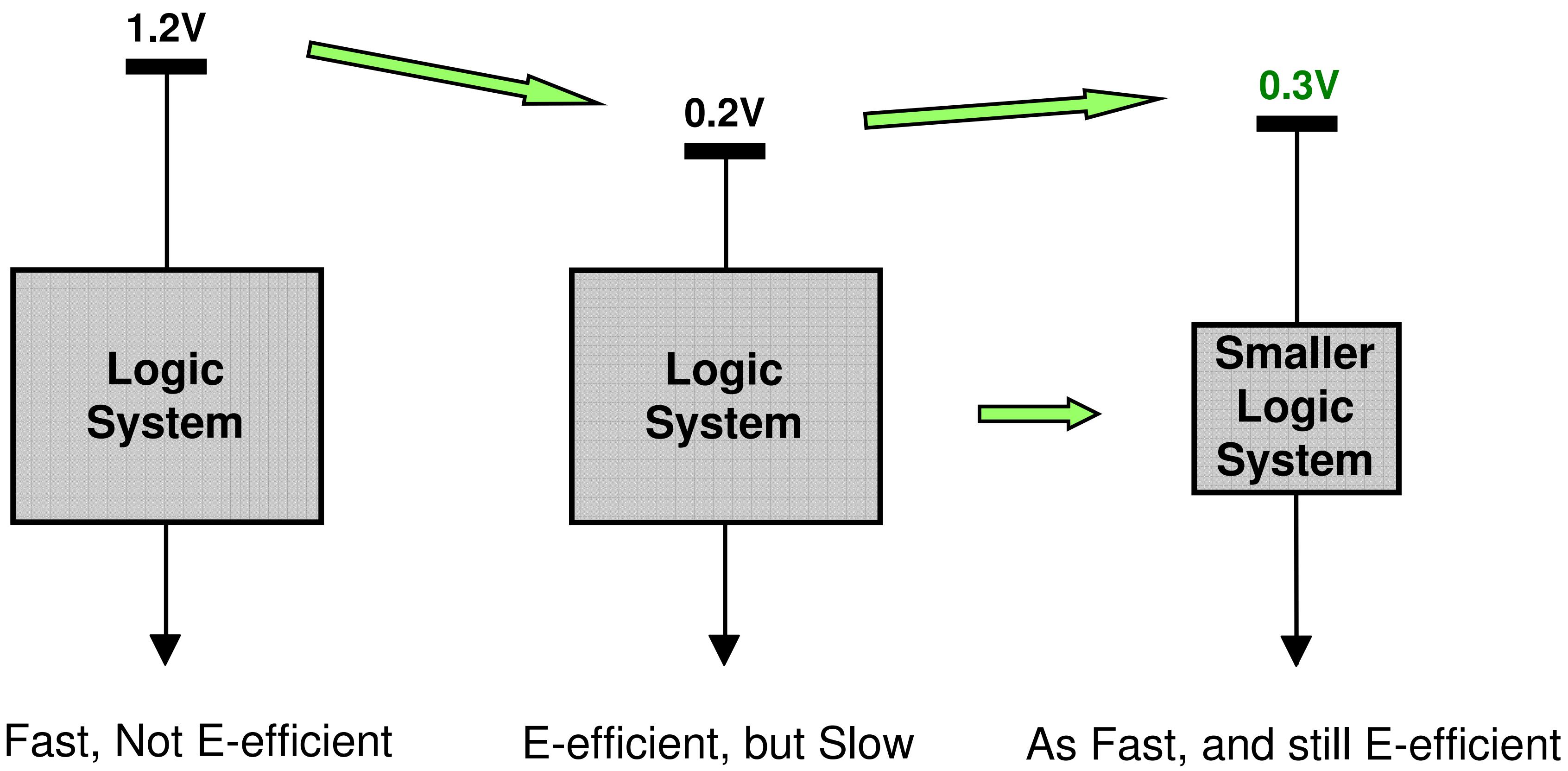
Note: Normalized Data

Sub-V_T: Helps Increase Speed @ Very Little Energy-Cost



Note: Normalized Data

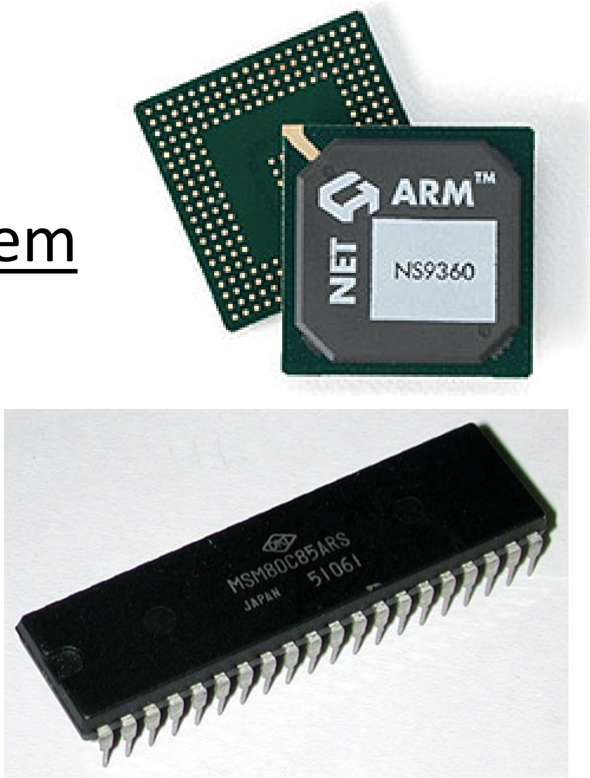
Making the Small, Slow Topology Faster



How do we make the Logic System Smaller & Less Leaky ?

Small, Less Leaky Systems: By Lowering System Level Bit Width

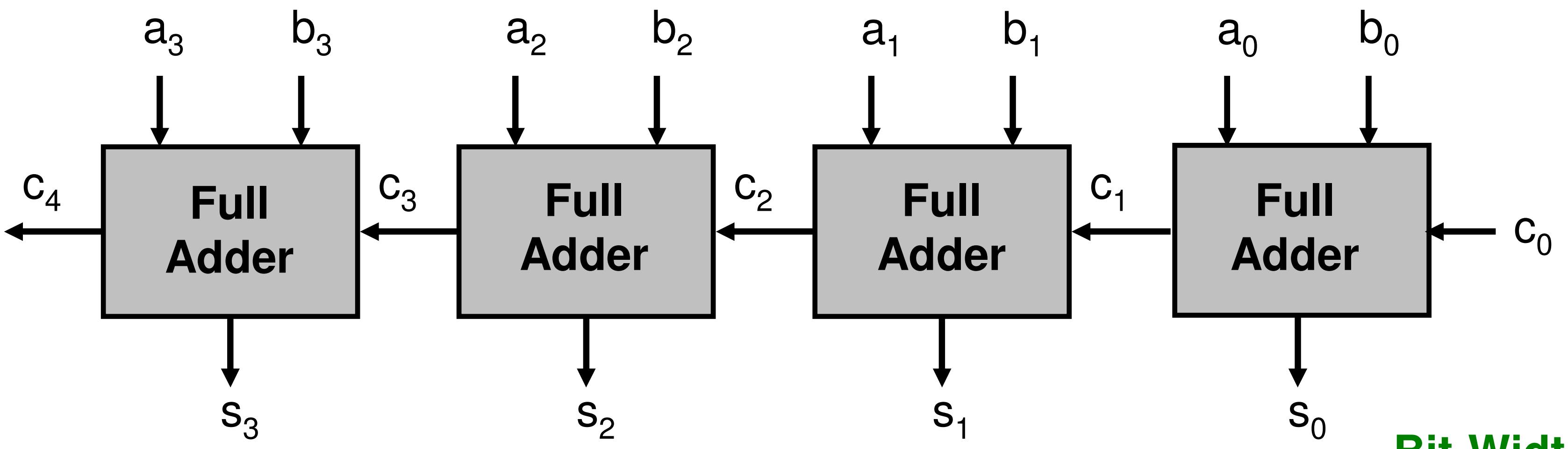
- What is System Level Bit Width?
  - Number of bits processed concurrently
  - System Bit Width = 1 => Fully Serial System
- Smaller Bit Width means:
  - Less number of leakage paths
  - But… More cycles needed to finish the same operation



Varying System Bit Widths: Intel 8 bit and ARM 32 bit processors

Why Lesser Leakage ?

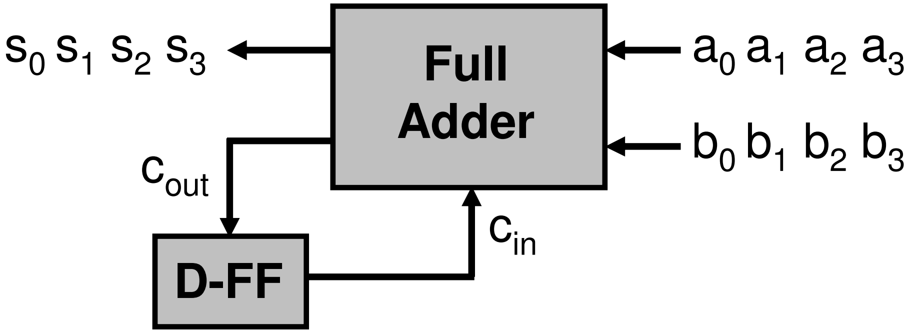
4b Ripple Carry Adder:



Bit-Width = 4

Serial Adder:

- **Needs 4 cycles**
- **Lesser I_{lkg}**



Bit-Width = 1

Lowering System Level Bit-Width

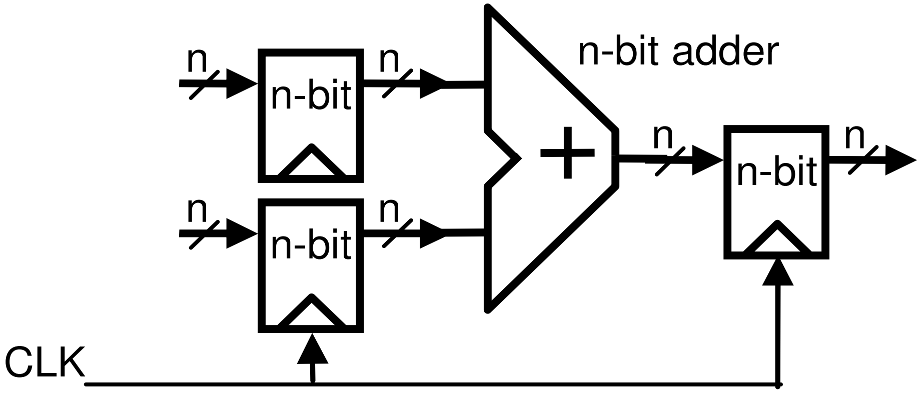
Systems compared:

- 1b SA-1
- 16b KSA-16
- 32b KSA-32

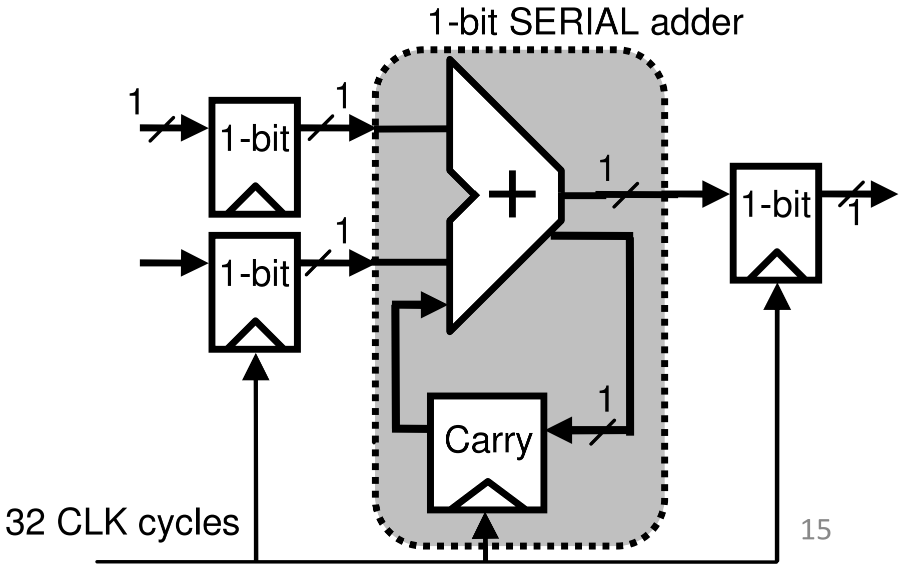
SA : Serial Adder

KSA: Kogge-Stone Adder

32b KSA-32 or 16b KSA-16



1b SA-1



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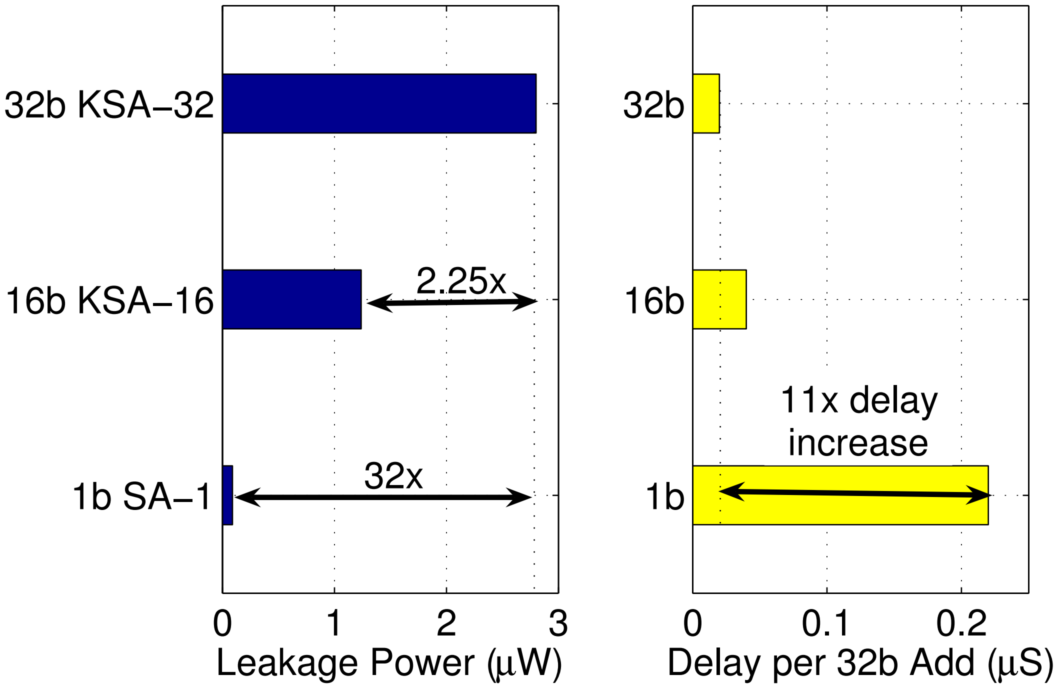
- **Serial Components in Parallel Systems**

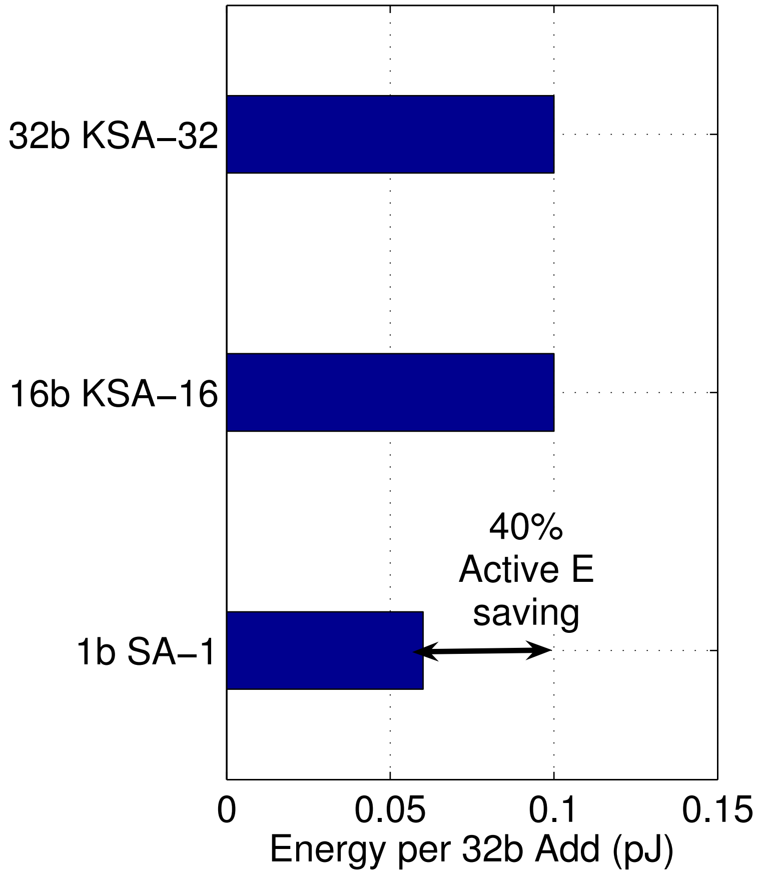
Leakage and Delay @ Equal VDD



Serial Systems Help Lower I_{lkg}

VDD = 300mV, data using 22nm PTM

Active E @ Equal VDD



Serial Systems help LOWER Active E :

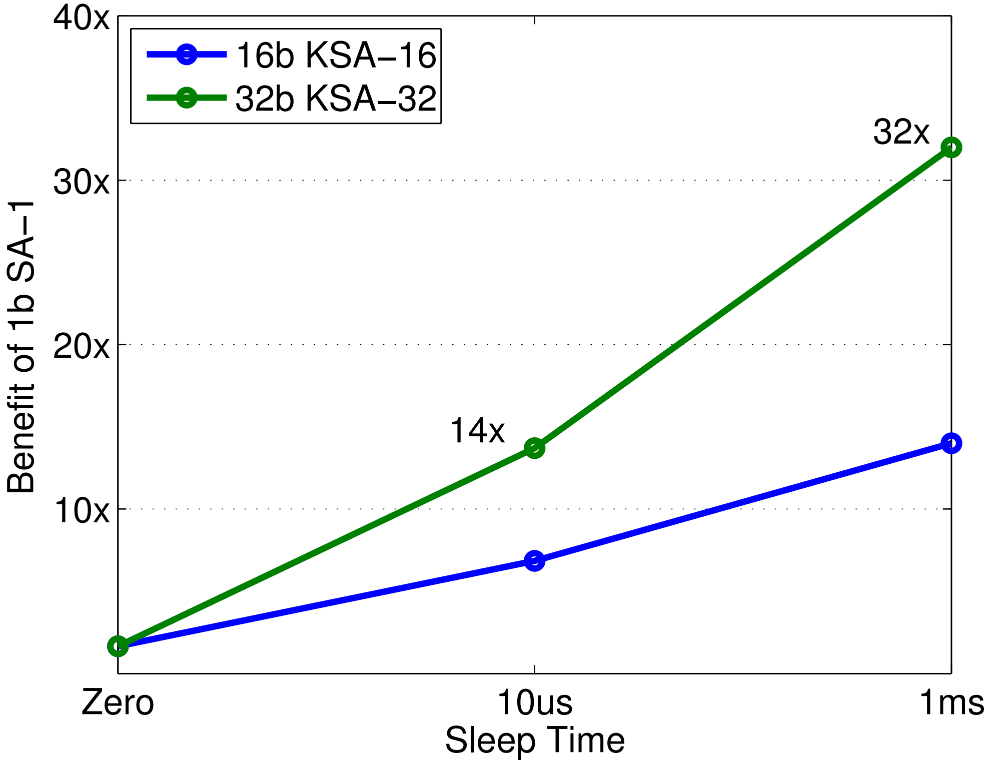
– Almost no glitching

– Super-linear Area saving

VDD = 300mV, data using 22nm PTM

Total E @ Equal VDD

Sleep Time	Total E Consumed (pJ)		
	1b SA-1	16b KSA-16	32b KSA-32
Zero	0.06	0.10	0.10
10us	0.07	0.48	0.96
1ms	2.72	38.10	85.90



Higher the sleep time, higher the benefit of a Serial System

We take $I_{lkg\_sleep} = 0.1 * I_{lkg\_active}$

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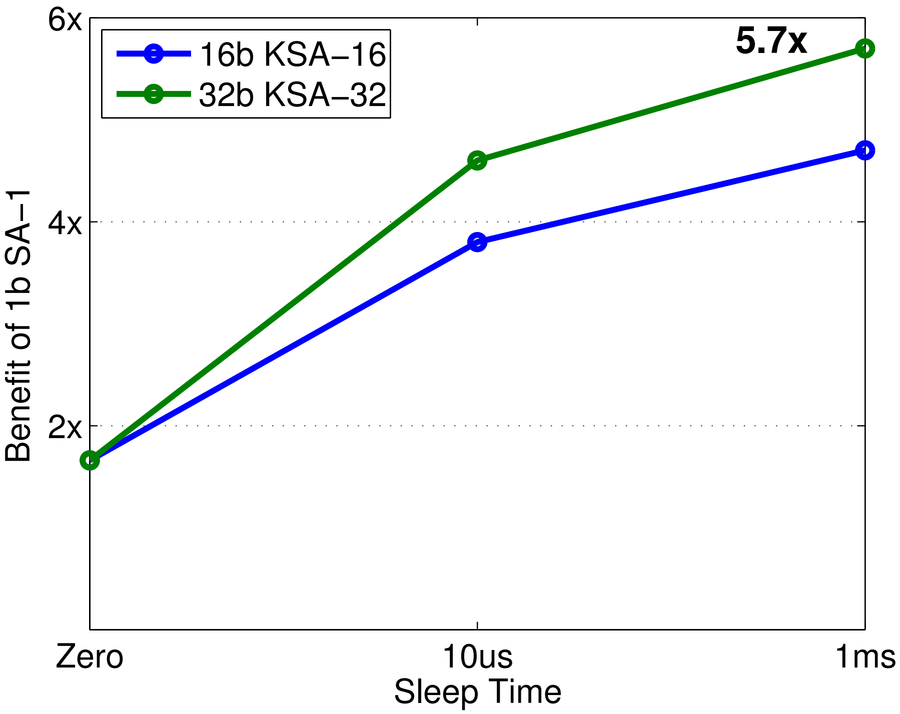
Active & Total E @ Equal Speed

Sleep Time	Total E Consumed (pJ)		
	1b SA-1	16b KSA-16	32b KSA-32
Zero	0.06	0.10	0.10
10us	0.21	0.80	0.96
1ms	14.90	70.50	85.90
VDD used	350mV	250mV	200mV



Even at the higher VDD a Serial System has lower:

- **Active E**
- **Sleep E**

Note: Delay kept at 0.1us

Conclusions @ Equal Delay

- ✓ **In Sub-V_T, at slightly higher VDD, a Serial System becomes as fast as a Parallel System**
- ✓ **Even at the higher VDD, a Serial System has lower Active E & Sleep E**

The constraint is that the ENTIRE system must be Serial

Vision of a Fully Serial System

- What’s already being done serially?
  - Successive Approximation Register (SAR) ADC
  - Radio / Wireless Communication

- Thus, i/p and o/p are already serial

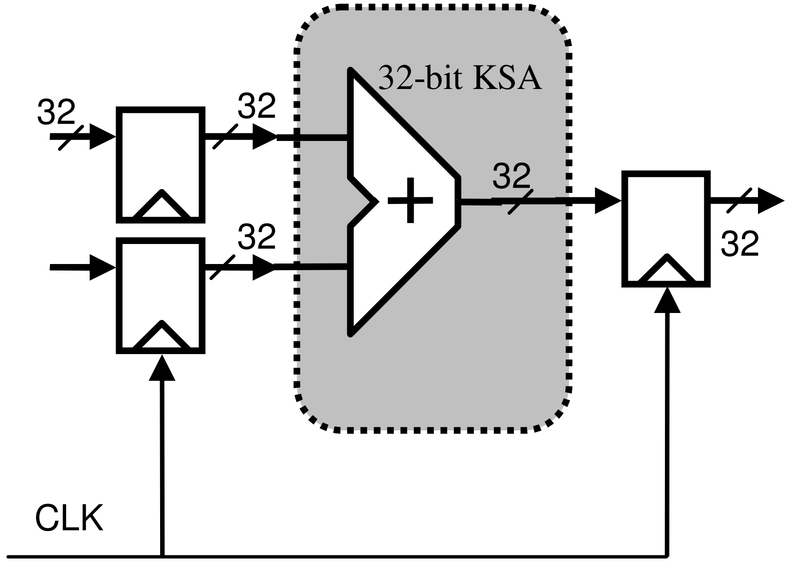
- Examples of Serial Architectures:
  - Serial DSPs (Distributed Arithmetic, R. Amritharajah, et al, 2005)
  - Serial Architectures used in RFID chips

Serial Components in Parallel Systems

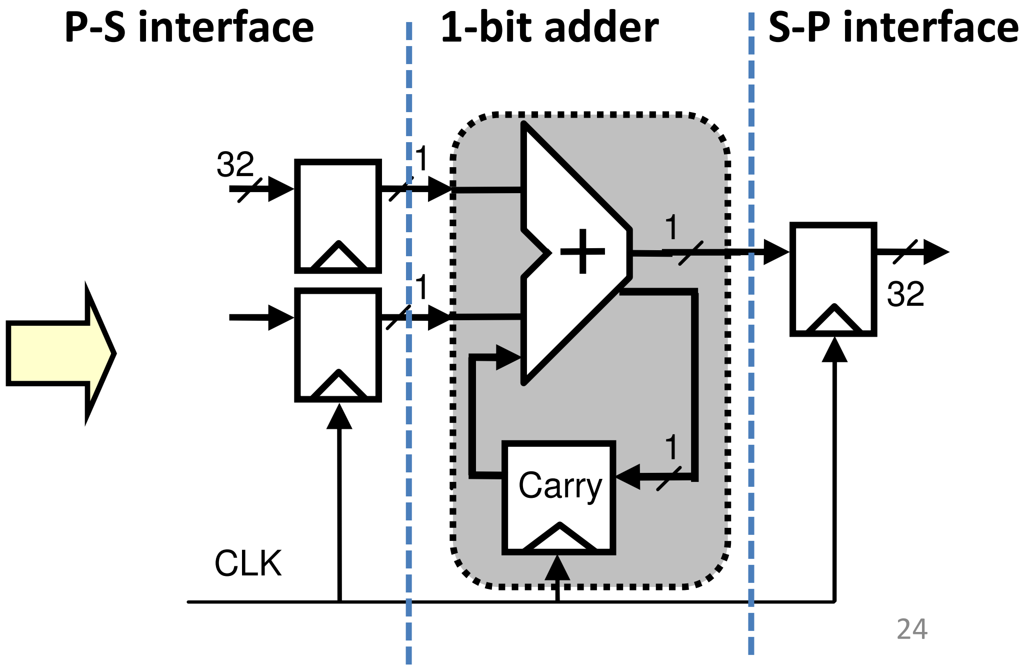
P-S and S-P interfaces will have:

- Active E overhead
- But we still get Leakage Current benefit

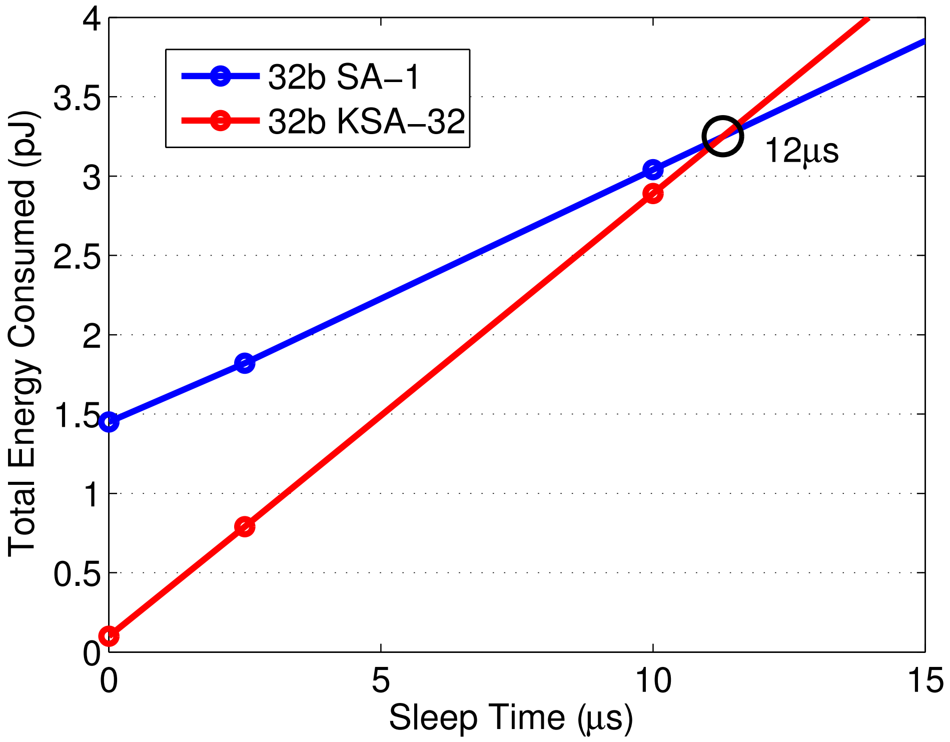
32b addition system with 32b KSA



32b addition system with a SA



32b system with a Serial Adder block



Parallel System with a Serial Adder Block:

- Has Higher Active E
- **But Helps Save Sleep E**

Contributions

- Small Bit-Width systems help save:
  - Active Mode E & Sleep Mode E
  - Can operate as fast as parallel systems by increasing VDD

- In the sub-V_T regime:
  - Simple topologies are more E efficient
  - Speed can be increased by increasing VDD @ little E cost

- Be flexible to “Re-Think the Topology”
  - As “porting” doesn’t lead to most E-efficient solution
  - Specially when design constraints change significantly

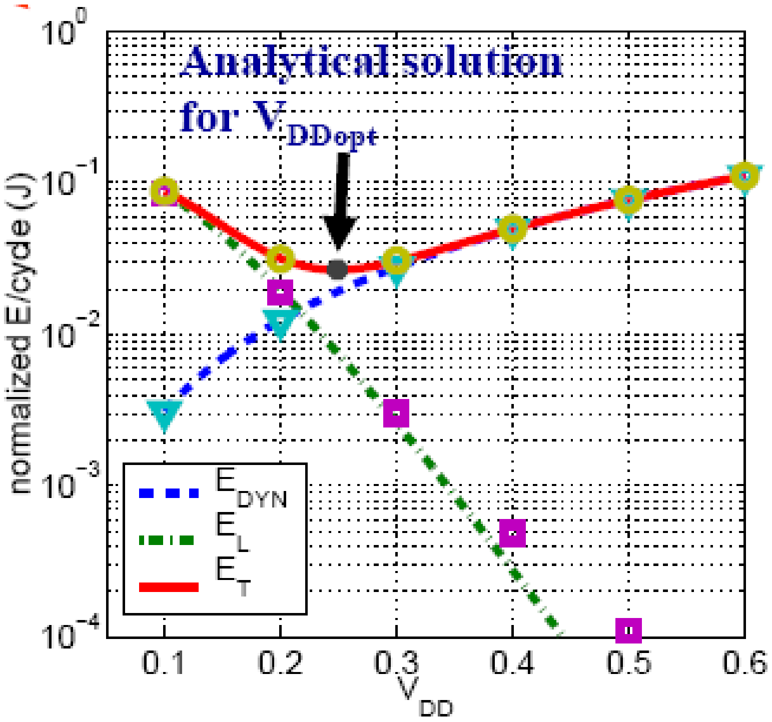
Thank you for your Time !

Backup slides ahead

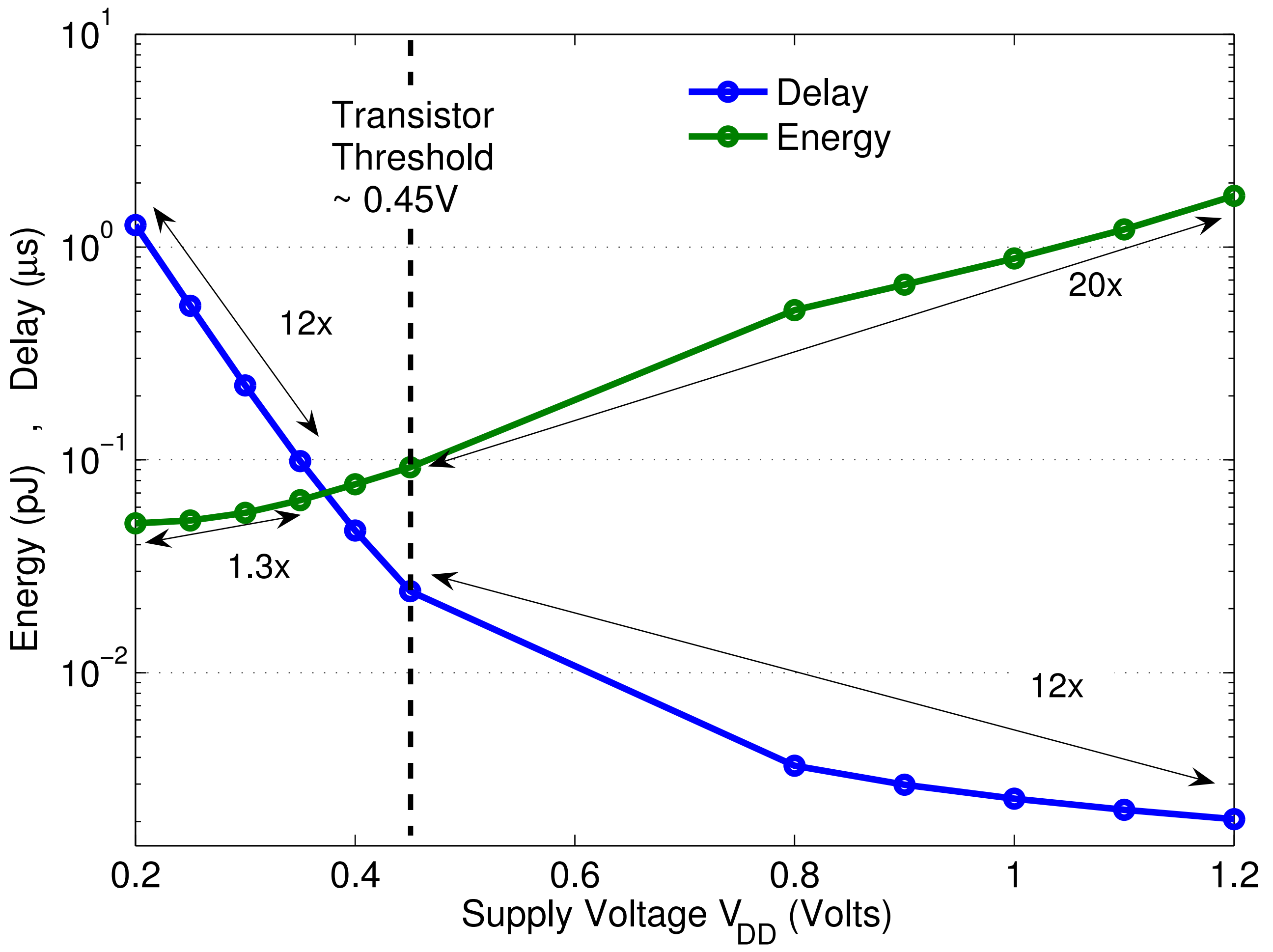
ULP applications and Sub-V_T

- Energy consumed <u>per operation</u> is minimized with VDD in Sub-V_T

- As VDD increases:
  - Delay decreases
  - => Leakage energy decreases
  - Dynamic energy increases
  - Total energy demonstrates a minima



Energy, Delay eqns above and below V_T are DIFFERENT



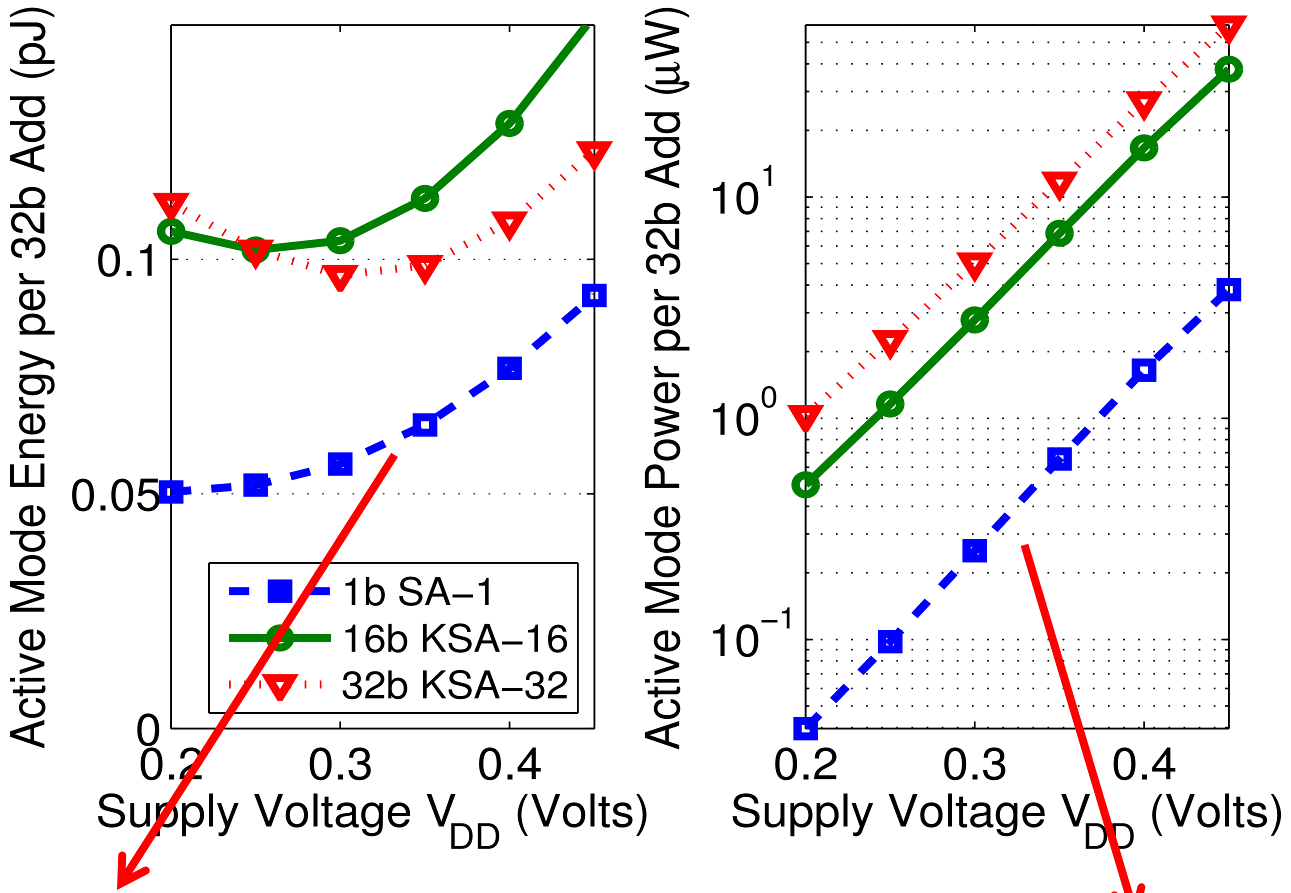
In Strong Inversion:

12x Speed-up costs
20x in Energy

In Sub-V_T:

12x Speed-up costs
ONLY 1.3x in Energy

Results across a VDD range



✓ **Active energy of 1b system < 32b system at all VDD points**

✓ **15x benefit in Active Mode POWER at all VDD points**

Equal Delay vs Equal VDD

Topology	Zero Sleep	10µs	1s	P_{lkg}	V_{DD}
1b SA-1	0.06	0.21	14919	0.15	0.35
16b KSA-16	0.10	0.80	70552	0.70	0.25
32b KSA-32	0.10	0.96	85852	0.86	0.20

All systems working @ 10MHz

@ 1 SEC sleep time, 1b system has **5.7x lesser** E than 32b system

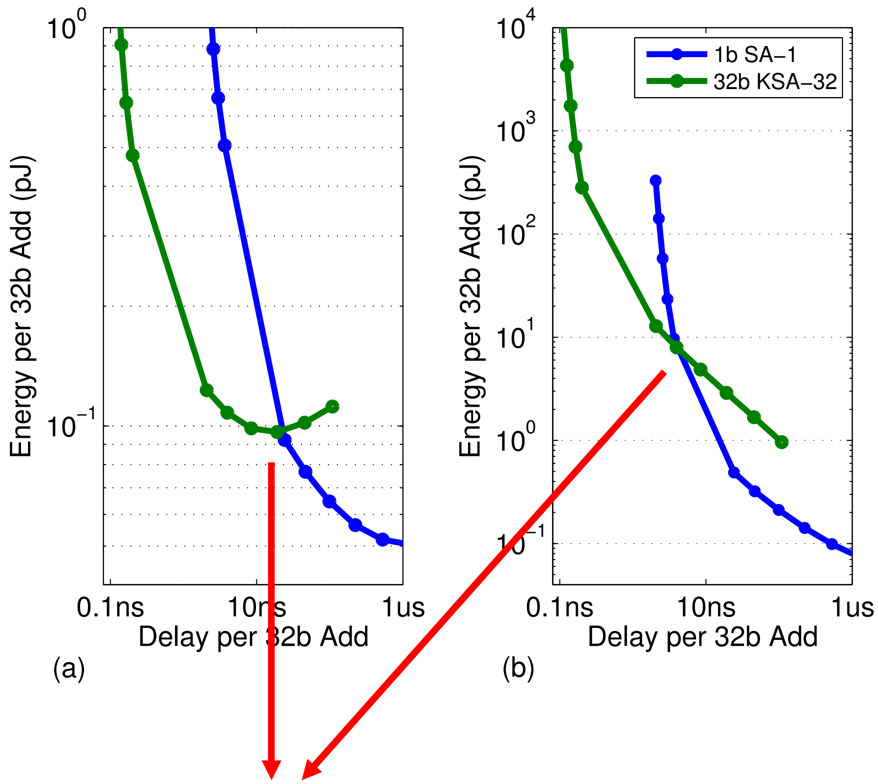
Topology	Zero Sleep	10µs	1ms	1s
1b SA-1	0.05	0.07	2.72	2723
16b KSA-16	0.10	0.48	38.10	38096
32b KSA-32	0.10	0.96	85.85	85852

All systems working @ equal VDD

@ 1 SEC sleep time, 1b system has **32x lesser** E than 32b system

At EQUAL DELAY, 1b systems are STILL MORE E efficient than 32b systems, though the benefit comes down from 32x to 5.7x

Serial Systems become Pareto-optimal in Sub-V_T

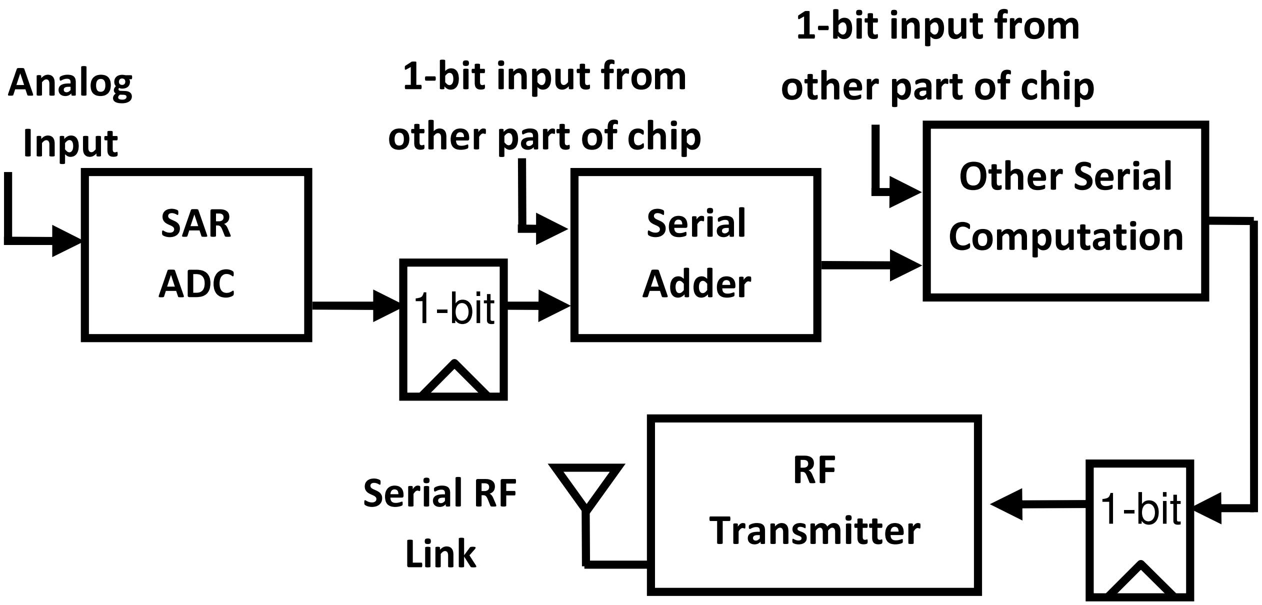


Pareto-optimal E-D curves across sub-threshold and strong-inversion:
(a) active mode energy
(b) total energy with 10μs of sleep time.

Below a certain E-D point, 1b system has lesser energy for the same delay

Vision of a Fully Serial System

- Data enters 1b per clock cycle
- Every 32 cycles, a word:
  - Streams through the system
  - Undergoes processing
  - Is Communicated off-chip using the wireless link.


Analog Input
SAR ADC
1-bit
1-bit input from other part of chip
Serial Adder
1-bit input from other part of chip
Other Serial Computation
1-bit
RF Transmitter
Serial RF Link