A 2.6-µW Sub-threshold Mixed-signal ECG SoC

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Abstract

This paper describes a 0.13-µm CMOS sub-threshold (sub-V_T) mixed-signal system-on-chip (SoC) that acquires and processes an electrocardiogram (ECG) signal for wireless ECG monitoring. The SoC uses a sub-threshold digital microcontroller (µC) for adaptive control of the sub-V_T biased analog components and for processing the ECG data. The µC operates from 0.24 V to 1.2 V and consumes as little as 1.51 pJ per instruction. The SoC consumes only 2.6 µW while providing either heart rate or ECG data.

Keywords: sub-threshold, mixed-signal, SoC, ECG, sensor

Ultra Low Power Mixed-Signal ECG SoC

We use sub-threshold circuits to minimize digital power consumption of our µC and to reduce system power. For example, the radio will dominate energy consumption in a wireless ECG sensor that streams ECG data. We repartition the ECG system to increase computation on the sensor node in the sub-V_T digital block, thereby significantly reducing the wireless channel data rate whenever possible (by up to 500X) and lowering system power.

Our SoC for wireless ECG monitoring combines an instrumentation amplifier (IA), an 8-bit analog-to-digital converter (A/D), and a sub-V_T µC. The SoC communicates with an off-chip radio via an on-chip UART. Fig. 1 shows the SoC architecture and voltage domains. Unlike previous ECG monitors [1][2], our SoC uses sub-V_T digital components (0.24 V to 0.5 V) and sub-V_T biased analog circuits to minimize power. Our approach leverages ultra low power (ULP) digital computation for adaptive control of the analog front-end and on-chip calculation of heart rate.

A. Analog Front-End

A simple differential IA topology based on [3] was chosen for the ECG amplifier. This topology reduces common-mode interference and DC offset at the ECG input using continuous offset control. The µC can also digitally control the IA's gain to use the full A/D range without clipping. An 8-bit A/D digitizes the amplified ECG signal at a 1 KHz sampling rate. Fig. 2 shows the dual-slope integrating A/D chosen for the low sampling rate, low noise, and low power consumption. The A/D does not require any resistors, and the current-source transconductance and integration capacitance do not have to be matched to any precise value. By adjusting the A/D supply voltage, fidelity can be traded for reduced power consumption.

B. Sub-threshold Digital Design

We designed a custom variant of the PIC16C5X series with a two-stage pipeline to meet the ECG processing needs. The customized µC has a 24-byte register file with 31 instructions and includes seamless state transition interrupts. The interrupts allow for context switching without the overhead of pushing values onto the stack. This is an important feature since interrupts from the A/D, UART, and timer drive the µC operation. We used a customized flow to synthesize the sub-V_T core. A custom tool characterizes library cells over all input combinations at the desired operating frequency, across process corners, and sub-V_T voltages. We replace cells that fail at low V_{DD} during the synthesis process. Our flow also uses Monte Carlo simulation to detect and correct hold time violations, since short register-to-register paths are more sensitive to variation in sub-V_T.

We designed a custom level converter to interface 0.25 V digital blocks to 1.2 V regions of the chip (Fig. 3a) without requiring additional voltage rails. Variation leads to large changes in the I_{on}/I_{off} ratio that make level conversion difficult. We avoid the use of zero-V_T devices [4] and intermediate supplies [5] with the use of diode-connected NMOS FET M5 to mitigate the P/N drive mismatch inherent to level conversion circuits. High V_T devices are also used to further improve the low voltage sensitivity. Fig. 3b shows robust operation across process corners and local variation to a very low V_{DD}.

Experimental Results

We fabricated the SoC in a 0.13-µm CMOS process with $I_N/I_P \approx 7$ (typical) at 0.3 V. Fig. 4 shows the IA's frequency response with the analog offset control enabled, which reduces the IA's input referred offset from 1.2 mV to less than 2 µV. The µC can adjust the IA gain from 20 dB to 42 dB, varying IA power from 0.934 µW to 1.55 µW. The analog portion of the A/D (sample and hold, the transconductance amplifier, integration capacitor, and comparator) operates from 1.2 V down to 0.5 V, with a tradeoff between power and effective number of bits (ENOB) shown in Fig. 5a. Fig. 5b shows the A/D's INL and DNL at 1.2 V. A/D metrics are slightly degraded due to a few missing codes near zero.

The sub-V_T µC is fully functional from V_{DD} of 1.2 V down to 240 mV. Fig. 6a shows the frequency and energy per instruction for the µC in sub-V_T (die photo in Fig. 6b). The minimum energy voltage for the µC is 280 mV (1.51 pJ/instruction, 475 KHz), where it remains fast enough to perform heart rate computation with 1 KHz sampling. Fig. 6c shows E/instruction vs. MIPS for our µC (logic, register file, and clock net) relative to previously published sub-V_T processors (cores only, not memory inclusive), which use different instruction sets. The level converter works below 180 mV (measurement limited by standard cell register failure).

Fig. 7 shows the results of the SoC processing an ECG waveform. The SoC can reduce the wireless data rate by 500X by computing the heart rate intervals from the ECG signal (Fig. 7a). As shown in Fig. 1, the A/D can also directly capture external signals, bypassing the IA (Fig. 7b). The heart rate algorithm is robust to many parameters, including excess noise in the IA revealed by our test setup, power-saving reduction of A/D V_{DD}, and ENOB. The algorithm has detected the peaks of a representative 60-second ECG sample with 100% sensitivity at A/D V_{DD} from 1.2 V down to 0.5 V with root-mean-square peak-to-peak interval errors less than 8 ms. The combined power consumption of the analog front-end (V_{DD} = 0.8 V) and the µC (V_{DD} = 0.28 V) is 2.6 µW, significantly less than previously published results [1][2].

Conclusion

We have presented the design and implementation of a mixed-signal ECG SoC that integrates sub-V_T analog and

digital circuits. Low-energy operation of the digital logic is sufficient to adaptively adjust analog components and to compute accurate heart rates in the presence of noise and degraded analog performance. Leveraging ULP sub-V_T digital computation permits low-power heart rate monitoring (with lower analog V_{DD}) and high fidelity ECG when necessary. The design of this SoC lays the groundwork for other adaptive, low-power body sensor applications.

References

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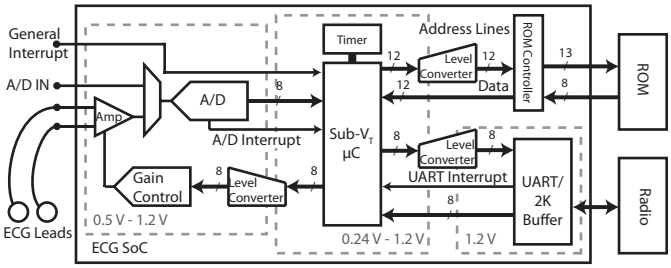

Fig. 1 ECG mixed-signal SoC block diagram.

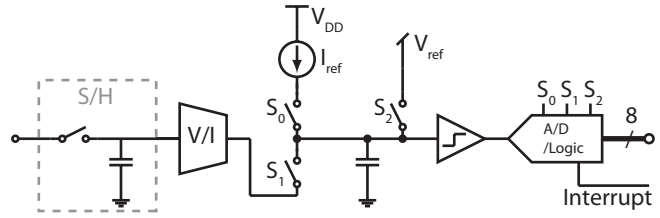

Fig. 2 8-bit, dual-slope integrating A/D.

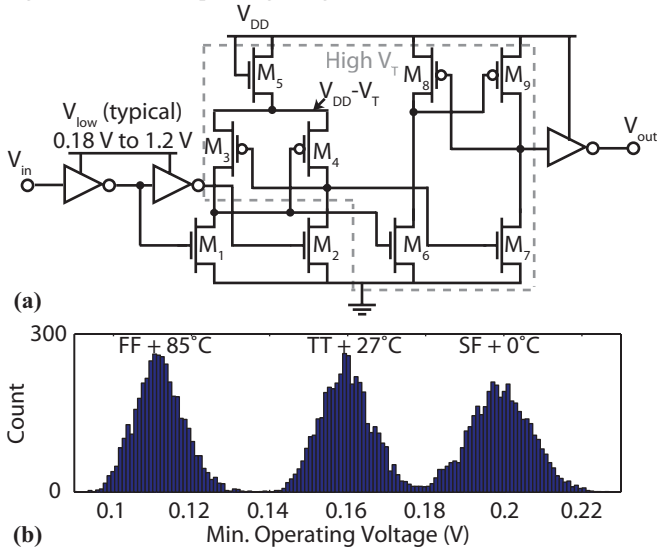

Fig. 3 (a) Level converter schematic for sub-V_T to full V_{DD} conversion. (b) Histogram of level converter's min. operating voltage due to variation.

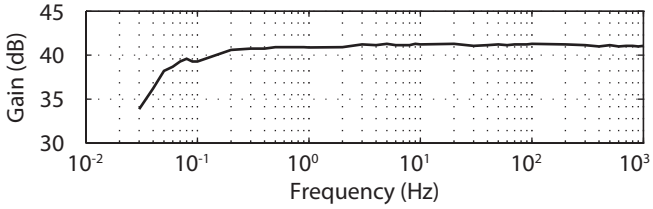

Fig. 4 Measured IA frequency response with offset control enabled.

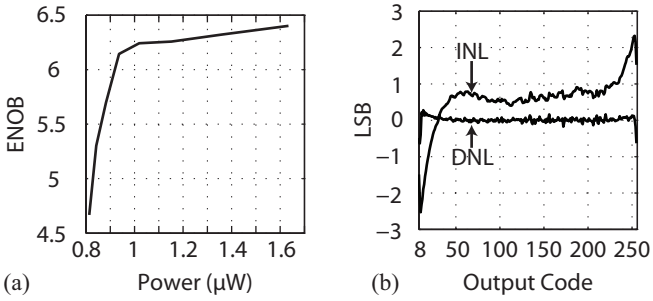

Fig. 5 (a) Effect of power scaling on A/D ENOB. (b) Measured A/D DNL and INL at 1.2 V, calculated over valid range of codes.

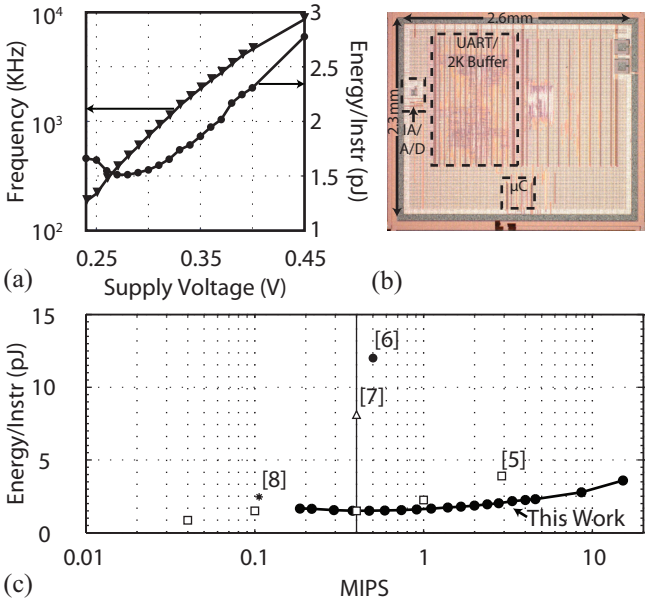

Fig. 6 (a) Microcontroller frequency and E/Instr measured in sub-V_T. (b) Photograph of the chip. (c) MIPS and energy consumption comparison to prior work, solid line indicates 0.4 MIPS requirement for heart rate detection algorithm.

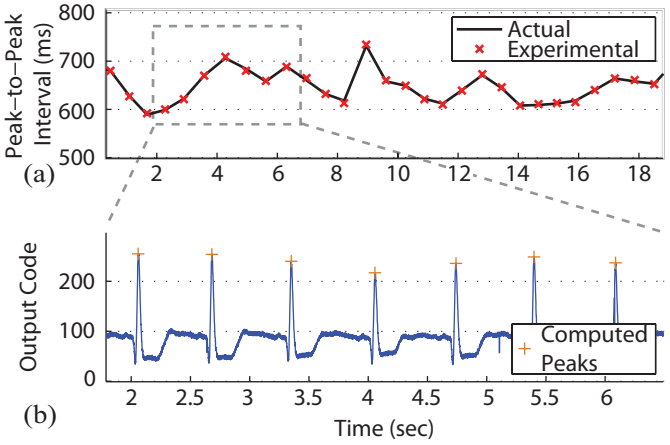

Fig. 7 (a) Measured heart rate computations performed on-chip. (b) ECG signal obtained through SoC A/D.