Improving Reliability and Energy Requirements of Memory in Body Sensor Networks

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Abstract — This paper evaluates the impact of different peripheral write assist techniques on the reliability and energy efficiency of Static Random Access Memory (SRAMs) in Body Sensor Networks (BSNs). The results of this characterization show that the best choice for a supply voltage and write assist combination varies based on the system level constraints and objectives. Further, factors outside the accessed cells such as half select stability dictate the optimal assist choice, the extent to which the assist should be applied, and the total array energy. Using data from a thorough study of assist options across V_{DD}s, we establish strategies for supply voltage and assist selection based on system constraints to reduce the array energy. While V_{DD} lowering assist technique provides the lowest array energy per operation of 8.5pJ at 0.5V when write delay is not constrained, negative bitline (NegBL) improves the write speed by 121X at the same voltage with 23pJ of energy.

Keywords—V_{MIN}, high-V_T, Sub-threshold, reliability, WM, Write HSNM, and Read HSNM

I. Introduction

The need for sustainable and energy-constrained Body Sensor Networks (BSNs) systems-on-chip (SoCs) for personal healthcare, bio-security, etc. increased significantly with the recent increase in ubiquitous sensors around human life. The challenge of such applications changed from the traditional performance driven application space to reliability, low-energy, and security. At the same time, the increase in memory capacity on SoCs used for BSNs and its large contribution to the system energy [1][2] necessitate the re-evaluation of its design to ensure reliability and minimize its contribution to the SoC energy. However, reducing energy by V_{DD} scaling causes reliability concerns and limits V_{MIN} [3]. This paper addresses the energy and reliability challenges by characterizing the energy, write stability, and minimum achievable V_{DD} of a low power high-threshold (V_T) 8T SRAM [4] array when using different write assist techniques.

II. Reliability Improvement Using Write Assist

For energy-constrained applications [1], guaranteeing functionality at or below the transistor V_T becomes a major concern. To quantify the impact of each assist technique on the reliability of the write operation, we use the write margin (WM) metric. Figure 1 a) shows the trends of WM across supply voltages for different assist techniques with different degrees (percentage of V_{DD}) of assist applied [5]. Interestingly, the assist that provides the best WM varies depending on the operating voltage and the degree of assist applied. Wordline (WL) boosting provides the largest improvement in WM among the assist techniques for V_{DD}s above 0. For supply voltages below 0.5V, V_{DD} lowering gives the highest WM. This change is due to the change in the sensitivity of WM to changes in the V_T of the pull-up (PU) and pass-gate (PG) transistors when V_{DD} is lowered. Weakening the PUs through V_{DD} lowering has a greater impact than making the PGs stronger using WL boosting at low V_{DD}s. As applying higher degrees of assist impacts the hold ability of row and column half-selected (HS) cells, Figure 1 b), captures the Write HSNM and Read HSNM (RSNM) at different V_{DD}s and write assist degrees.

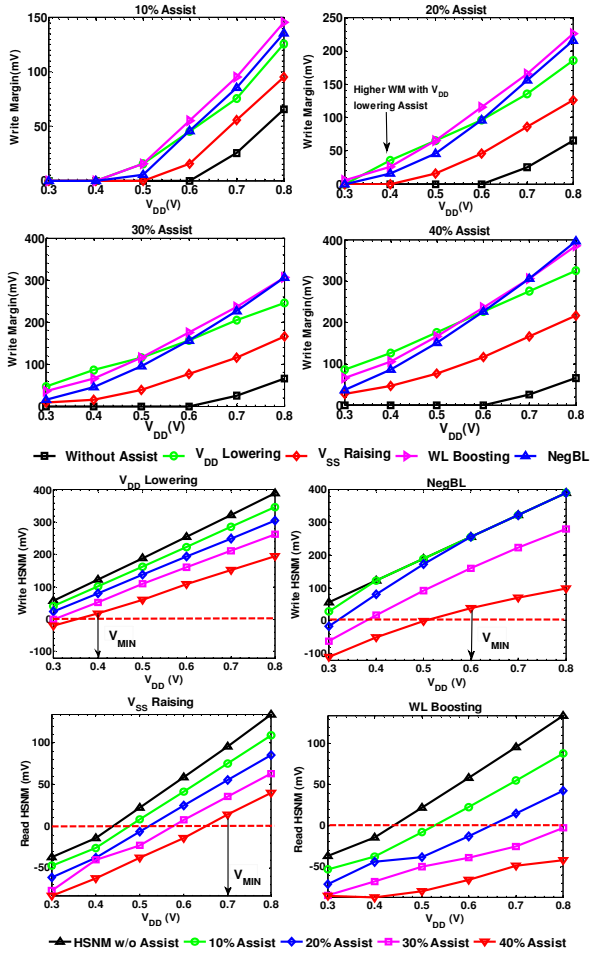

Figure 1: Impact of assist techniques on: a) WM b) Read and Write HSNM.

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TABLE 1: RANGE OF V_{DD}S AND APPLIED ASSIST FOR THE RELIABLE WRITE OPERATION ON THE ARRAY

V_{DD} (V)	Achievable range of applied assist(% of supply)			
	V_{DD} Lowering	V_{SS} Raising	WL Boosting	NegBL
0.5	10 – 40%	X	X	10 – 30%
0.6	10 – 40%	10 -30%	10%	10 – 40%
0.7	0 – 40%	0- 40%	0 – 20%	0 – 40%
0.8	0 – 40%	0 -40%	0 – 20%	0 – 40%

Based on the data from Figure 1, TABLE 1 summarizes the range of assist that can be applied at a given V_{DD} for the considered assist techniques.

III. ENERGY MINIMIZATION USING ASSIST TECHNIQUES

We evaluate the effectiveness of write assist techniques for reducing the total write energy as: 1) WM vs total write energy (i.e. the energy consumed by an array for a reliable operation), and 2) total write energy vs. write delay (i.e. the energy required for a given performance). The 1KB array energy reported includes the row and column drivers with their parasitic, the pre-charge circuit, and the SRAM cells. We divide the total array energy into five components as:

$$E_{1\,KB\,Array} = E_{BL} + E_{WL} + E_{CF} + E_{HS} + E_{Leak} \quad (1)$$

where, E_{BL} is the selected cell BL driver/pre-charge energy, E_{WL} is WL driver energy, E_{CF} is the energy drawn from the cell V_{DD} when the node are flipping, E_{HS} is the energy dissipated in HS cells, and E_{Leak} is the leakage energy of the unselected cells.

Figure 2 a) shows the Energy Optimal Contours (EOC) of different assist techniques connecting WM-energy optimal points. Here, the non-assisted array can also provide an energy optimal choice at higher V_{DD}s. For V_{DD} lowering, 40% assist can be applied to achieve a V_{MIN} of 0.5V that also provides the optimal energy for a given WM. Figure 2 a) suggests different strategies for trading off energy, margin, and V_{MIN} for a given system level constraint on energy. Figure 2 b) shows the optimal energy/operation for a given delay for different V_{DD}s and applied assist. Even though V_{DD} lowering reduces V_{MIN} down to 0.5V and minimizes the total energy (E_{MIN} = 8.5pJ), it incurs a significant delay penalty. V_{DD} lowering at V_{DD}=0.5V is 121X slower compared to NegBL at V_{DD}=0.5V with 23pJ of total energy, and ~800X slower than WL boosting at V_{DD}=0.6V while consuming 12.8pJ.

IV. CONCLUSION

In this paper, we evaluated different write assist techniques for minimizing SRAM array write energy to enable energy-constrained BSN SoCs. Based on this study, we conclude the following: 1) the reliability (WM) trend of write-assist techniques in sub-threshold are different than super-threshold thus the assist design decisions will be different for a given system level constraints in sub-threshold, 2) V_{DD} lowering provides maximum V_{DD} scaling down to 0.5V with the least energy, but negatively impacts write delay, 3) NegBL provides the optimal solution for higher performance (speed) with a marginally higher energy at 0.5V compared to V_{DD} lowering, and lower robustness, and 5) WL boosting shows the energy/operation optimal solution for a system operating at higher V_{DD}s. In conclusion, this paper provides an in depth system-level evaluation of assist techniques studying the different trade-offs between the array V_{MIN}, array E_{MIN}, write reliability, and performance for reliable and energy-constrained BSN applications.

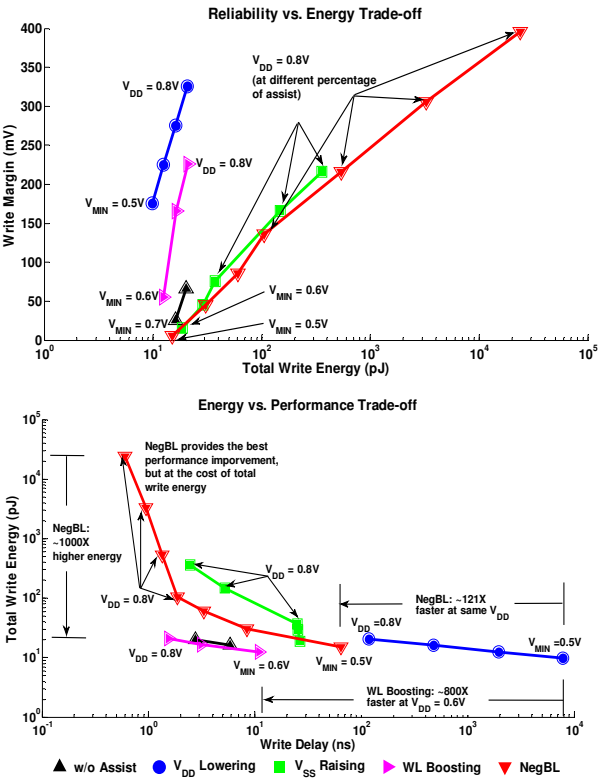

Figure 2: a) WM vs. total write energy trends and (b) total write energy vs. write delay (performance) contours for different assist techniques with achievable array V_{MIN}

I. ACKNOWLEDGMENT

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