Improving Dynamic Leakage Suppression Logic with Forward Body Bias in 65nm CMOS

Daniel S. Truesdell and Benton H. Calhoun
Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA, USA
Email: dst4b@virginia.edu

Abstract—This paper investigates the effect of body biasing on the leakage and delay of dynamic leakage suppression (DLS) logic. We present a brief theoretical analysis of the impact of body biasing on DLS logic as well as measurements from a test chip in 65nm CMOS. Results show that forward body biasing can reduce delay by up to 41X with negligible impacts on leakage.

I. INTRODUCTION

Steady growth of the IoT has created a landscape of low-power sensor nodes for data acquisition and event detection in a variety of applications such as structural and environmental monitoring. For maximum sustainability, sensor nodes must be reliable and low-maintenance. To address this need, nodes operate at ultra-low power levels and can additionally harvest their own energy in order to extend battery lifetime. In digital circuits, power reduction has been achieved by scaling down supply voltage to the subthreshold domain and limited operating frequency to the kHz-range or lower. At this point, leakage currents dominate total digital circuit power and can still be significant, consuming 10’s to 100’s of nW unless the circuit is completely power gated. To continue digital circuit power reduction, direct efforts to reduce leakage current are required [1]. Dynamic leakage suppression logic [2], [3] achieves ultra-low leakage that is well-suited for IoT applications but comes at the cost of severely degraded operating frequency. Efforts to improve the speed and flexibility of DLS logic have required additional transistors [4], [5] since there are not any known intrinsic knobs (such as supply voltage) for strongly tuning performance. In this paper, we propose a body biasing technique for DLS logic as an intrinsic performance knob and investigate its impact on leakage and delay. We first review the operation of DLS logic and provide a brief theoretical analysis of the impact of body biasing on DLS logic performance. Finally, we present measurements from a test chip fabricated in 65nm CMOS.

II. OPERATION AND BODY-BIASING OF DLS LOGIC

Fig. 1 shows a standard DLS logic gate (a) and the proposed body-biased DLS gate (b). During the steady state, the standard DLS logic gate strongly reduces subthreshold leakage through the inactive pull-up (M_{HN}, M_{PX}) or pull-down (M_{NX}, M_{FP}) network by leveraging the stack effect to force the devices into super-cutoff mode where V_{GS} is less than 0V (Fig. 2). The strength of this leakage-reduction effect is dependent on 1) leakage mechanisms such as gate leakage, junction leakage, gate-induced drain leakage (GIDL), and band-to-band tunneling at negative V_{GS} which counteract the subthreshold leakage reduction, and 2) the relative leakage between the inactive devices which influences the steady-state voltage of V_{t}. To calculate the leakage current of the DLS pull-up network in Fig. 2 we begin with the standard subthreshold current, which is expressed as

\[ I_{DS} = I_0 e^{(V_{GS} - V_{t}(1 + \eta) - V_{SB}) / \eta kT} \left( 1 - e^{\eta kT / V_{SB}} \right) \]

(1)

where \( n \) is the subthreshold swing ideality factor, \( \nu_T \) is the thermal voltage \( kT / q \), \( V_{t0} \) is the nominal threshold voltage, \( \eta \) is the DIBL coefficient, \( k_T \) relates the body effect coefficient \( \gamma \) and the surface potential \( \phi_B \) by \( k_T = \gamma / 2 \sqrt{\phi_B} \), and \( I_0 \) is the current at threshold given as

\[ I_0 = \mu_Core \frac{W}{L} (n-1) \nu_T^2 \]

(2)
Assuming $V_{DD} \gg kT/q$, $V_s$ can be solved by equating the subthreshold current through $M_{HN}$ and $M_{PX}$:

$$V_s = \frac{k_\Gamma V_{BN} + V_{DD}(\eta + 1) + \Delta V_{t0} + n_vT \ln \left( \frac{i_{op}}{i_{0n}} \right)}{2 + 2\eta + k_\Gamma}$$

(3)

Where $\Delta V_{t0} = V_{in0} - V_{tp0}$ is the difference in the nominal threshold voltages of $M_{HN}$ and $M_{PX}$ and $i_{0n}, i_{op}$ are the nominal threshold current of $M_{HN}$ and $M_{PX}$, respectively. Note that if $M_{HN}$ and $M_{PX}$ are identical ($i_{op} = i_{0n}$ and $\Delta V_{t0} = 0$) and we neglect DIBL and the body effect, $V_s$ simply becomes $V_{DD}/2$.

The leakage current of $M_{HN}$ can be solved using (3) along with (1)–(2)

$$I_{OFF,M_{HN}} = i_{0n} e^{\frac{V_{BN}}{kT} + (k_\Gamma + \eta + 1)} \left( \frac{i_{op}}{i_{0n}} \right) \frac{1}{\eta + 1}$$

(4)

$$A = \frac{V_{BN}}{k_\Gamma} + V_{DD}(1 + k_\Gamma - \eta^2) - V_{in0}(1 + \eta) - V_{tp0}(1 + k_\Gamma + \eta) + n_vT \ln \left( \frac{i_{op}}{i_{0n}} \right)$$

(5)

During a falling input transition, $M_{PX}$ enters weak inversion, but $M_{HN}$ remains in super-cutoff. $V_s$ and $OUT$ are equalize, pulling both $V_s$ and $V_{GS}$ of $M_{HN}$ towards 0V. Leakage through the $M_{PN}$ naturally occurs in the output node, producing positive feedback by increasing its own $V_{GS}$. Eventually, $V_s$ and $OUT$ have charged to $V_{DD}$, leaving $V_{GS}$ and $V_{DS}$ of the $M_{HN}$ at 0V. The on-current can be approximated to the subthreshold current of $M_{HN}$ when $V_{DS} \approx V_{DD}$ and $V_{GS} \approx 0$

$$I_{ON,M_{HN}} = i_{0n} e^{\frac{V_{BN} - V_{DD} - V_{tn}}{kT}}$$

(6)

$$B = \frac{V_{DD}(\eta + 1) - \Delta V_{t0} - 2V_{BN}(1 + \eta) - n_vT \ln \left( \frac{i_{op}}{i_{0n}} \right)}{k_\Gamma + 2\eta + 2}$$

(7)

Increasing $V_{BN}$ lowers the $V_s$ of $M_{HN}$ which affects the stack effect by increasing $V_s$. While this further reduces the $V_{GS}$ of $M_{HN}$ causing increased leakage due to GIDL, it also decreases $V_{DS}$ which reduces leakage due to DIBL resulting in only a small net increase in leakage current (Fig. 2). $I_{ON}$ experiences a greater increase since GIDL is not a factor due to $V_{GS}$ being fixed at 0V. Note that these effects can be heavily influenced by technology, so $I_{OFF}$ and its sensitivity to forward body biasing may vary in SOI or FinFET devices.

III. MEASUREMENTS AND CONCLUSION

The body-biased DLS logic gates were designed using a standard cell design approach that uses tap-cells to independently bias $V_{BN}, V_{FP}, NW$, and the substrate. A test chip was fabricated in 65nm CMOS (Fig. 3) containing arrays of 1000 leaking inverters and 29-stage ring oscillators for two cases: $\Delta V_{t0} = 0$ (all transistors are the same $V_{t0}$) and $\Delta V_{t0} \approx 0.25V$ ($M_{HN}/M_{FP}$ are lower $V_{t0}$ than $M_{PX}/M_{NX}$). In both cases, $M_{HN}$ and $M_{PX}$ are sized relative to the inner transistors such that $i_{op}/i_{0n} = 5\mu m/120nm$. Forward body bias was applied to $M_{HN}$ and $M_{FP}$, where $V_{BN} = V_{FBB}$ and $V_{FP} = V_{DD} - V_{FBB}$. Fig. 4 shows single inverter leakage and delay across $V_{DD}$ and $V_{FBB}$ for $\Delta V_{t0} = 0$. Both $V_{DD}$ and $V_{FBB}$ are nearly constant across $V_{FBB}$, while delay reduces with $V_{FBB}$ up to 21x for $\Delta V_{t0} \approx 0.25V$ and 41x for $\Delta V_{t0} = 0$. Increasing $V_{DD}$ causes an increase in delay (decrease in on-current, consistent with (6)–(7)). This effect is very small for $\Delta V_{t0} \approx 0.25V$, and more pronounced for $\Delta V_{t0} = 0$. This voltage-delay sensitivity to $\Delta V_{t0}$ is not accounted for in (6)–(7) and is likely due to differences in $\eta$ and $k_\Gamma$ between the different $V_s$ transistors when $\Delta V_{t0} \neq 0$. Increasing $V_{DD}$ also reduces subthreshold current according to (4)–(5), but increases gate leakage ($\propto V_{DD}^{e^{-k/T}}$) until it dominates the total leakage current. This occurs for all $V_{DD}$ for $\Delta V_{t0} \approx 0.25V$ and for $V_{DD} > 0.4V$ for $\Delta V_{t0} = 0$. From these results, forward body bias is recommended to maximize performance of DLS logic at negligible leakage cost.

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REFERENCES


