Design Optimization of Register File Throughput and Energy using a Virtual Prototyping (ViPro) Tool

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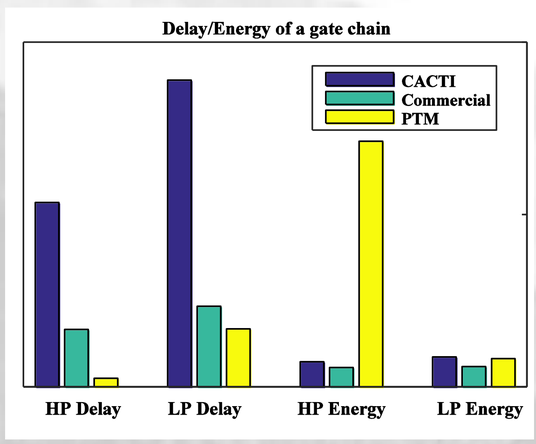
Introduction

- Register File (RF)
  - A register file is one of the widely used memories in processors that is usually implemented with a multiple port SRAM. RFs take up a significant fraction of the power budget of processors, and they are also the critical path that constraints the clock cycle in processors.
  - More than 30 unique custom RFs can be employed in a single CPU or SoC, a delicate RF design for low power and high performance is necessary, which requires a significant design effort.
- Virtual Prototyping Tool (ViPro)
  - The previous version of ViPro only supports 6T SRAM design, and it basically runs brute force simulation by enumerating design knobs like the number of rows, columns, and banks.
  - This work provides a good opportunity to assist RF design optimization by modifying ViPro to rapidly evaluate different RF prototypes with built-in sub-circuits. The outputs of ViPro are delay and energy of all of the evaluated prototypes which can inform the designer of the structures that satisfy the requirements.

Motivation and Background

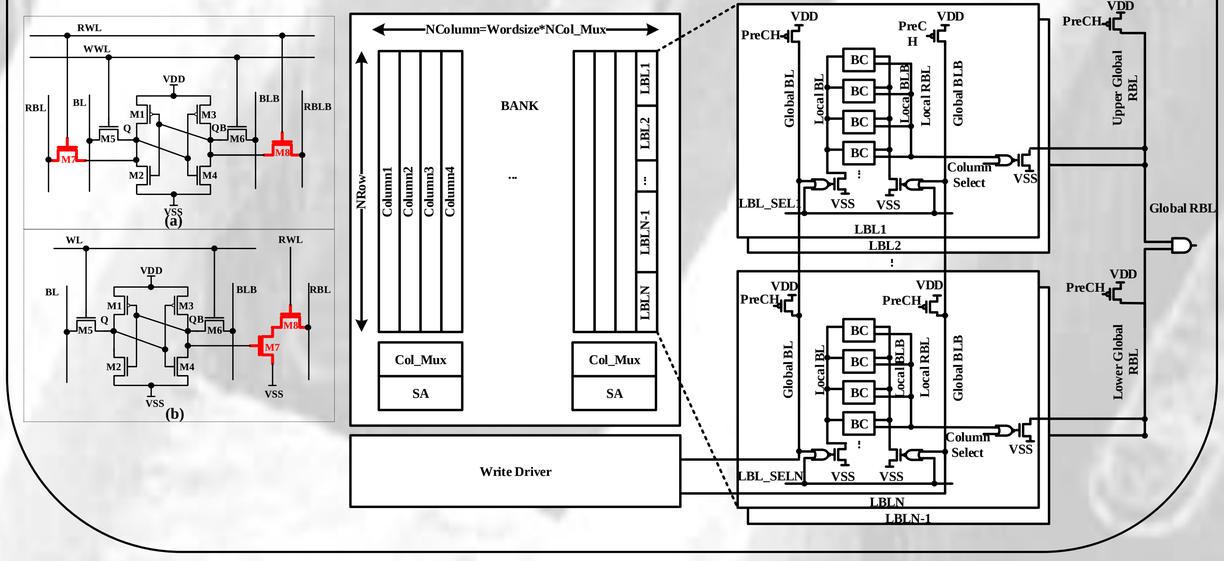
- Limitation of CACTI
  - Similar tool likes CACTI developed by HP Laboratories also evaluates delay and energy of memories, but the results are extremely inaccurate due to using a mathematical circuit model.



- Motivation of developing ViPro for Register Files
  - The above figure illustrates the delay and energy of a gate chain which is a fundamental element of circuits, and results of CACTI using high performance and low power transistors are both substantially different from SPICE simulation results of the commercial technology and the predictive technology model for the same gate chain. Fortunately, ViPro can overcome this issue by easily adapting to any selected technology.

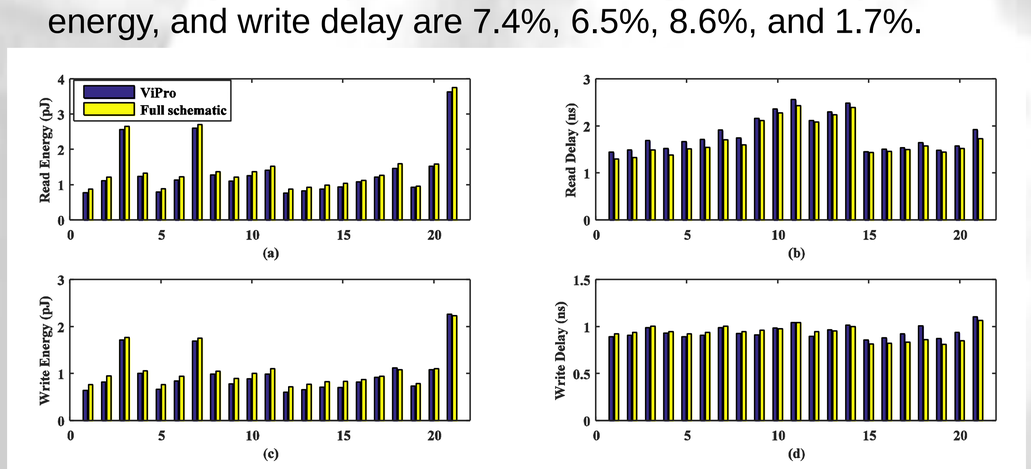
Major Contributions

- Multi-port Bitcell Layouts
  - Two types of BL sensing scheme: Differential BL and single-ended BL sensing scheme.
  - Sizes of the RF bitcell are critical in calculating parasitic capacitance and resistance, compact bitcell layouts are designed and extracted to improve the accuracy of ViPro.
- Hierarchical BL Sensing Scheme
  - Hierarchical BL sensing with local BLs can potentially achieve lower energy consumption by reducing active BL capacitance.



Verification for ViPro

- Four metrics are chosen as the standard for comparison between ViPro fully built RF schematic
  - The average discrepancies of read energy, read delay, write energy, and write delay are 7.4%, 6.5%, 8.6%, and 1.7%.

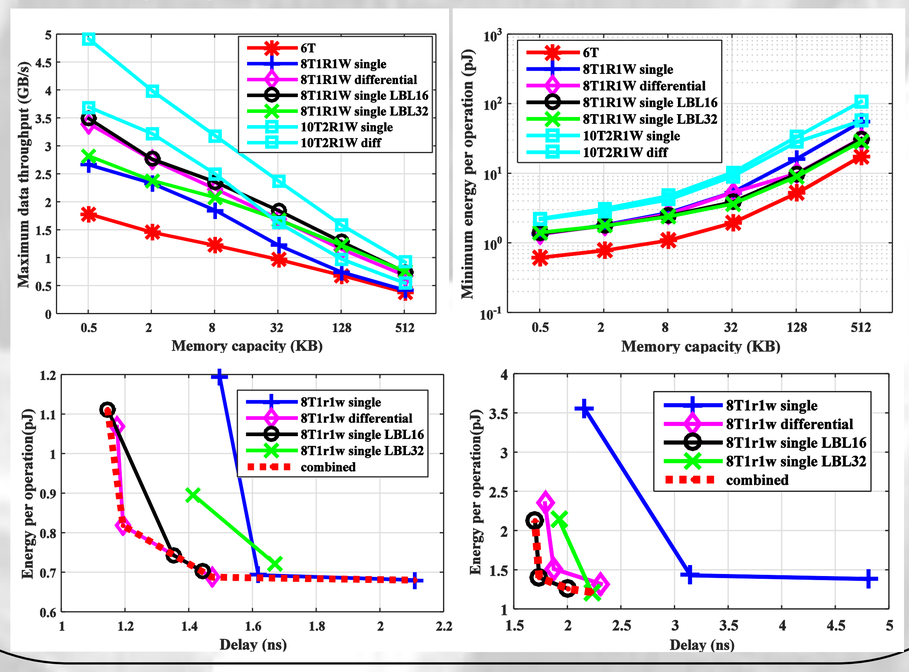


Algorithm

- ViPro enables early design space exploration by creating virtual prototypes of complete RF macros with built-in simulation templates. It then combines these templates with process-related data to generate netlist that can be simulated using Spectre. ViPro also manages a hierarchical model of the memory to calculate the prototype's global metrics, such as energy and delay. Since ViPro allows the components of memory to be redefined using varying levels of detail, designers can quickly evaluate and re-optimize a complete prototype in an early design cycle.

Results

- Improvements in the Maximum Data Throughput
  - Data throughput of 10T 2R/1W ports bitcell with differential BL is 2.75 times than 6T bitcell at 0.5KB, and 2.33 times at 512KB.
- Improvements in the Minimum Energy Consumption
  - At 0.5KB, the lowest energy per operation of 8T 1R/1W bitcell is realized by single-ended BL sensing scheme, which is 7.5% lower than differential BL sensing scheme.
- Improvements in the Minimum Energy Consumption
  - A combined Pareto curve with either lower energy consumption or lower delay is plotted as the dotted line.



Conclusions

- The expanded version of ViPro for RF not only fills the blank of optimizing multi-port RF optimization, it also employs an additional hierarchical BL sensing technique which brings significant performance improvement and energy reduction to meet required specifications.

Future Work

- Following the same method of this work, templates for cache memory have been included by adding a tag array and a comparator circuit, which enhances ViPro to be capable of optimizing the most commonly used SRAM-based scratchpad memory and cache.