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# A 1.3µW, 5pJ/cycle sub-threshold MSP430 processor in 90nm xLP FDSOI for energy-efficient IoT applications

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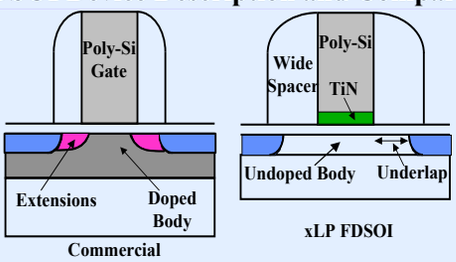
## 1. Introduction

This poster presents an implementation of a 16-bit MSP430 processor for ultra-low-power (ULP) systems catering to battery-less wireless sensor nodes, biomedical, and other IoT applications. Implemented in a custom extremely low power (xLP) 90nm FDSOI process, the processor

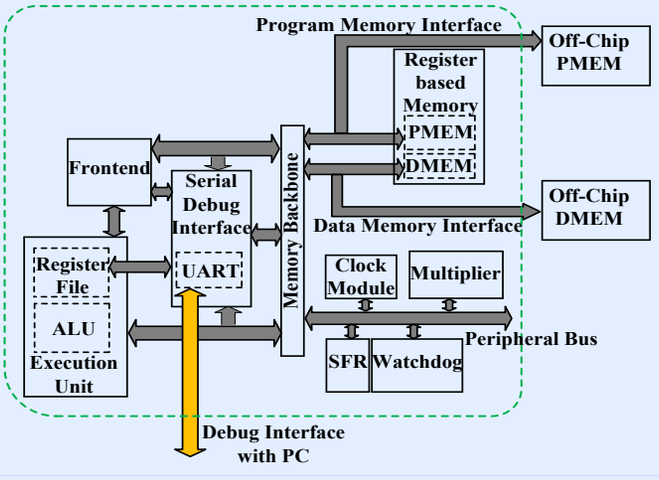
- Consumes 1.3µW operating at 0.4V while executing a QRS peak detection algorithm at 250 kHz.
- Supports the standard MSP430 instruction set architecture (ISA)
- The measured energy while operating at 250 kHz was 5pJ per cycle at 0.4V.
- The fabricated xLP devices show 55% reduction in threshold voltage ($V_T$) variation compared to similar-sized transistors in a traditional FDSOI process.

## 2. xLP FDSOI Device Description and Comparison

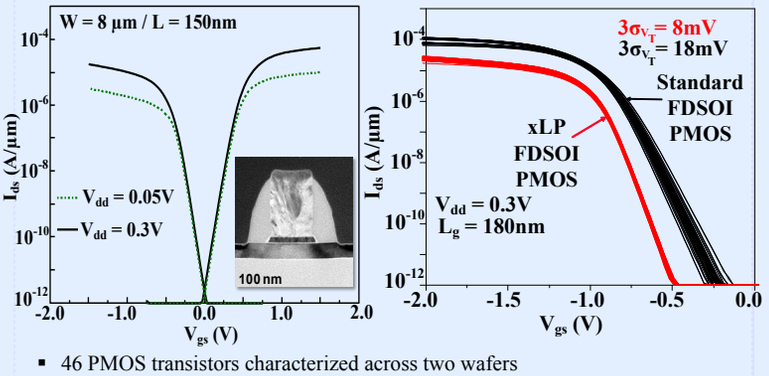



- xLP transistors are fabricated using 30-nm Si on 145-nm BOX
- The SiON gate dielectric thickness is 3.5nm, 5 metal layers of aluminum interconnect and $SiO_2$ dielectric
- Device engineering includes a 1020 °C, 5s rapid thermal anneal, ~10 nm of $CoSi_2$, and a 20-min 400 °C hydrogen passivation anneal
- Eliminating channel doping reduces $V_T$ variation caused by non-uniformity in SOI thickness and RDF
- $V_T$ is set by a work function-tuned TiN metal gate
- Device capacitances are minimized by 76% by eliminating source-drain extensions and employing wide nitride

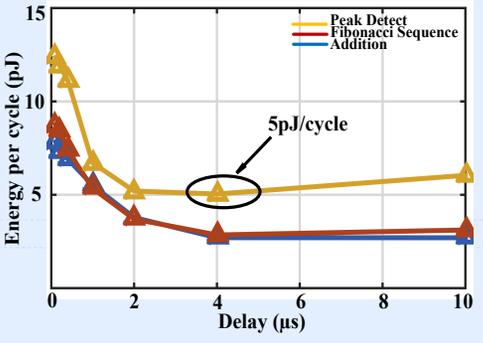
## 3. MSP430 Processor Architecture




## 4. Measured Results




- 46 PMOS transistors characterized across two wafers
- 3σ variation in $V_T$ was found to be 8mV




- Min energy of 5pJ per cycle at 0.4V and 250 kHz running peak detection
- For higher performance, the processor can operate at 1MHz at 0.6V, consuming 6.7pJ per cycle
- By sacrificing 34% energy, 4x performance improvement can be achieved
- Measured minimum energy across 8 functional dies show a σ/µ of 0.0405

## 5. Comparison with prior work

| | [1] | [2] | [4] | [11] | [12] | This Work |
|---|---|---|---|---|---|---|
| Technology | 65nm | 180nm | 180nm | 65nm | 130nm | **90nm FDSOI** |
| Architecture | 16-bit MSP430 compatible | ARM Cortex M0+ | ARM Cortex M0 | 16-bit MSP430 compatible | 16-bit MSP430 compatible | **16-bit MSP430 compatible** |
| Operating Voltage | 0.3-0.6V | 0.16-1.15V | 0.6V | 0.32-0.48V | 0.55V-1.2V | **0.38-0.9V** |
| Min Energy | 6-10pJ/cycle @ 0.5V | 44.7pJ/inst@0.55V | 17.2pJ/inst@0.26V | 2.6pJ/cycle@0.375V executing FIR filtering | 14.8pJ/cycle@0.6V | **5pJ/cycle@0.4V executing peak detection** |
| Operating Frequency | 8.7kHz-1MHz | 2Hz-15Hz | 160-330kHz | 25-71MHz | - | **100kHz-10MHz** |
| Area | 1.62mm2 | 2.04mm2(CPU+MEM) | 1.7mm2(CPU+MEM) | 0.42mm2 | 5.13mm2(CPU+Mem+Accel) | **0.44mm2** |

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