Optimizing SRAM Bitcell Reliability and Energy for IoT Applications

Harsh N. Patel, Farah B. Yahya, Benton Calhoun

University of Virginia

VA - USA

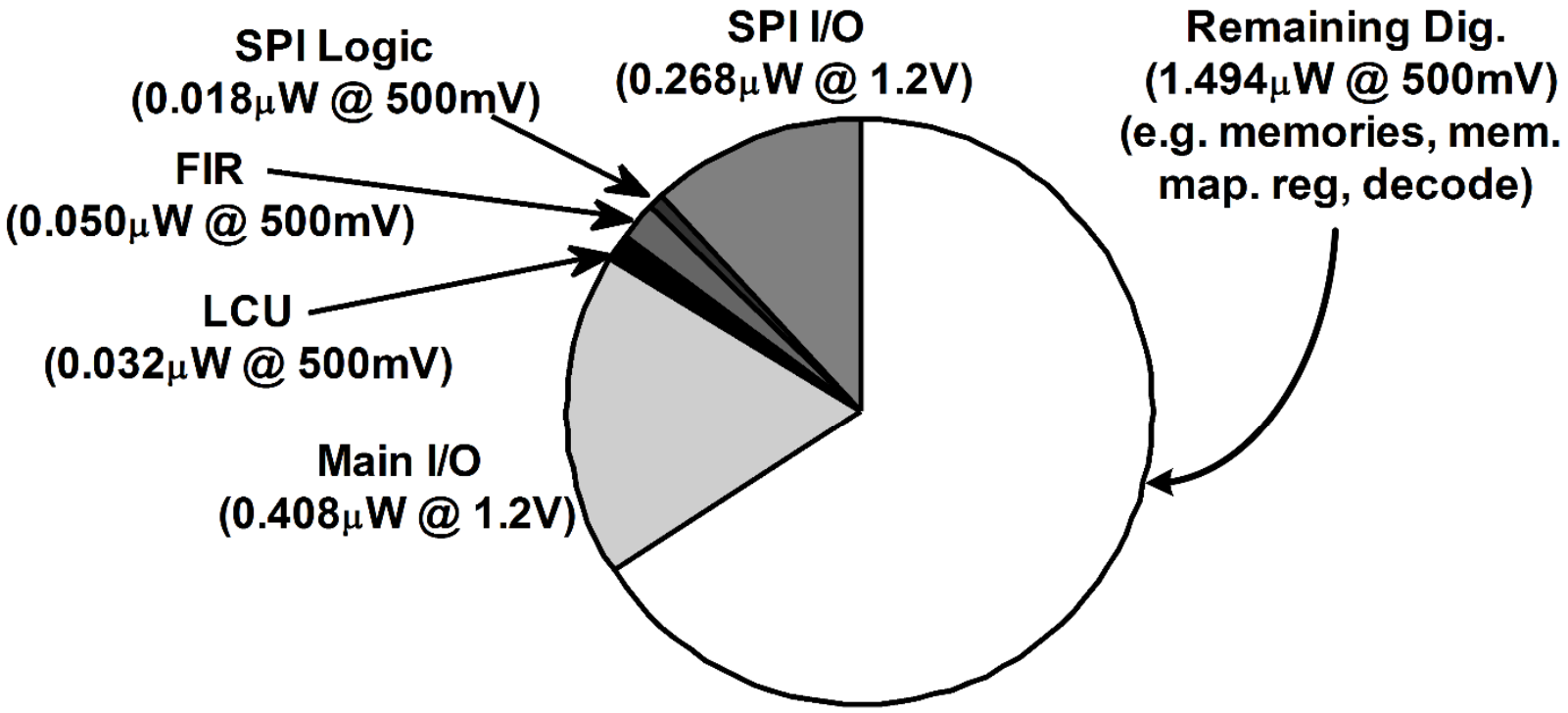
Robust
Low
Power
VLSI

Outline

- Motivation
- Metrics for evaluation
- Metric trade-offs
- Test Chip results
- Conclusion

Motivation

- SRAM dissipates more than 60% of total SoCs power[1]
  - Demands lower operating V_{DD} (CV_{DD}^2)
    - Energy optimal point falls in sub-threshold region

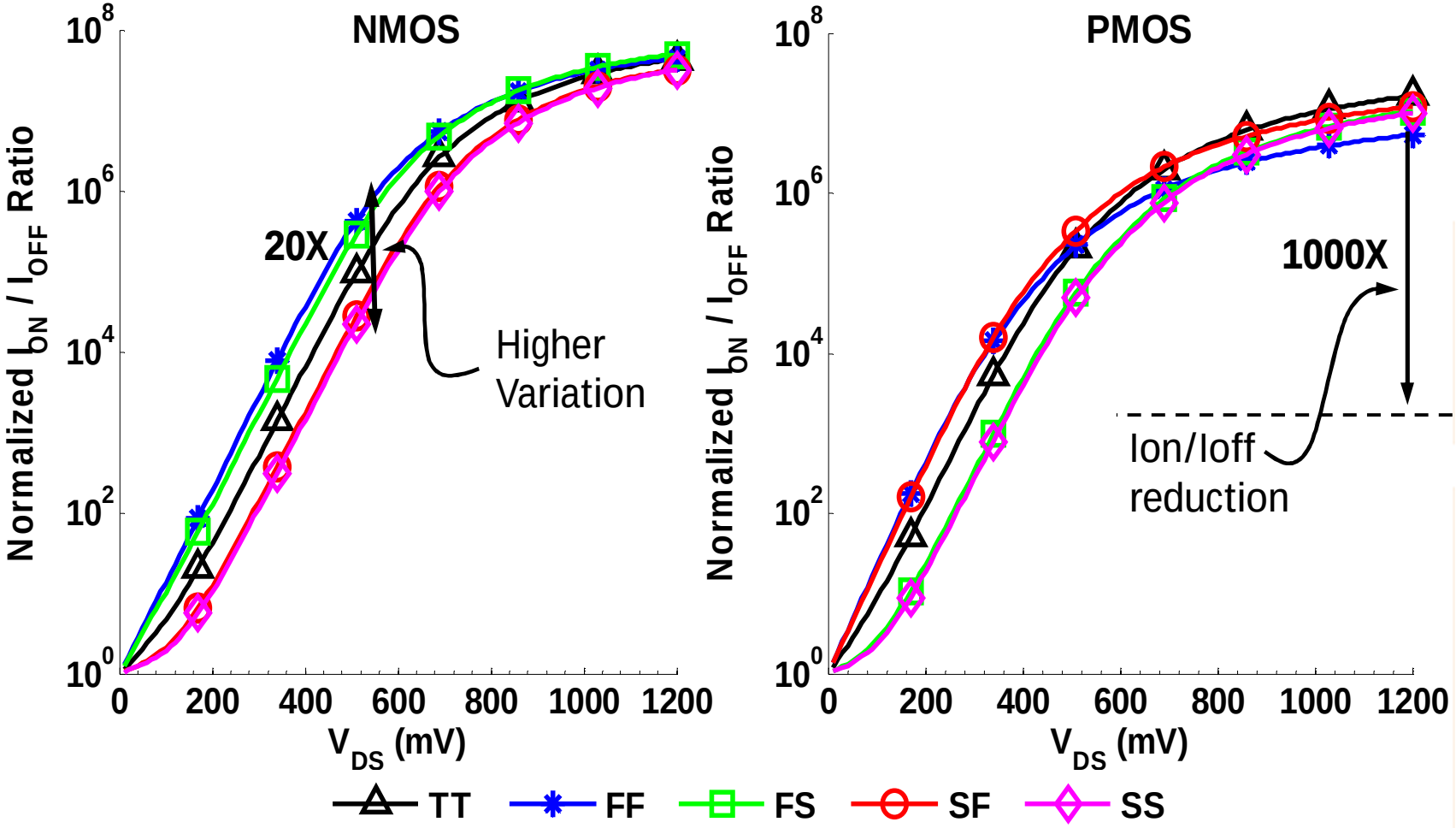


Total Digital Power: 2.27μW @ 200kHz

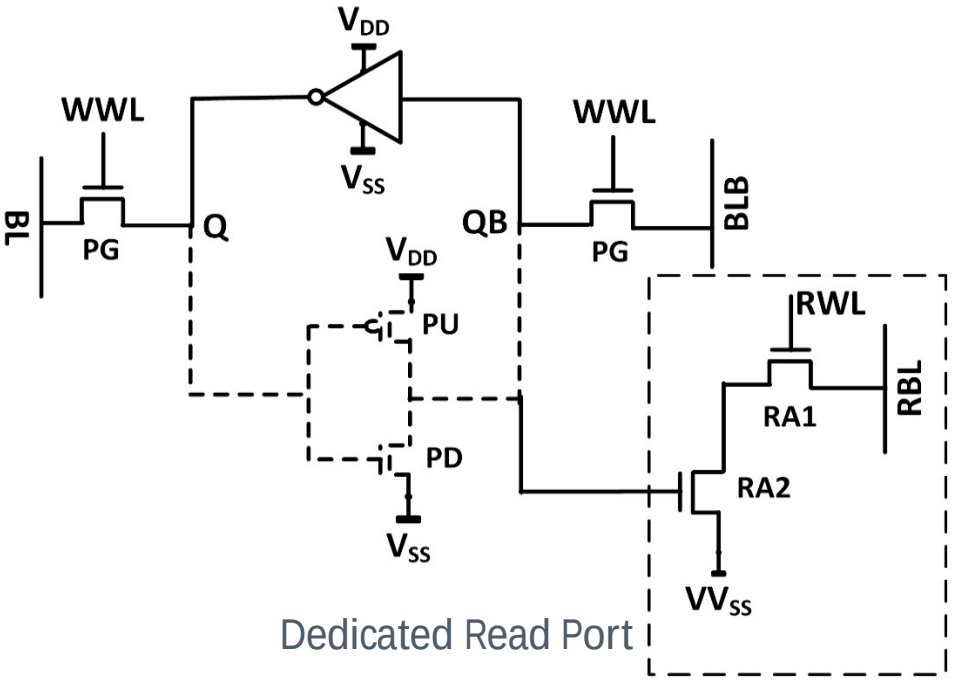
[1] ISSCC 2015

Motivation

- Sub-threshold design challenges:



Motivation



Bitcell	Device Usage			
	PU	PD	PG	RA
HVT	high-V_T	high-V_T	high-V_T	high-V_T
SVT	Standard-V_T	Standard-V_T	Standard-V_T	Standard-V_T
MVT1	high-V_T	high-V_T	Standard-V_T	Standard-V_T
MVT2	Standard-V_T	Standard-V_T	high-V_T	high-V_T
MVT3	high-V_T	high-V_T	high-V_T	Standard-V_T
MVT4	high-V_T	Standard-V_T	Standard-V_T	Standard-V_T

Metric Consideration

- Metrics of interest: Reliability and Energy.

Category	Evaluation Metrics		
Reliability	Date Retention Voltage (DRV)	Hold & Read Static Noise Margins (HSNM / RSNM)	Write Margin (WM)
Dynamic	Leakage Power	Read/Write Energy (Power-Delay product)	

DRV: Minimum VDD below which the storage nodes (Q/QB) flip when the bitcell is un-accessed.

HSNM: Ability of an un-accessed bitcell (WWL/RWL=0, BL=BLB) to reject DC noise.

RSNM: Ability of the half-selected cell to maintain its state during pseudo-read operation (WWL=1, BL=BLB).

WM: Ability of the bitcell to write into the cell (flip the content of storage nodes)

Metric Consideration: Reliability

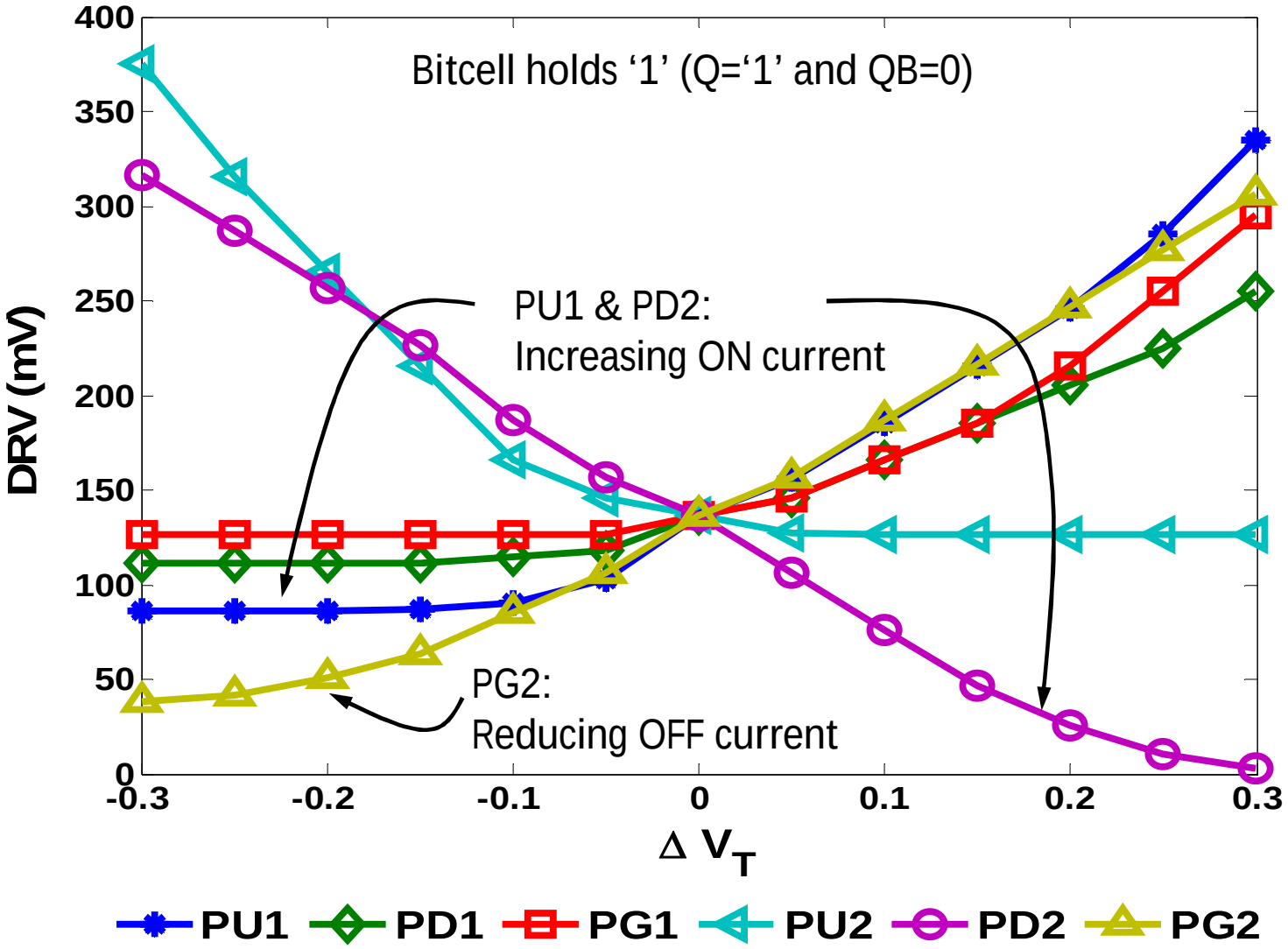
Setup:

Variation Consideration:

- Intra-die: 1000-point Monte Carlo (MC)
- Inter-die: Across corners (FF, FS, TT, SF, SS)
- Temperature: [-50, 125]°C

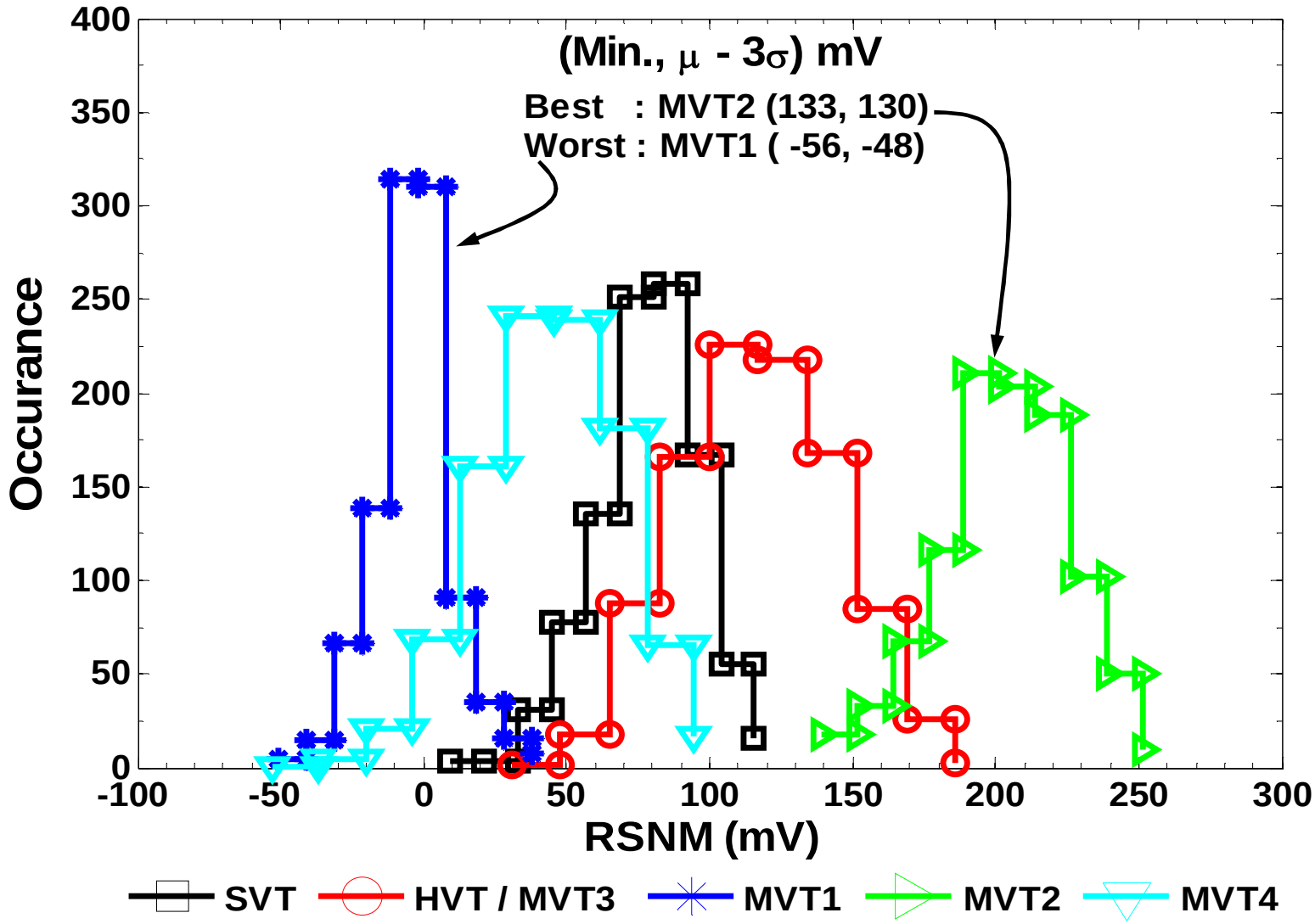
Reliability - Intra-die variation

a) DRV



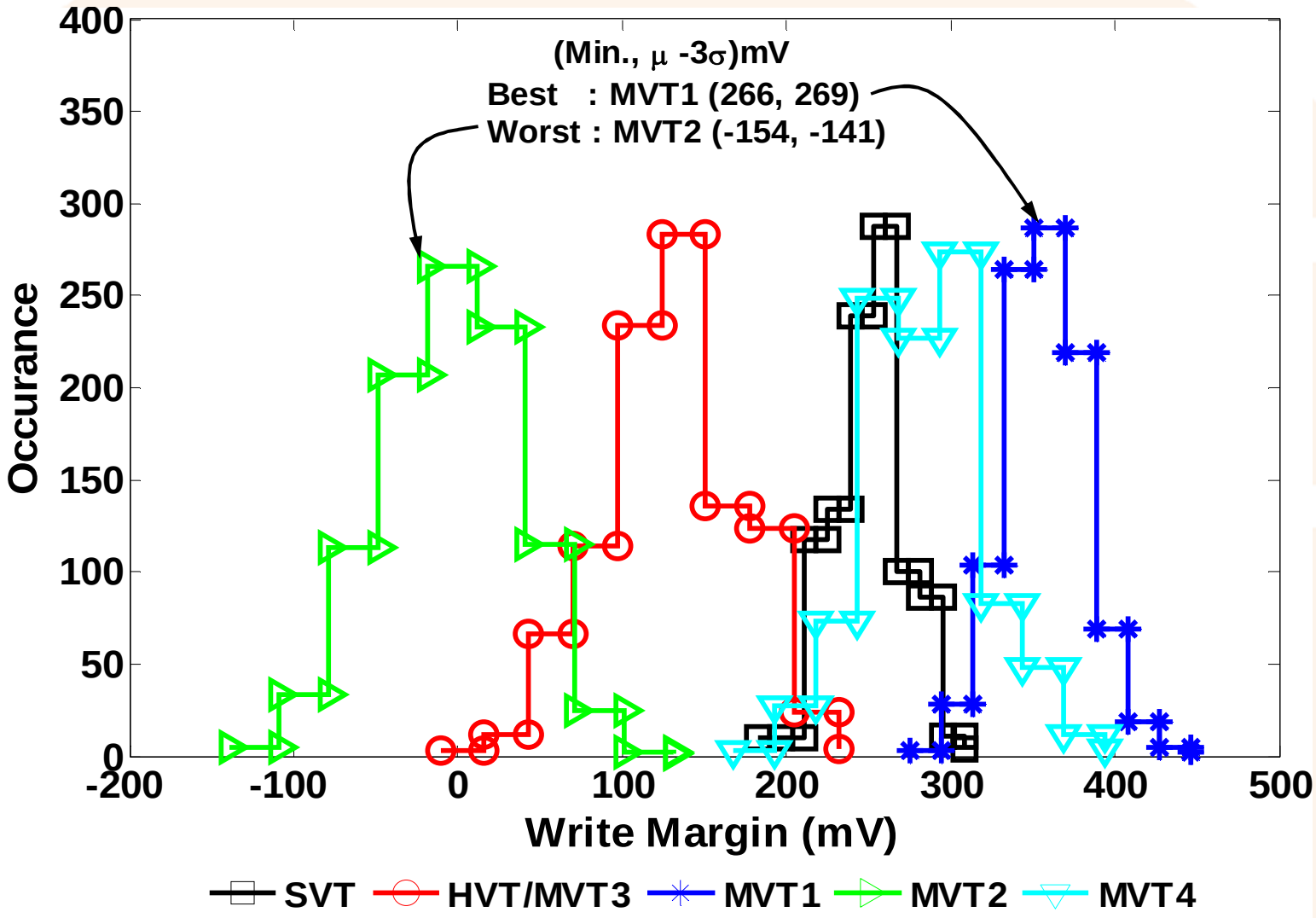
Reliability - Intra-die variation

b) HSNM/RSNM



Reliability - Intra-die variation

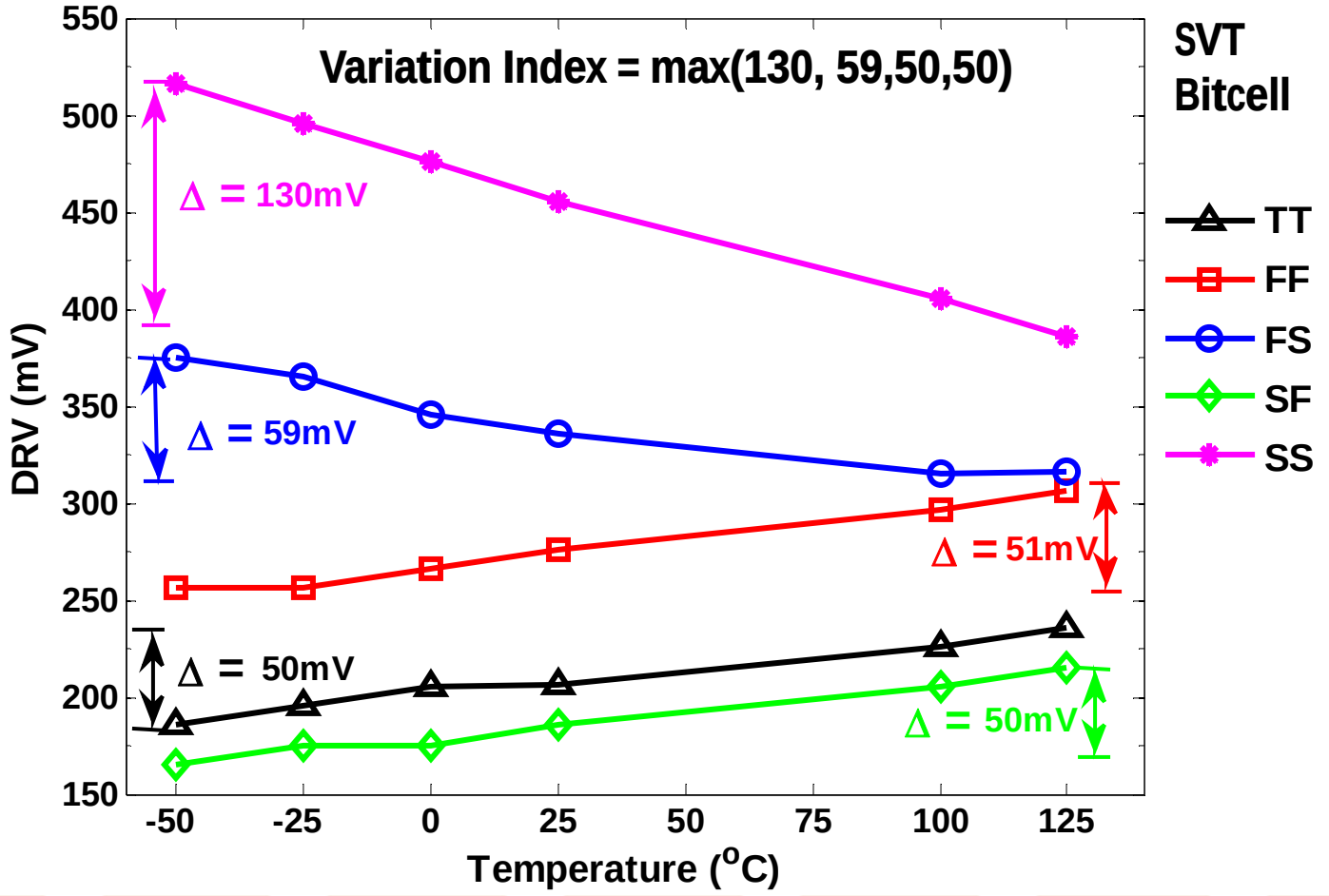
c) WM



Reliability – Inter-die variation

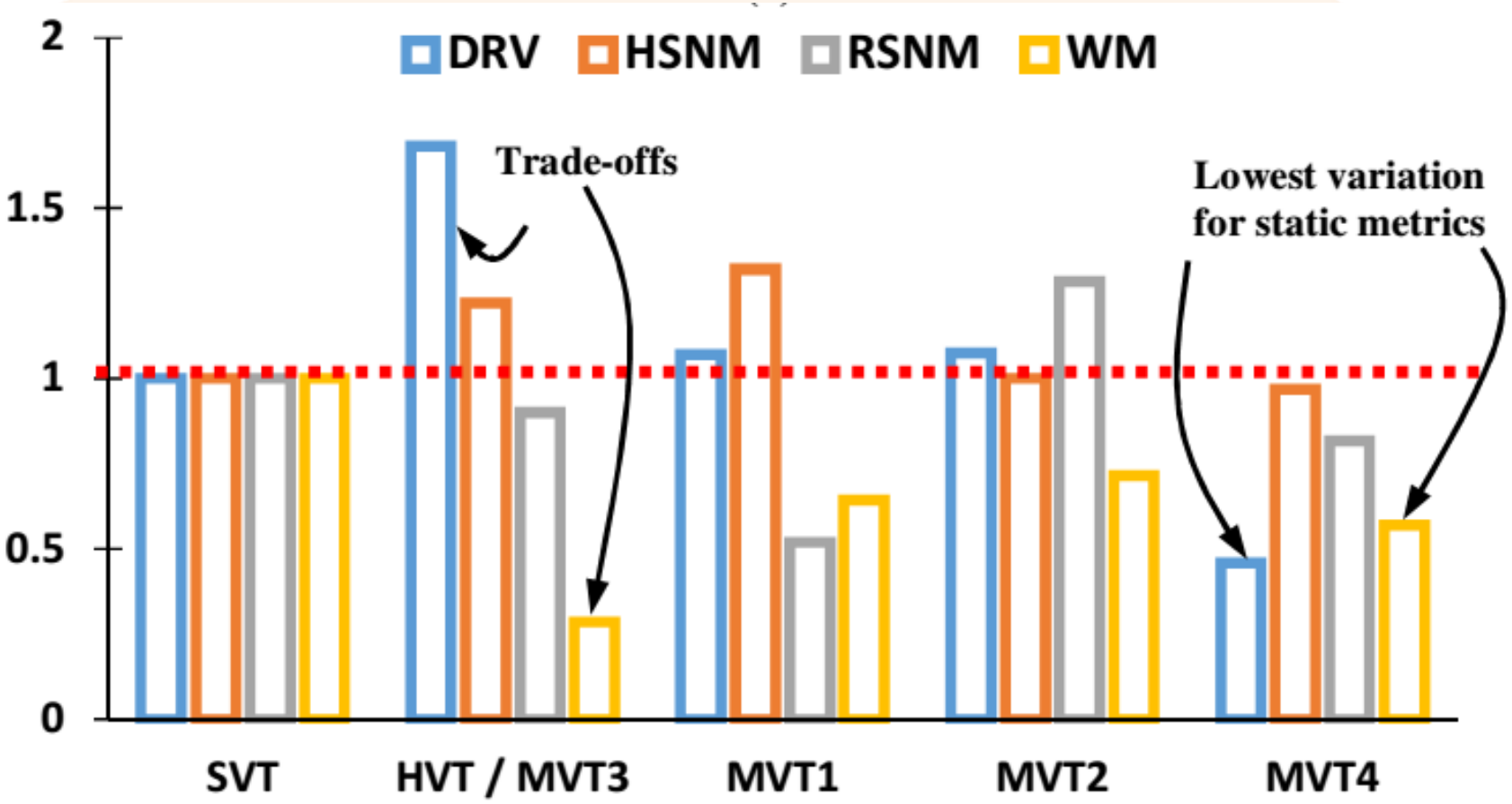
Variation Index (VI):

"The maximum deviation in a metric that a chip, fabricated at any corner, can experience due to temperature variation".



Reliability – Inter-die variation

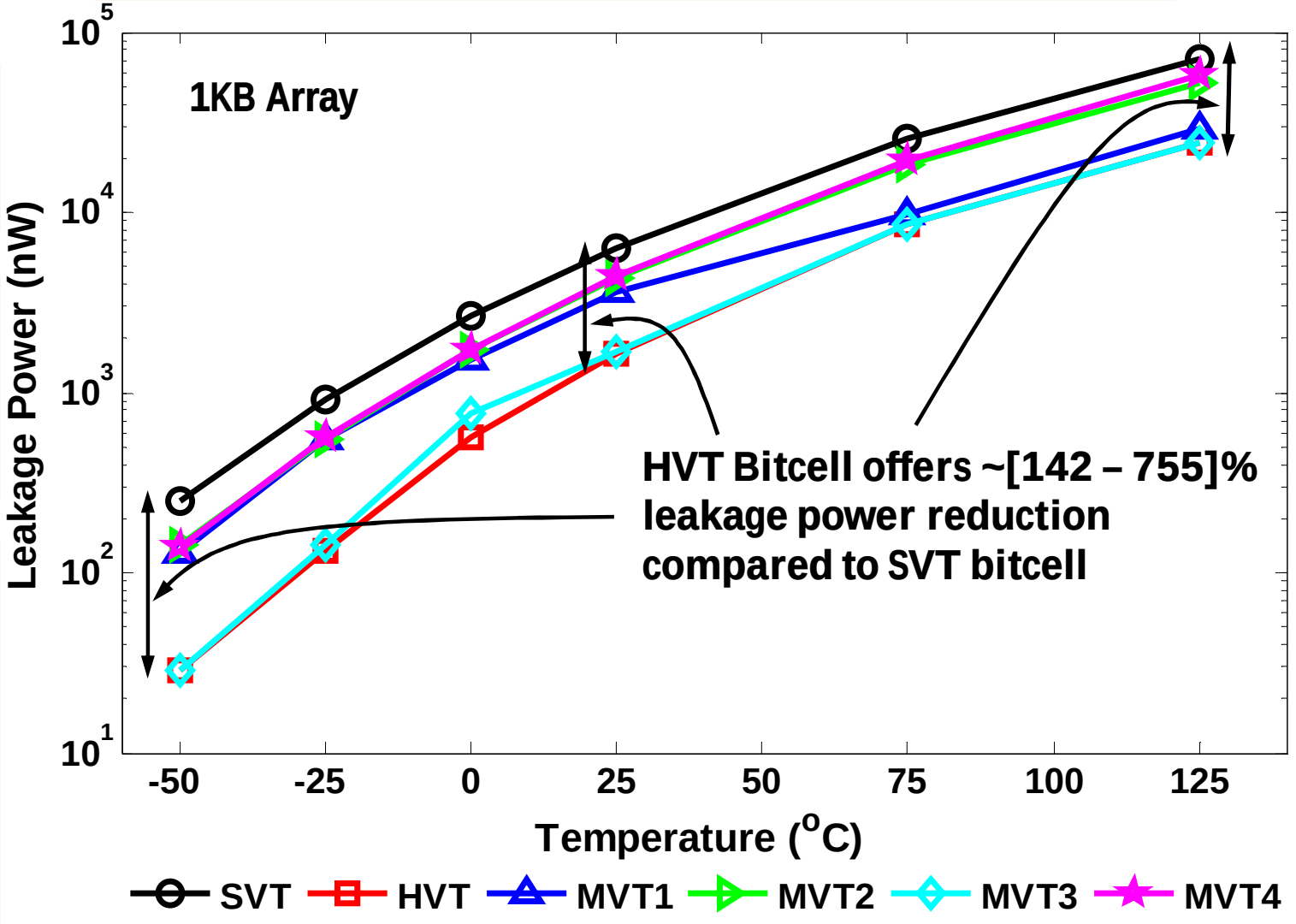
Variation Index (VI)



Comparison of Variation Index (VI) for different metrics across bitcells

Metric Consideration: Dynamic

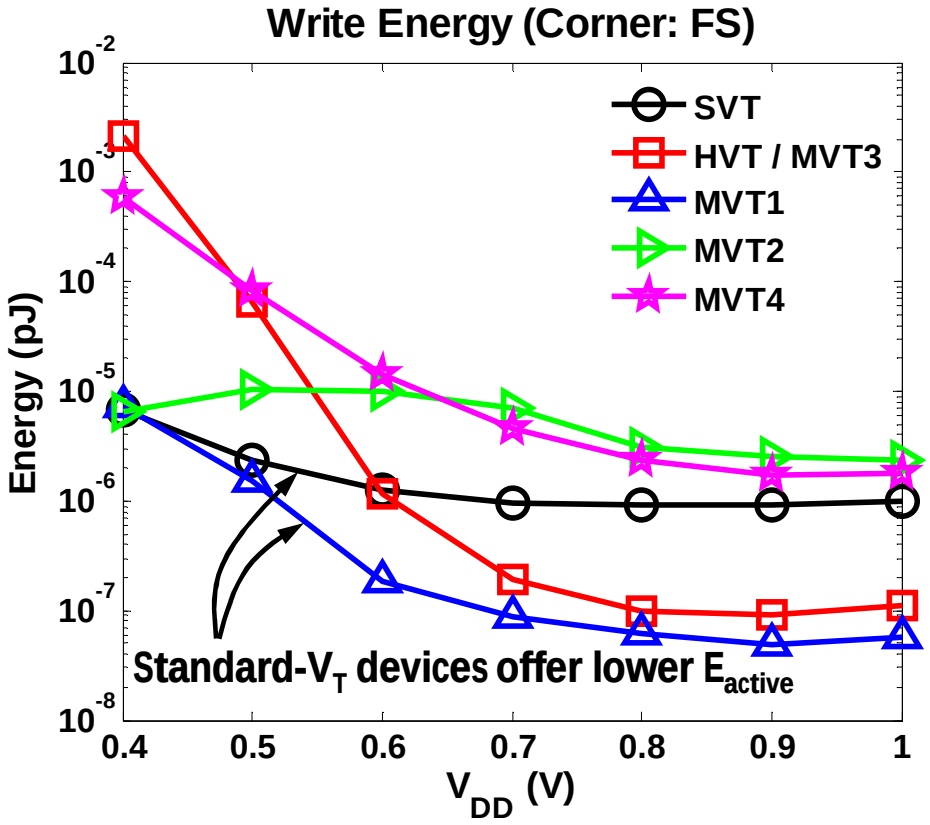
a) Leakage Power

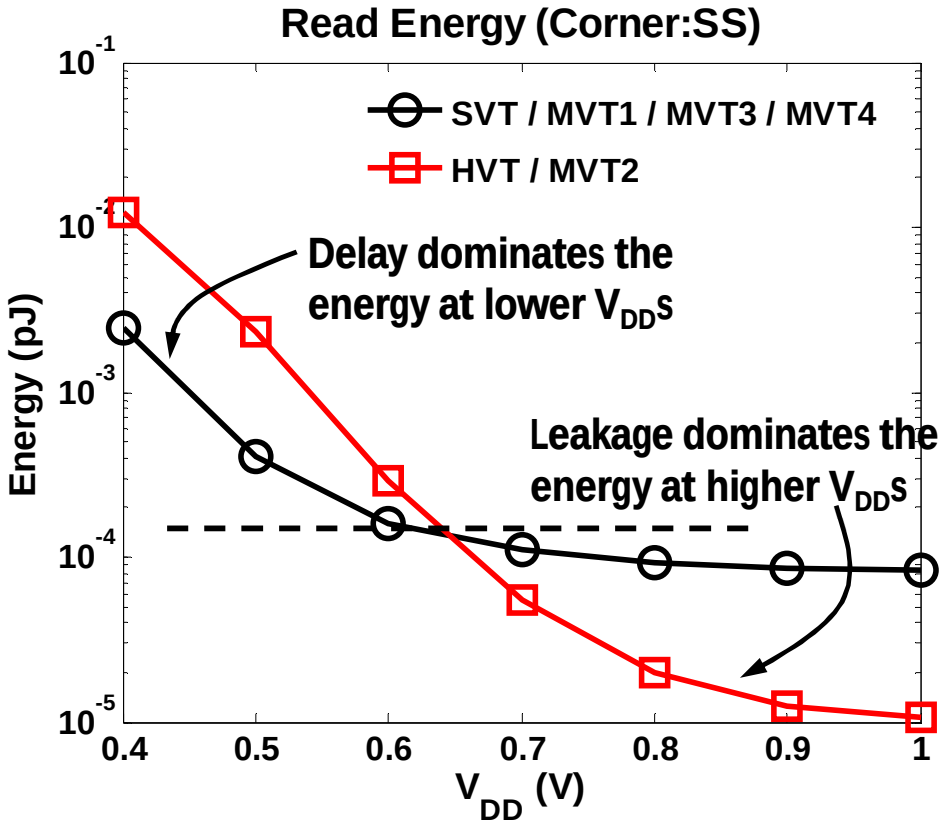


Dynamic

b) Write/Read Energy

Worst corner array Write/Read energy comparison of different bitcells



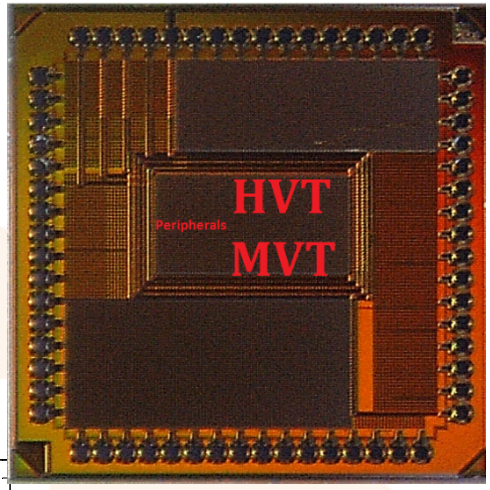


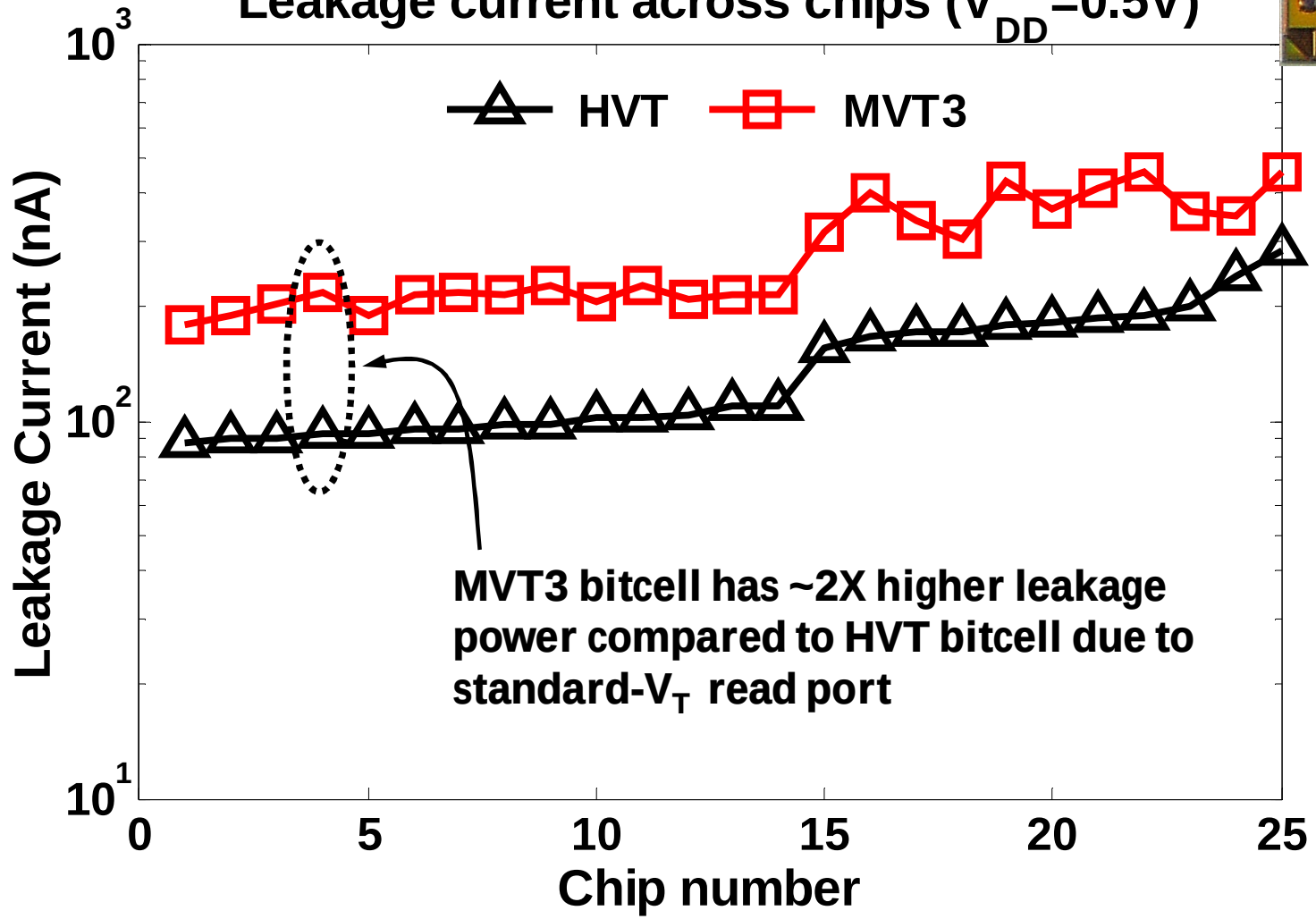
Comparison

Static	Best-to-Worst bitcell choice (left to right)				
DRV	HVT/MVT3	MVT1	SVT	MVT2	MVT4
HSNM	HVT/MVT3	MVT1	MVT2	SVT	MVT4
RSNM	MVT2	HVT/MVT3	SVT	MVT4	MVT1
WM	MVT1	SVT	MVT4	HVT/MVT3	MVT2

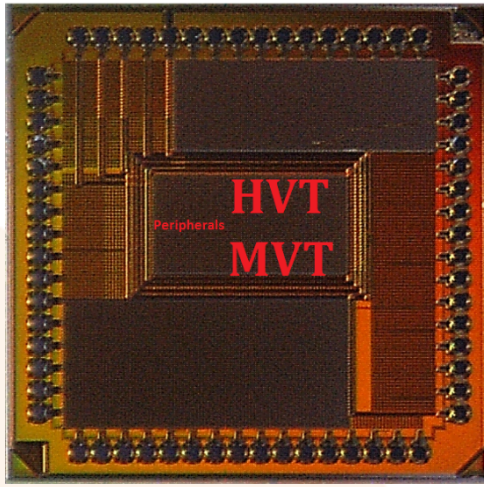
Dynamic					
Leakage	HVT/MVT3	MVT1	MVT2	MVT4	SVT
Write Energy	MVT1	SVT	MVT2	HVT/MVT3	MVT4
Read Energy	SVT / MVT4 / MVT1 / MVT3			MVT2 / HVT	

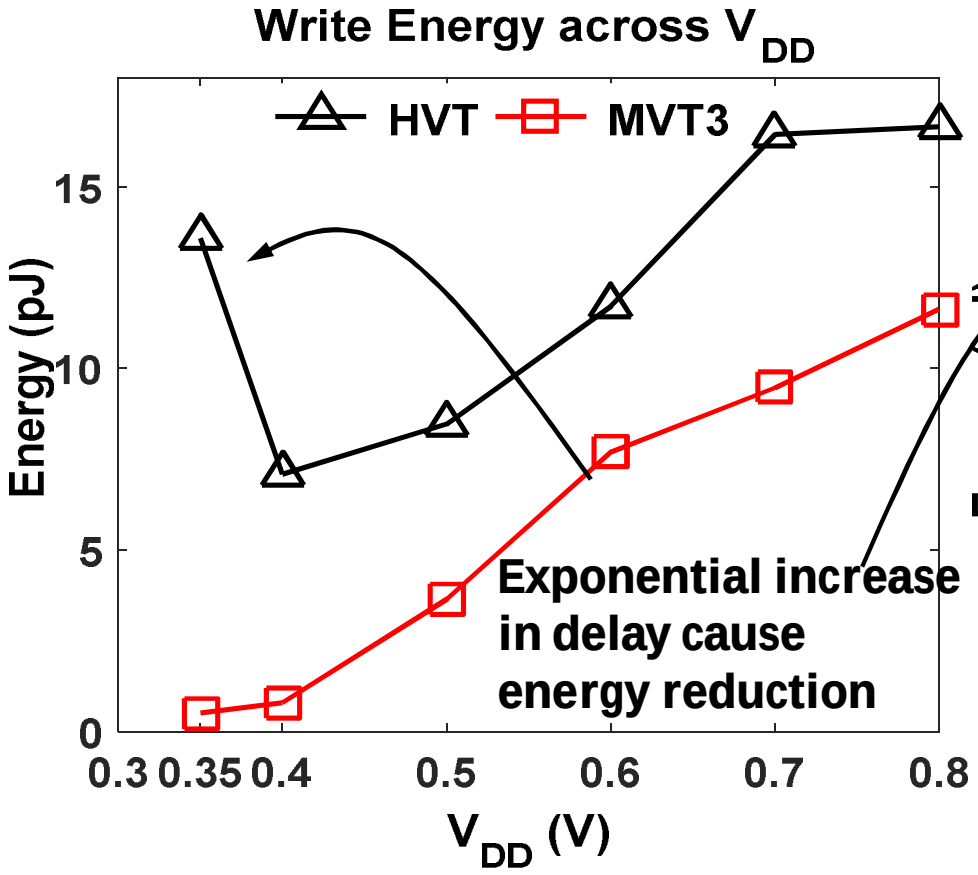
Test chip results

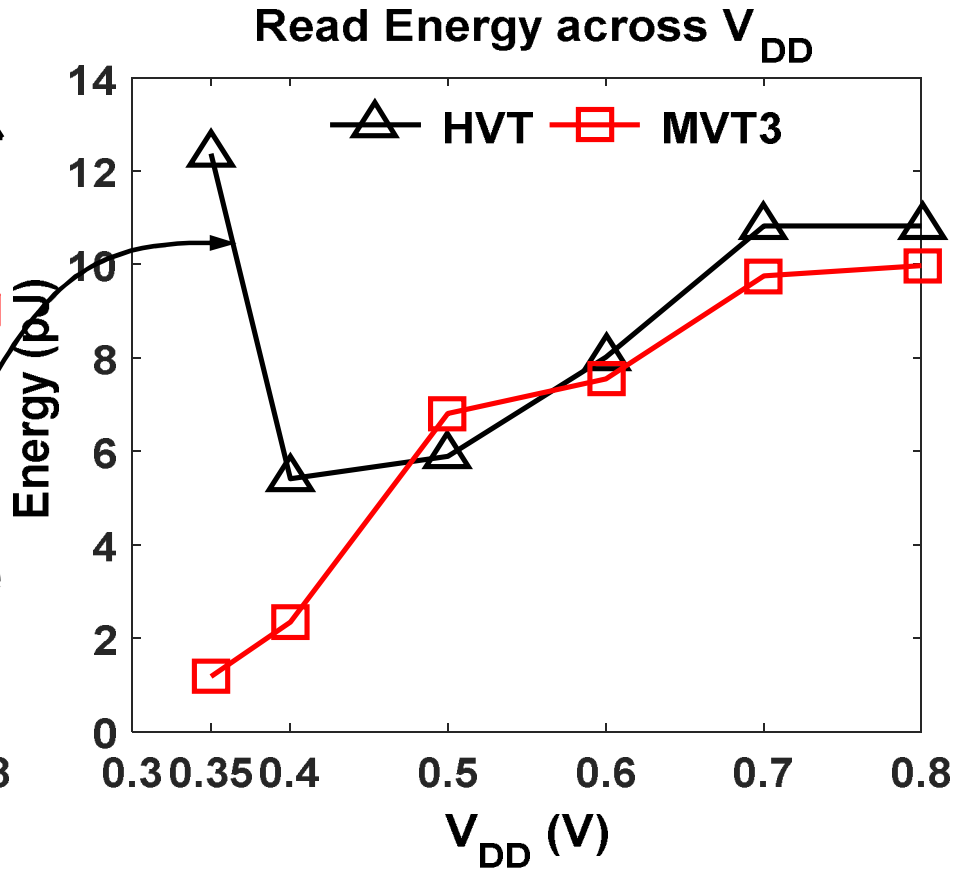




Test chip results



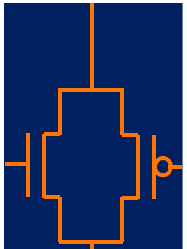




Conclusion

Optimal bitcell selection summary w/ trade-offs and targeted IoT application

Design Metric	Best Bitcell choice	Trade-off(s) metrics	Possible IoT application
DRV	MVT2	WM + Leakage	Applications w/ longer stand by time (e.g. remote sensing)
HSNM	HVT/MVT3	WM + Write speed	Robust design to operate in noisy environments (difficult terrain sensing)
RSNM	MVT2	WM + Leakage	Low V_{DD} write operation (low-power application)
WM	MVT1	RSNM + DRV	
Leakage	HVT	Write/Read Delay + WM	'Mostly Stand-by' application (e.g. body sensing)
Active Energy	MVT1 / MVT3		'Mostly Active' application (e.g. DSP, speech processing)



Thank you!