Exploring Circuit Robustness to Power Supply Variation in Low-Voltage Latch and Register-Based Digital Systems

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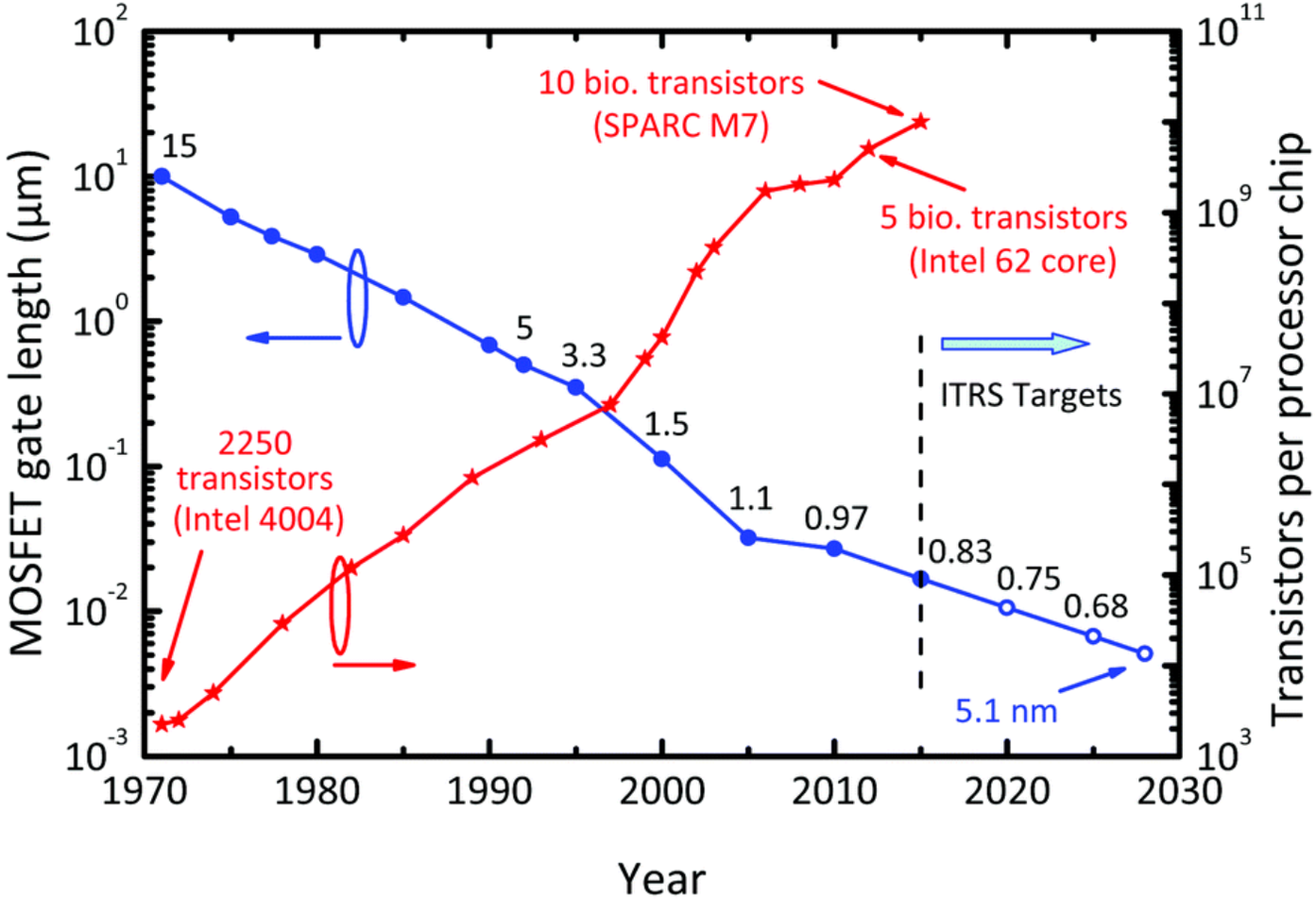
Robust
Low
Power
VLSI

Motivation and Background



Source: The International Technology Roadmap for Semiconductors, http://www.itrs.net.

Shrinking devices + Higher operating speeds → Higher operating currents → **IR drop + L(dI/dt)**

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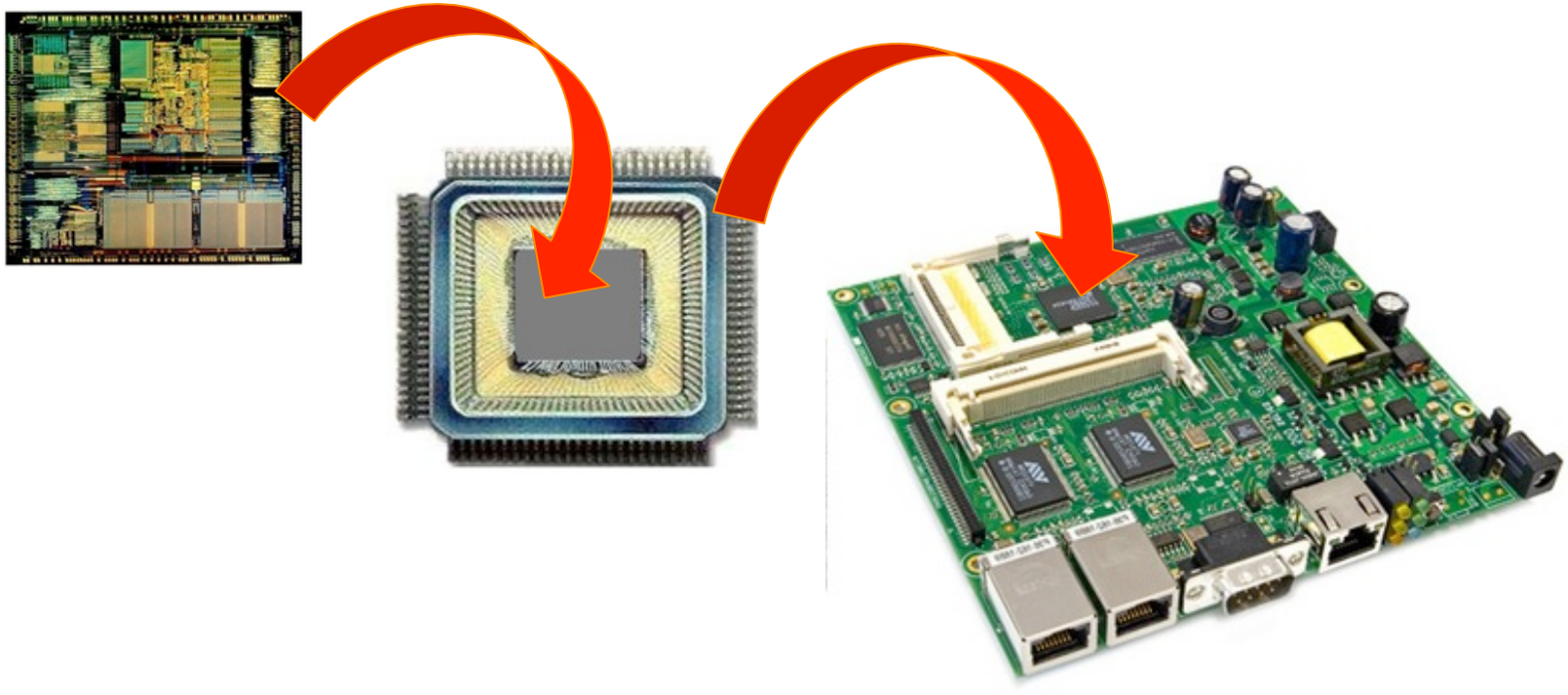

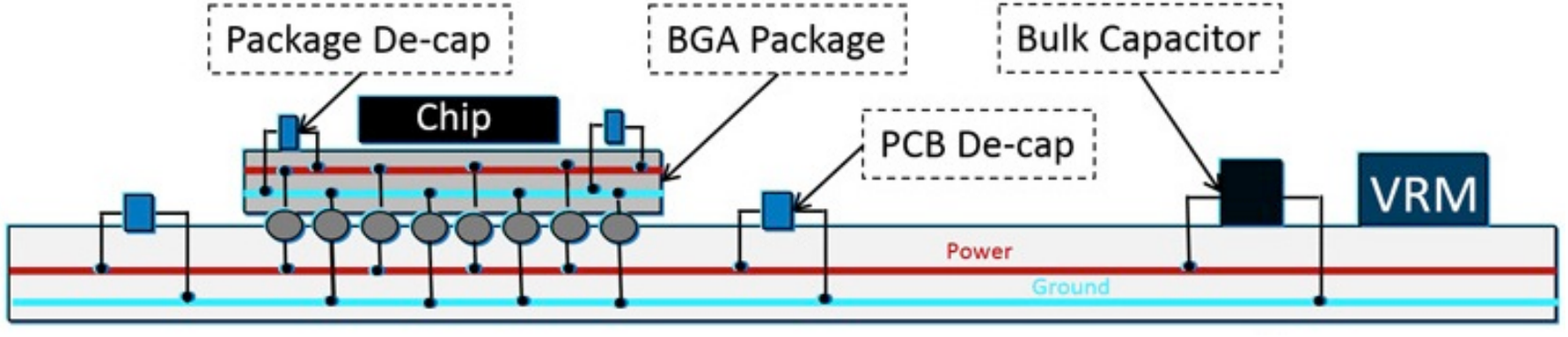

Source: http://www.ansys.com/Products/Electronics/Option-SIwave-PSI-Solver

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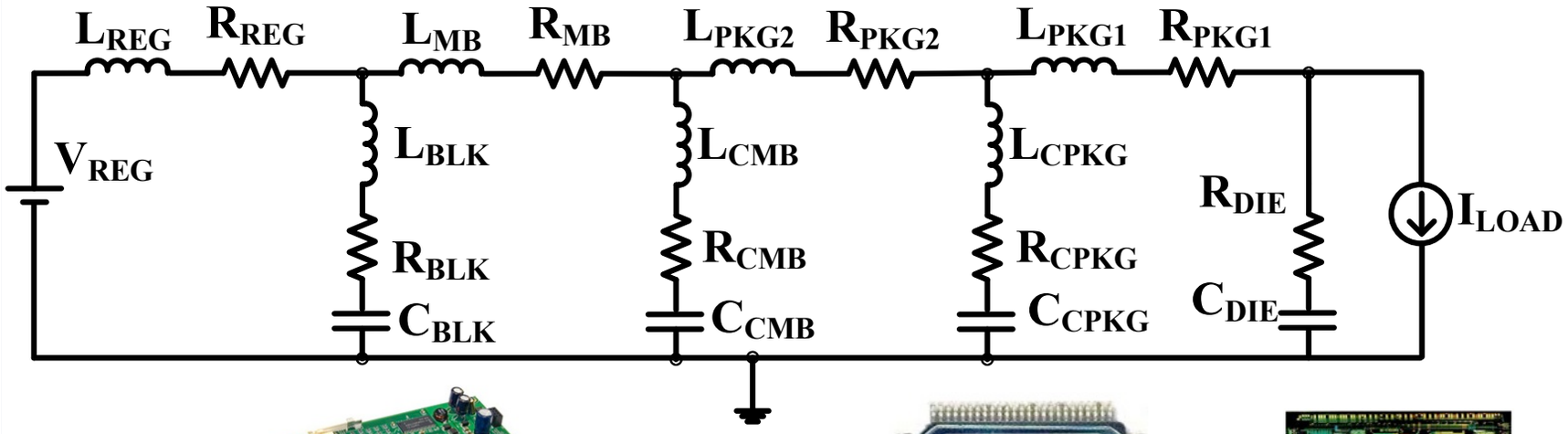
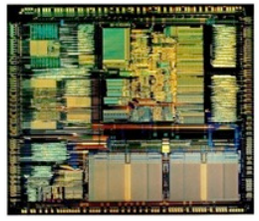
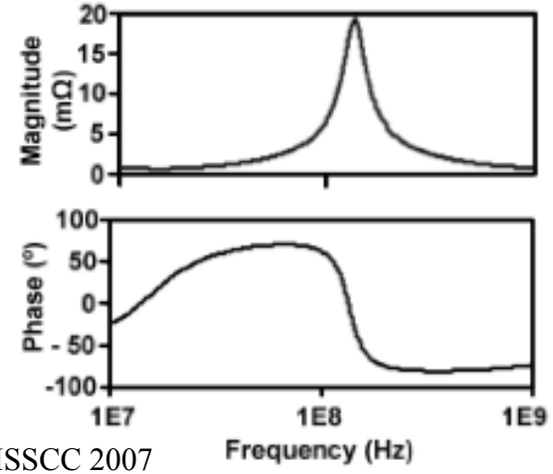




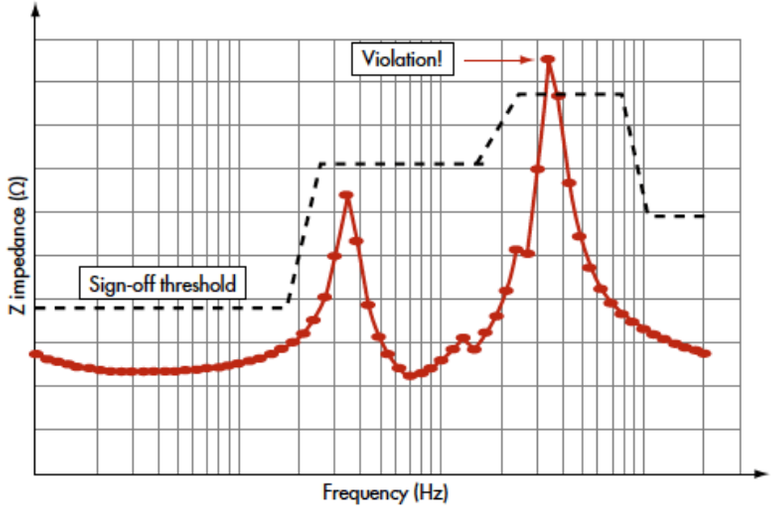
Parasitics (Package, PCB, regulator, chip) → **Power Supply Noise**



Adapted from: J. Xu, P. Hazucha et al. " On-Die Supply-Resonance Suppression…", ISSCC 2007

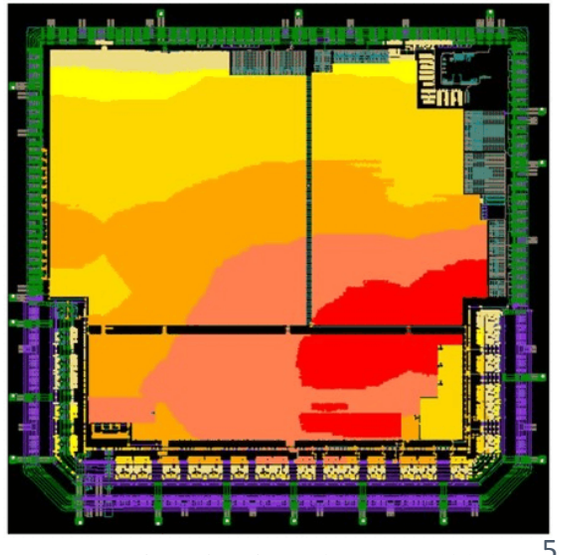
Motivation and Background

- High Frequency: $L\frac{di}{dt}$, package resonance

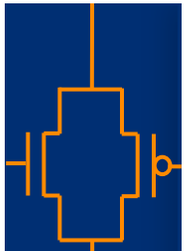


Source: http://electronicdesign.com/boards/understanding-power-integrity-system-wide-challenge

- **Low Frequency: Voltage Regulator, IR drop**



Source: http://www.soccentral.com/results.asp?EntryID=19453



Outline

- Problem Statement
- Overview of prior work
- Proposed solution and hypothesis
  - Evaluation of latch-based pipelines in presence of power supply noise
  - All-digital ULP power supply droop measurement
- Measured Results
- Summary and Conclusion

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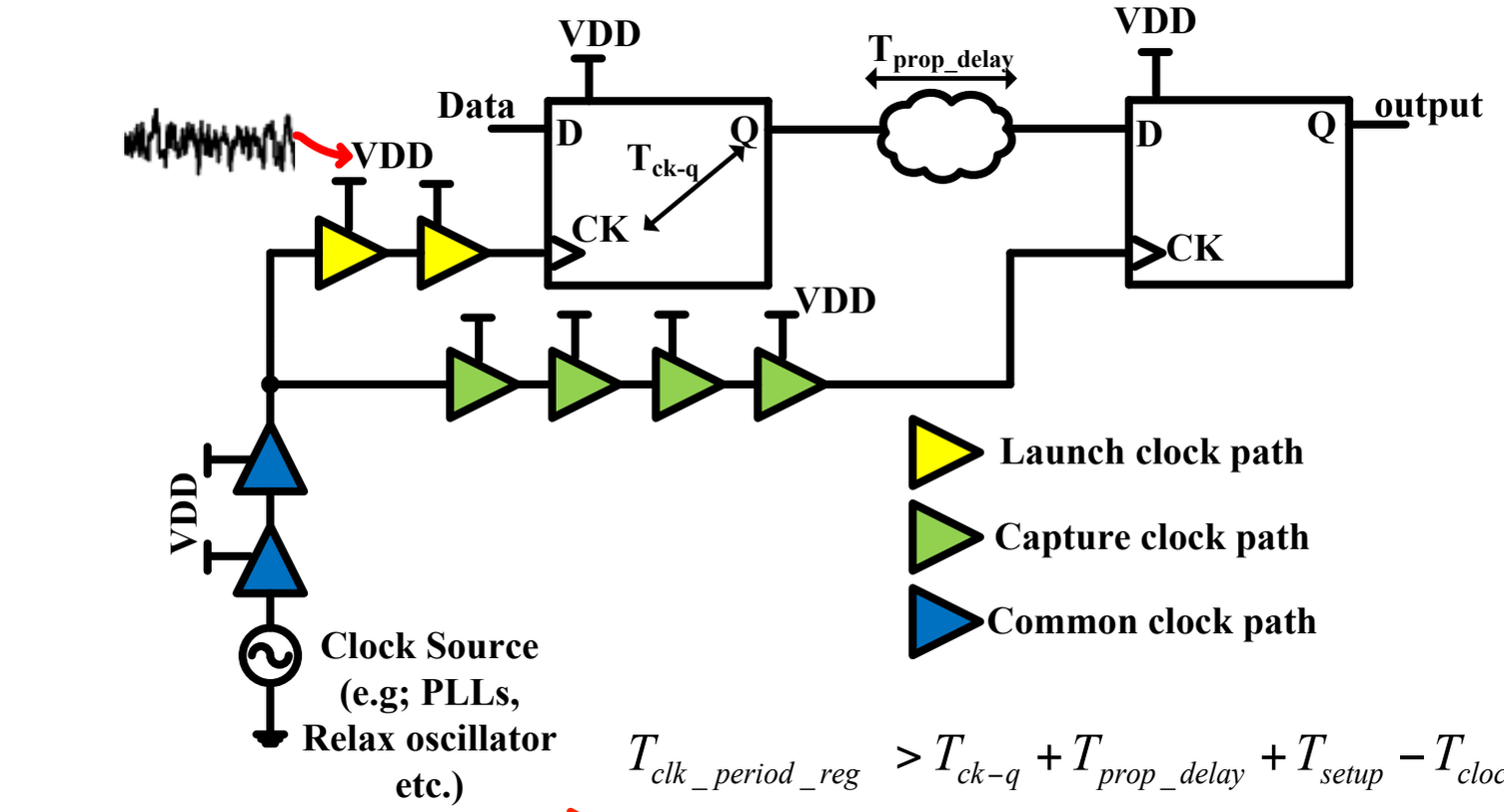
Problem Statement

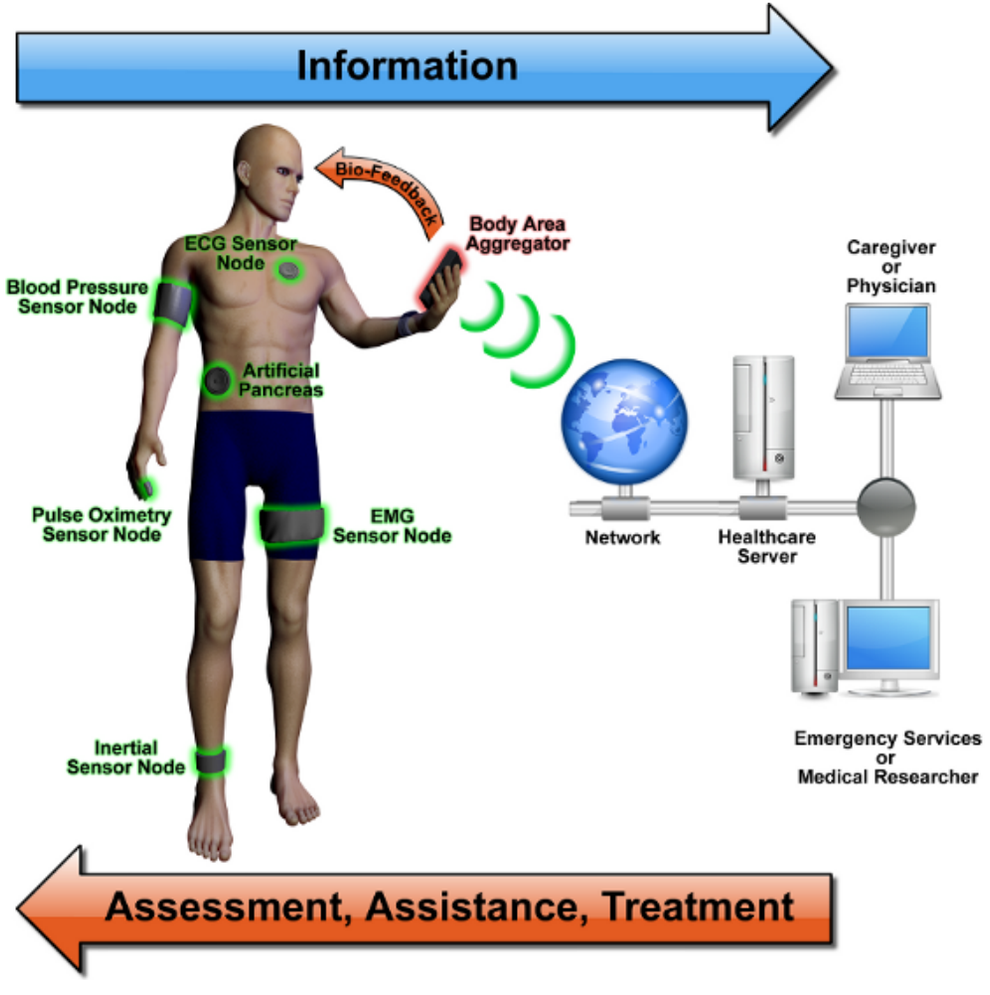


$$T_{clk\_period\_reg} > T_{ck-q} + T_{prop\_delay} + T_{setup} - T_{clock-skew}$$

$$T_{prop\_delay} > T_{hold} + T_{clock-skew}$$

Metastability → Timing errors → Performance degradation and yield

Problem Statement



Source: http://inertia.ece.virginia.edu/engineering-research/body-area-sensor-networks

- Self-Powered systems are severely energy-constrained
- Small form-factors
- Longer operational lifetime for ubiquitous deployment
- Supply voltage variation (Harvesting conditions, Regulator drift etc.)

=> Need for a compact, ULP supply-voltage monitor and resiliency to voltage variation

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Overview of Prior Work

- Adaptive clock distribution and in-situ timing error detection and correction [1] ➔**Area**
- On-Die Analog Droop detectors [2] ➔**Higher Quiescent currents**
- Decoupling capacitors [4] ➔**Gate leakage**

=> Need **low cost**, **compact, ULP** supply voltage **droop monitors** in **high-efficiency** voltage regulators for ULP systems

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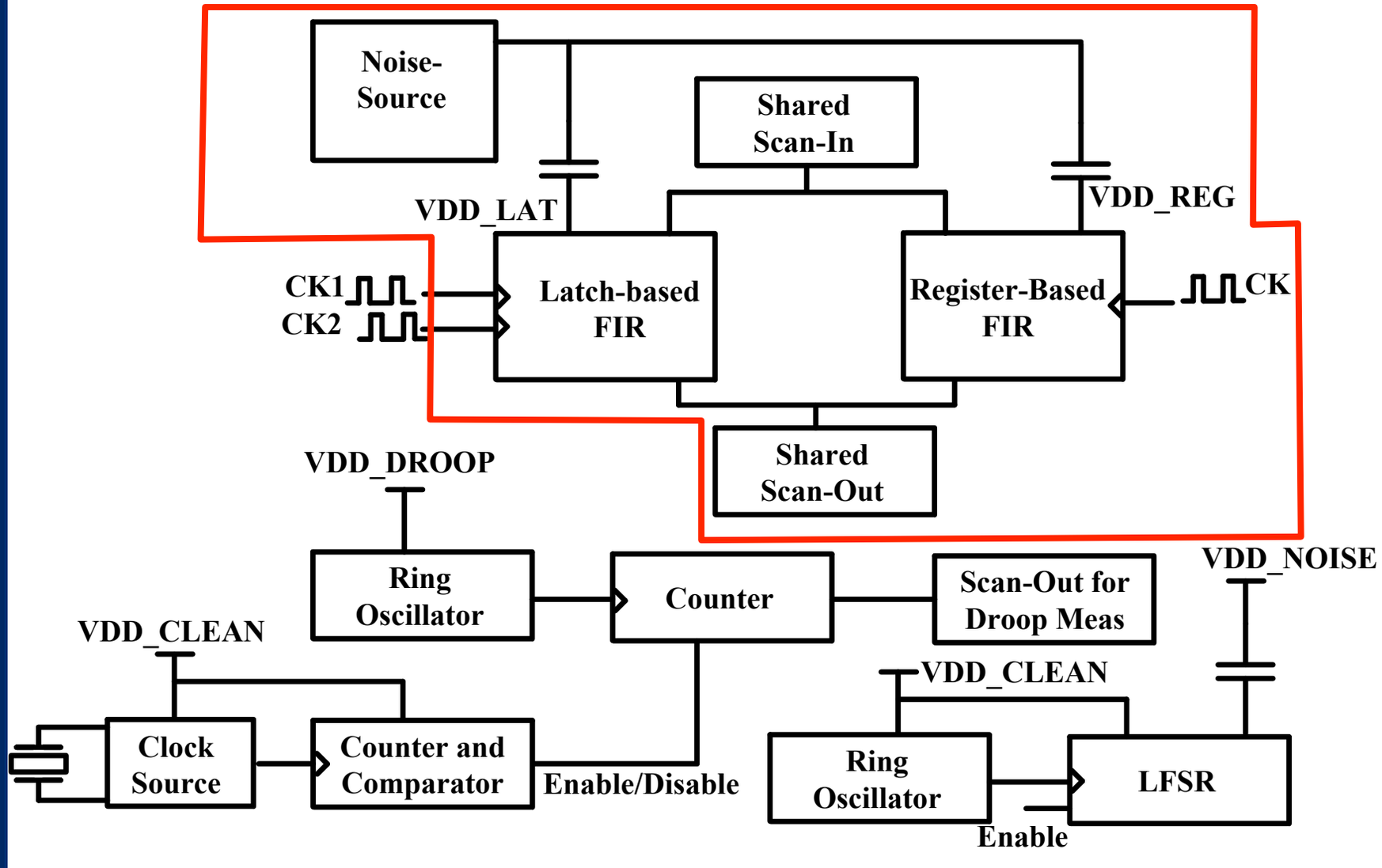
Proposed Solution and Hypothesis

- Power supply noise in latch-based vs. register-based implementations
  - Time borrowing and transparency window in latches can help in resolving metastability issues
  - Higher operating speeds in latches can reduce leakage energy in low VDD operation
- Propose an all-digital ULP droop measurement scheme with current-starved ROs and digital logic for calibration

Block Diagram



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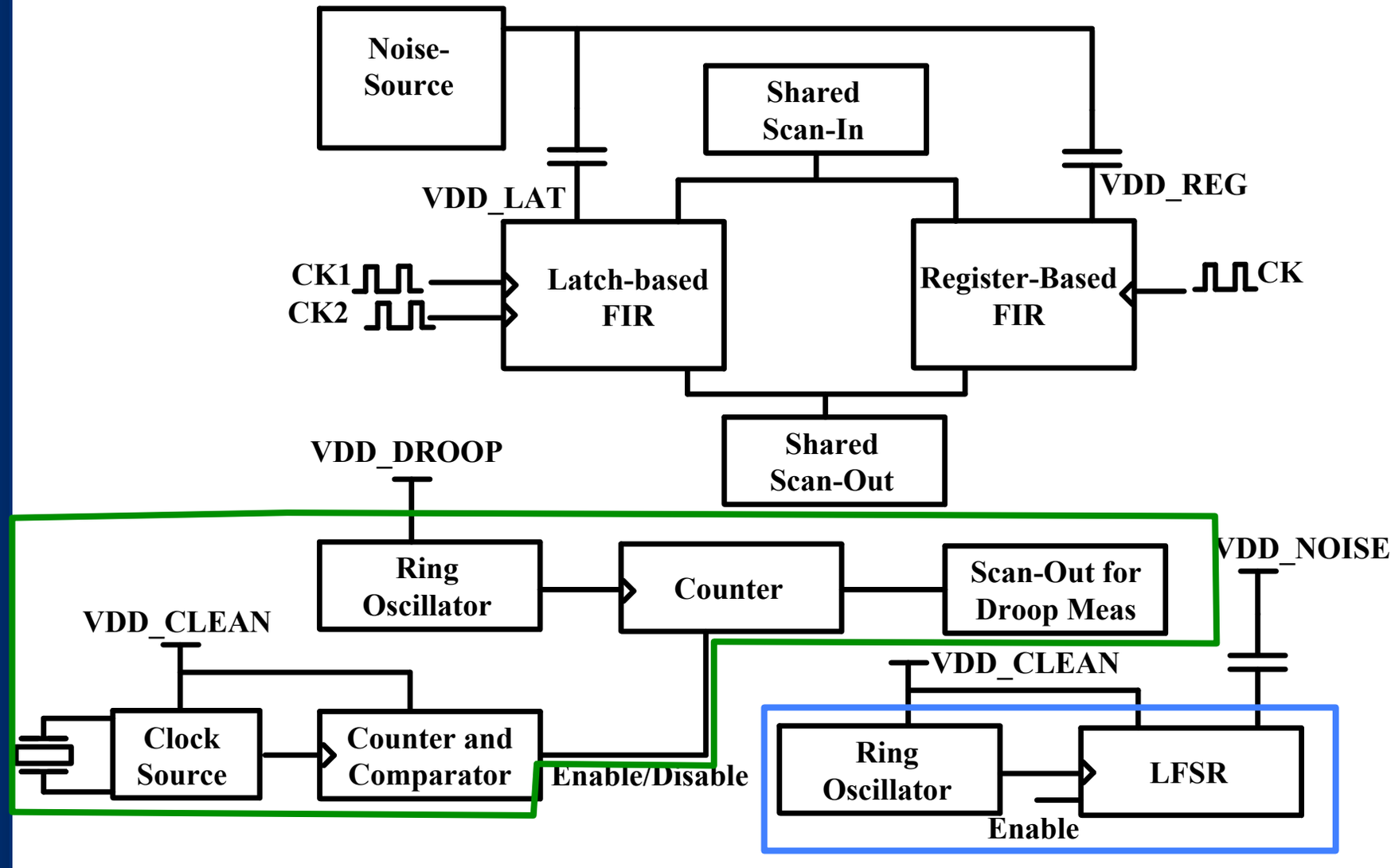
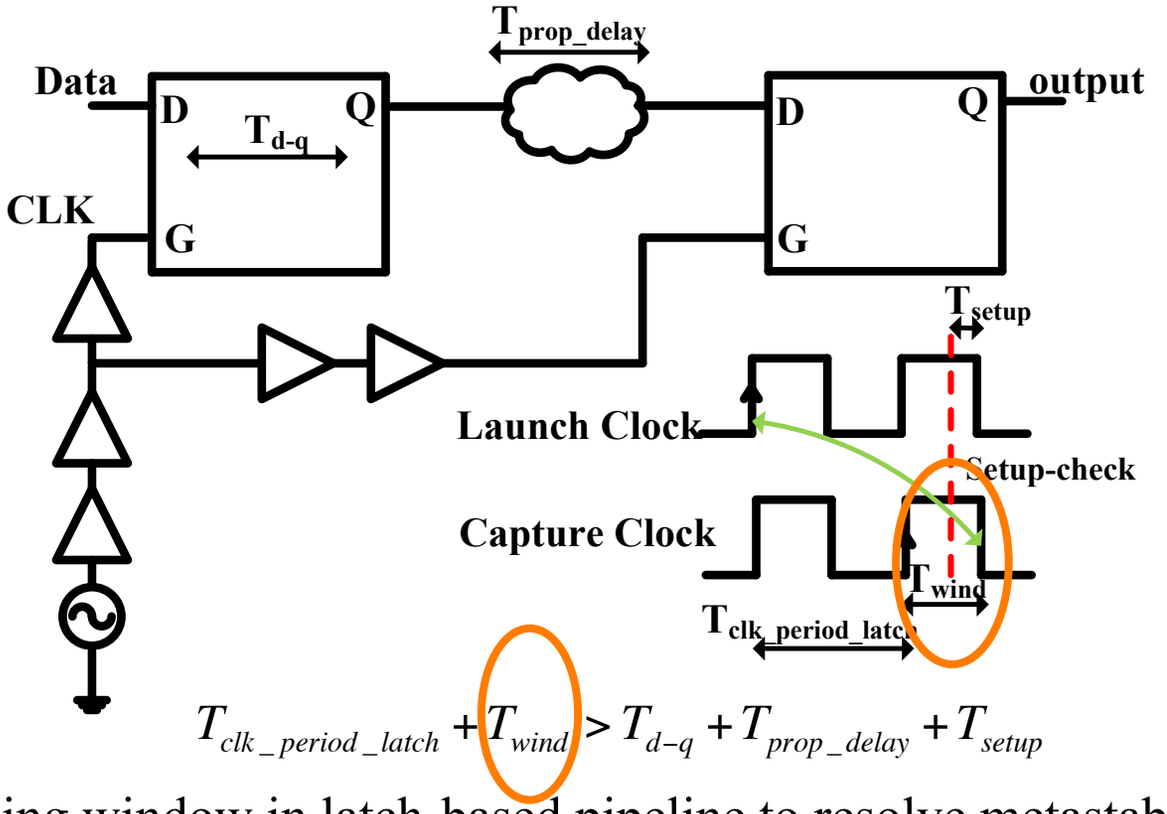


Latch-based implementation



$$T_{clk\_period\_latch} + T_{wind} > T_{d-q} + T_{prop\_delay} + T_{setup}$$

- Extra timing window in latch-based pipeline to resolve metastability
- Hold margins can be improved using non-overlapping clocks for launch and capture
- Higher operating speeds can amortize higher leakage energy in sub-V_T

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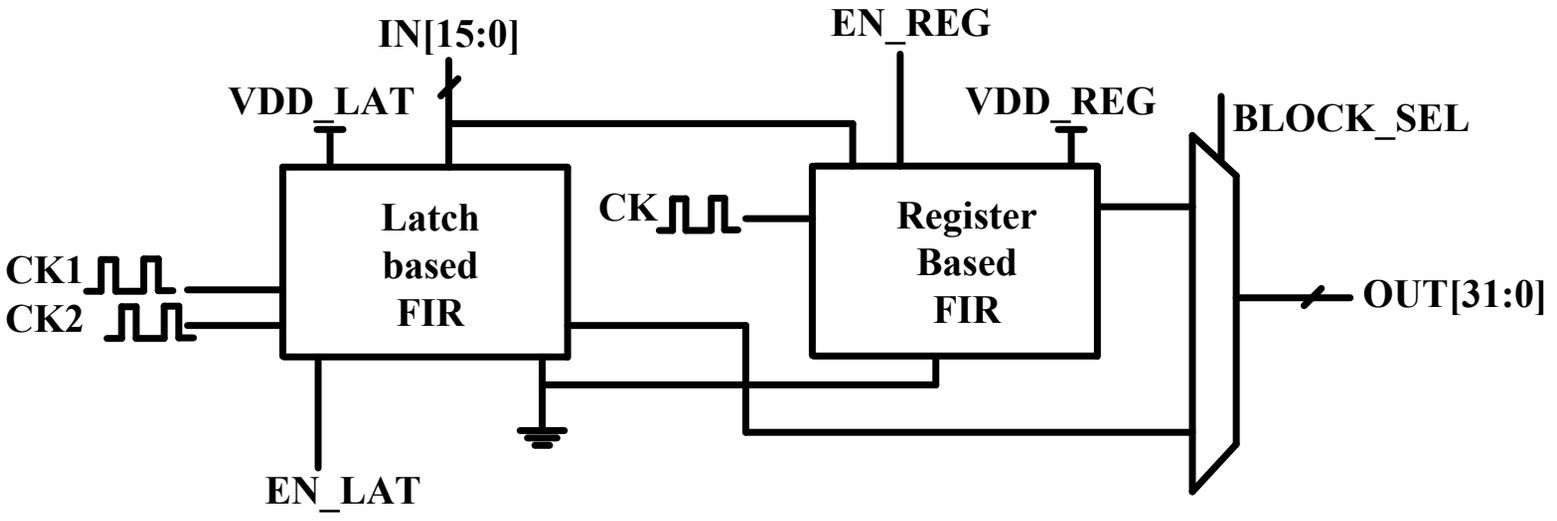
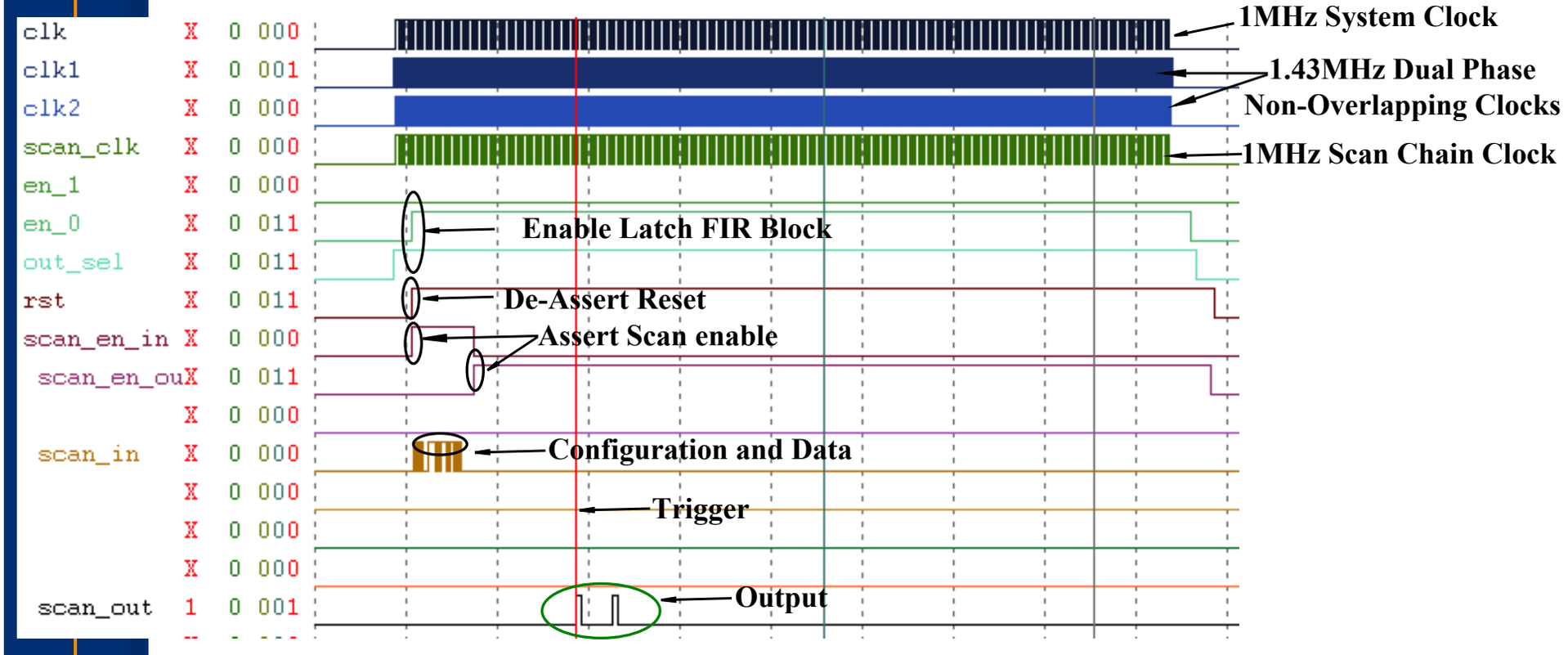
Latch-based vs. Register-based implementation: Test setup

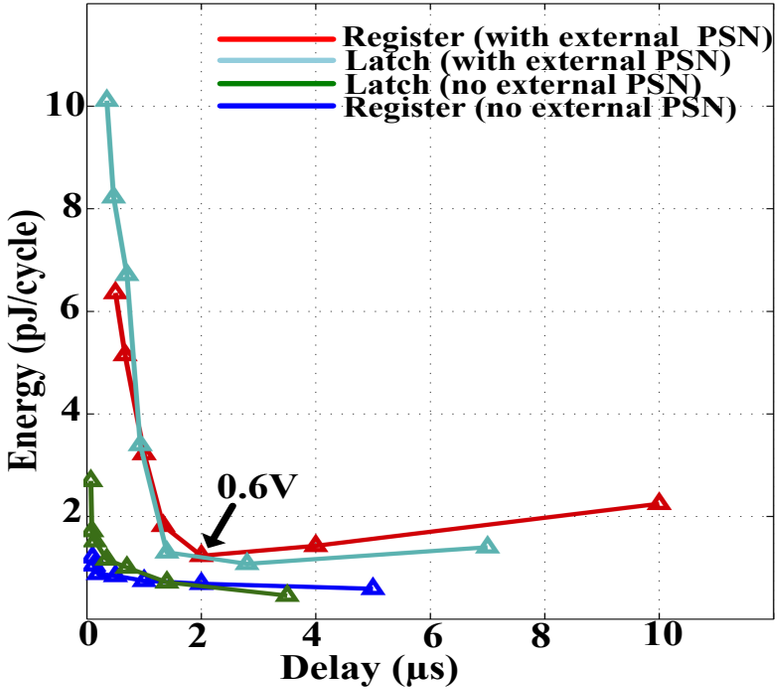


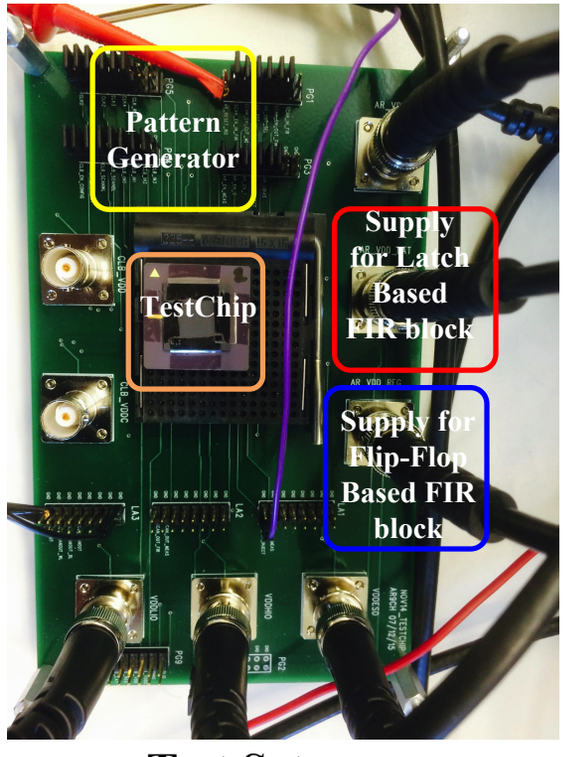
- 16-bit, 32-tap FIR filter used as DUT. Implemented using both latches and flip-flops.
- Latch-based implementation utilizes non-overlapping clocks (CK1 and CK2) for launch and capture → Improved hold-margins

Latch-based FIR implementation- Measured Waveforms



Latch-based vs. Register-based implementation-Measured Results





Test Setup

- **25-37% Improvement in energy-efficiency at low VDDs (< 0.6V)** in latch-based implementation in presence of low-frequency supply noise
- **44-120mV external 1kHz supply noise** injected for testing

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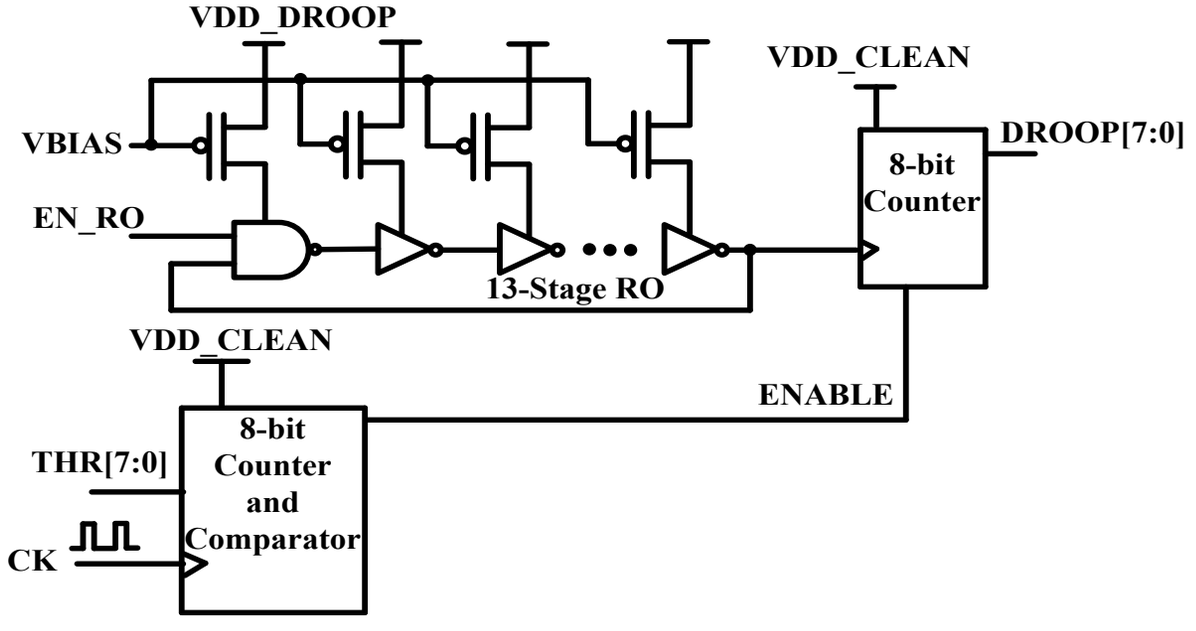
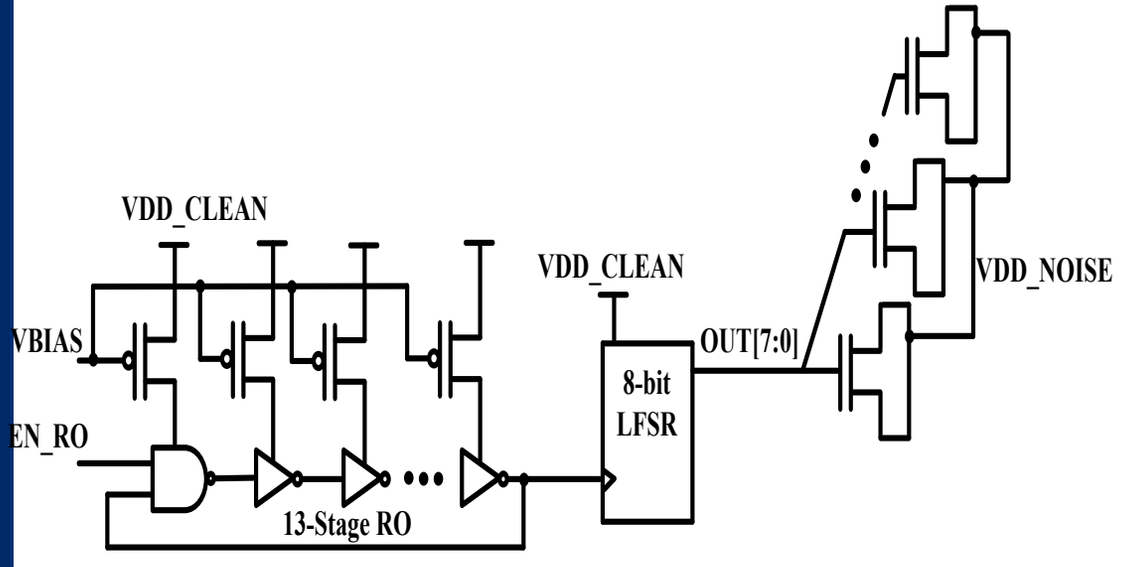
All-Digital on-die Power Supply Droop Measurement



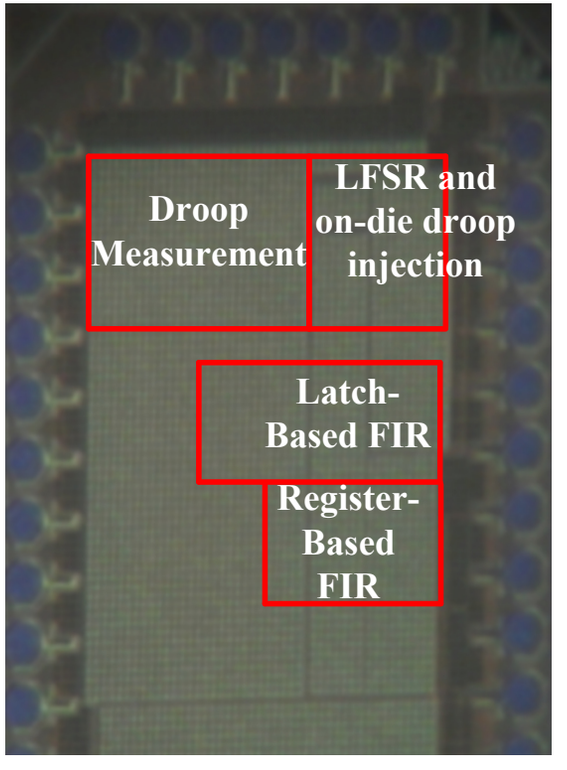
Droop Measurement Scheme

- Current-controlled ring oscillator operating at noisy supply
- A counter running at noise-free supply counts RO clock cycles

Droop Measurement Unit: Test setup



On-Chip Noise Injection Circuit



Die Photo

- On-chip noise injection: 8-bit LFSR clocked by a 13-stage current-starved RO couples an 8-bit pseudo-random noise sequence using on-chip capacitor-bank
- Off-chip noise injection: Variable amplitude 1kHz sawtooth waveform coupled to the supply using Agilent 33250A function generator

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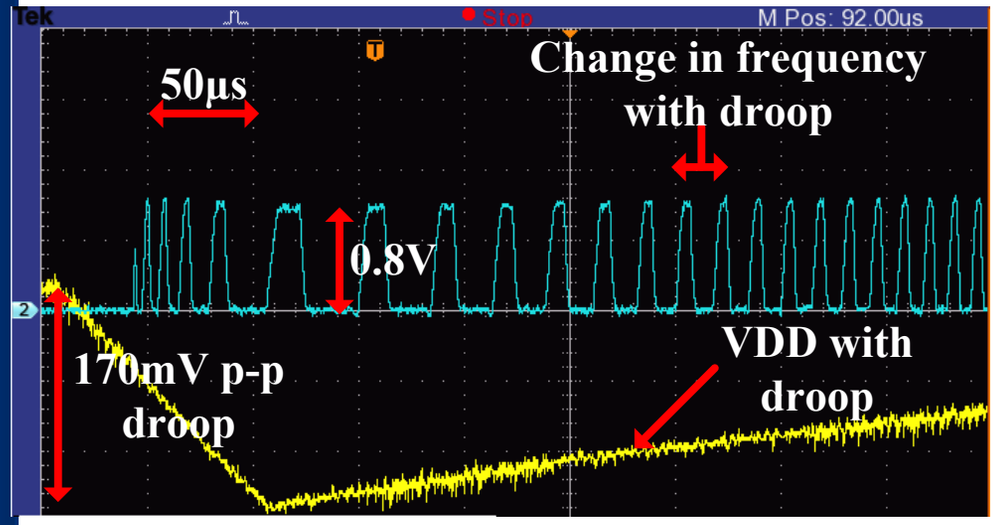
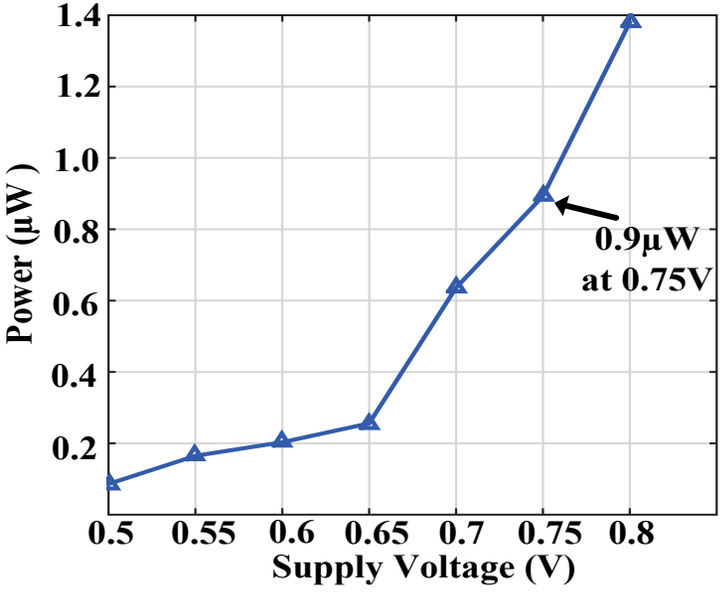
All-Digital Power Supply Droop Measurement Unit-Measured Results





VDD (V)	Peak-Peak Droop (mV)	Hex equivalent
0.8	48	0x07
0.8	72	0x19
0.8	104	0x4A
0.8	128	0x6E

Proxy for Supply droop magnitude

Droop Measurement Unit- Comparison with prior work

	[1]	[2]	[3]	**This Work**
Technology	16nm FinFET	90nm bulk	0.13µm bulk	**0.13µm bulk**
Supply Voltage	0.7-0.95V	0.7V-1.3V	0.74-1.3V	**0.5-0.8V**
Analog/Digital	Digital	Analog	Digital	**Digital**
Area	2590µm2	–	9060µm2	**7100µm2**
Power Consumption	2.5mW at 0.9V	–	46.4-56µW at 0.81V	**0.9µW at 0.75V**
Max Droop Range	90mV at 0.9V	270mV at 1V	189mV at 0.81V	**44-170mV at 0.5-0.8V**
High/Low frequency	High	High	Low	**Low**

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Summary

- We evaluated the impacts of power supply noise in a latch-based implementation of an FIR filter and compared with a register-based implementation
  - Time borrowing and transparency windows in latch-based pipelines help in resolving metastability issues
  - Higher operating speeds in a latch-based pipeline amortized leakage energy in low VDD operation
- We presented an all-digital ULP droop measurement scheme for ULP systems

References

[1] Bowman, K.A.; Raina, S.; et al., "A 16 nm All-Digital Auto-Calibrating Adaptive Clock Distribution for Supply Voltage Droop Tolerance Across a Wide Operating Range," in *Solid-State Circuits, IEEE Journal of* , vol.51, no. 1, pp.8-17, Jan. 2016

[2] Muhtaroglu, A.; Taylor, G.; Rahal-Arabi, T., "On-die droop detector for analog sensing of power supply noise," in *Solid-State Circuits, IEEE Journal of* , vol.39, no.4, pp.651-660, April 2004

[3] Kwanyeob Chae; Mukhopadhyay, S., "All-Digital Adaptive Clocking to Tolerate Transient Supply Noise in a Low-Voltage Operation," in *Circuits and Systems II: Express Briefs, IEEE Transactions on* , vol.59, no. 12, pp.893-897, Dec. 2012

[4] Jie Gu; Hanyong Eom; Kim, C.H., "On-Chip Supply Noise Regulation Using a Low-Power Digital Switched Decoupling Capacitor Circuit," in *Solid-State Circuits, IEEE Journal of* , vol.44, no.6, pp.1765-1775, June 2009

Thank You!