Soft Errors: Reliability Challenges in Energy-Constrained ULP Body Sensor Networks Applications

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***Abstract*— Aggressive technology and supply voltage scaling has led to increasing concern for reliability. Optimizing power and energy with sub-threshold (sub-V_T) operation exponentially increases the occurrences of both static and dynamic failures. With smaller node capacitances with each technology and supply scaling node, radiation-induced Single Event Upset (SEU) has become a critical design metric for Ultra-Low-Power (ULP) applications. In this paper, we explore the impact of radiation-induced soft errors on sub-threshold SRAM implemented in a Body Sensory Node (BSN) as an ULP application. We also demonstrate an exponential reduction in the critical charge (Q_{Crit}) of a storage node with supply in near- and sub-V_T design, resulting in a significant design consideration for the low-power applications. The huge process variation in sub-V_T results in 3X Q_{Crit} variation. Finally, we compare the trend of technology scaling and supply voltage scaling on Q_{Crit}.**

Keywords*— *Critical charge, ECC, robustness, single-event upset, SRAM, V_{MIN}, Variation Index, Write Margin.

I. INTRODUCTION

The trend of linear technology scaling has significantly reduced the reliability of digital systems. The transient change in the node value due to high-energy particle strikes has a complex relationship with an area over-designed approach and hence requires detailed research [1]. In [2], authors highlighted the severity of the device scaling below 1µm length by showing the short circuit between drain and source due to a single particle strike. In addition to technology scaling, the supply voltage (V_{DD}) has been scaled significantly to minimize the active energy (CV_{DD}^2) for Ultra-Low Power (ULP) applications such as wearable healthcare and wireless devices [3]. In [4], the authors show benefits of energy and leakage reduction at sub-V_T. However, sub-threshold operation poses critical reliability issues such as soft errors in sub-threshold have become a very critical problem to be addressed. Soft errors can cause a significantly higher failure rate than all the other reliability mechanisms combined. For example, a typical failure rate for a "hard" reliability failures such as gate oxide breakdown and electromigration is about 1-50 failure-in-time (FIT). There are half-a-dozen other critical reliability mechanisms which cumulatively cause 50-200 FIT. However, for an unprotected design, the SER can exceed 50000FIT per chip [5].

In this work, we study the impact of the radiation-induced soft errors in ULP applications operating at sub-V_T. We discuss the mechanism behind the soft errors in Section II followed by the experimental results in Section III. Finally, we conclude the paper in Section IV.

II. EXPERIMENTAL SETUP

The impact of particle strikes depends on the circuit design and therefore the concern of soft-error. The SRAMs, storing the state in two bi-stable elements, is considered to be robust because of the inherent feedback nature of the storage. However, with supply and technology scaling, denser SRAM with lower power requirement reduces the resiliency of the SRAM over technologies. Therefore, in our experiments, we consider a 6T SRAM bit cell design in 130nm technology that has been implemented in Body Sensor Node (BSN) [3].

We study the impact of particle strike on a reversed-bias pn junction that results in a current pulse with a particular rise time (t_R) and fall time (t_F). The current pulse generated due to the particle strike depends on many factors, including the size of the device, biasing V_{DD}, substrate doping, particle strike distance from the junction, the type of the ion particle, strength of the feedback path in the case of SRAM or FF, and well doping. For our experiment, we consider double-exponential pulse [6] as an impact of particle strike on the device. During the particle strike, the SRAM bitcell is considered to be in the 'Hold' state. An iterative process performs a binary search for an applied Q_{Coll} for which the node flip value is checked. Fig. 1 shows different current pulses based on the various t_F values. Here, the purpose of exploring various current pulse with different t_F is to understand the impact of the current pulse on the Q_{Crit}.

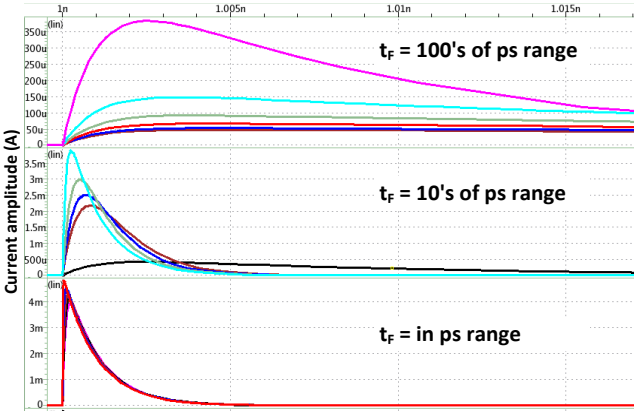

Fig. 1. Change in the pulse width of the current pulse is emulated by varying t_F of the pulse for a constant V_{DD} and Q_{Coll}.

III. RESULTS

Fig. 2 shows Q_{Crit} values for different particle strikes having different t_F. In the super-threshold range of supply voltages, the faster diffusion (shorter t_F) results in 100X Q_{Crit} reduction for the same amount of charge collected. The trend is predominant at super- and near-threshold range. While in the sub-threshold, even larger current pulse causes the flip due to the smaller node capacitance. The authors in [7] showed the difference in the charge collection property using a 3D device model for bulk/planner and FinFET. The result shows how different devices with different physical structures (e.g. bulk, FDSOI, FDSOI) with various charge collection properties impact the Q_{Crit}. Fig. 3 illustrates the effect of supply scaling on Q_{Crit}.

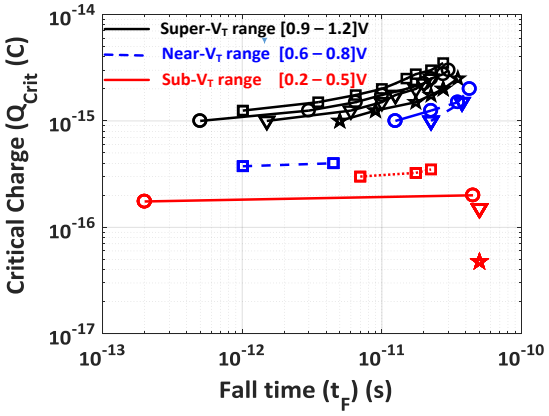

Fig. 2. Effect of t_F (i.e. charge collection property) on Q_{Crit} for the same value of Q_{Coll} at given V_{DD}.

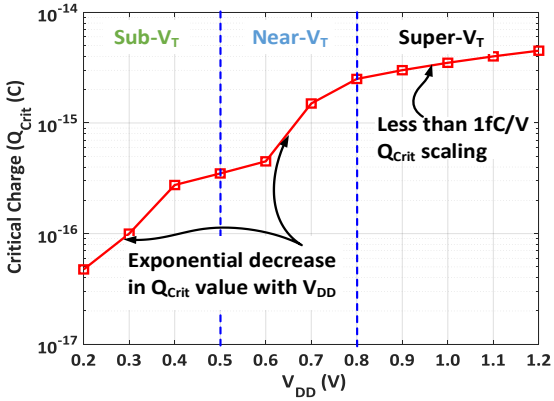

Fig. 3. Effect of Soft-Error on V_{DD} scaling.

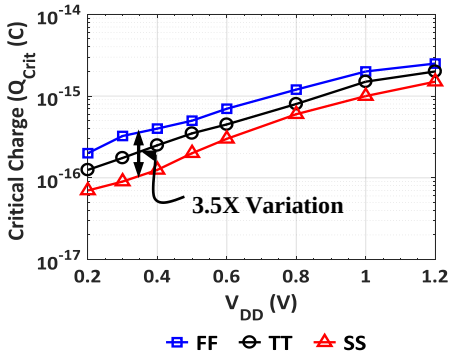

Fig. 4. Q_{Crit} has 3.5X variation across process variation for the 130nm technology node for the sub-threshold range of V_{DD}s

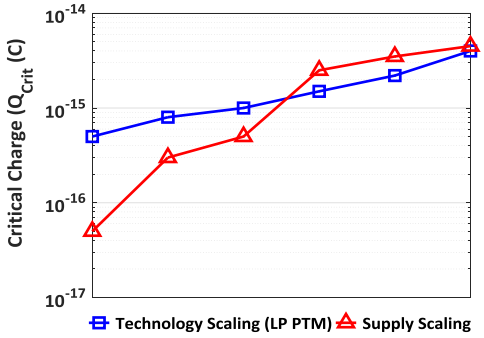

Fig. 5. Comparison: Impact of technology scaling vs. supply scaling on the Q_{Crit} of the storage node

In the super-threshold, scaling the supply voltage only reduces Q_{Crit} by less than 0.5fC/V and hence does not impact reliability until the supply scaling is limited to this range. However, in the near- and sub-V_T voltages, Q_{Crit} reduces exponentially. In this range of V_{DD}'s, the Q_{Crit} becomes so small that even a particle strike at nominal altitude with a lower flux can flip the node value. Because the ON current (I_{ON}) has an exponential dependency on the V_T in sub-threshold [4], process variation impacts Q_{Crit}. A reduced I_{ON} results in a weaker feedback path for the storage node in a crossed couple bitcell. Fig. 4 shows the impact of process variation on Q_{Crit}. To summarize the impact of supply scaling on soft errors, we compare the impact of technology scaling on the Q_{Crit} with the supply voltage scaling. We consider low-power (LP) device models from the PTM [8]. Fig. 5 shows linear scaling of the Q_{Crit} value with the technology scaling while an exponential decay with supply voltage scaling towards the sub-threshold range of V_{DD}s and hence suffices the need of better design consideration at scaled supply compared to a scaled technology node.

IV. CONCLUSION

In this paper, we explore the reliability challenges for ULP applications induced by soft-errors. While supply scaling has been proven as an efficient metric to optimize power and energy for battery-less BSN application, reliability at scaled supply voltage operation is a big challenge. We also studied the impact of multiple current pulses on a critical charge (Q_{Crit}). The results help to understand Q_{Crit} behavior for different device structures based on charge diffusion property. Finally, the supply scaling effect on Q_{Crit} has been studied. The impact of process variation in sub-threshold resulted in 3.5X higher Q_{Crit} shows significant reliability issue due to sub-threshold operation.

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