A 0.6V 8 pJ/write Non-Volatile CBRAM Macro Embedded in a Body Sensor Node for Ultra Low Energy Applications

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Abstract

A non-volatile CBRAM macro embedded with a body sensor node processing platform operates at low voltages down to 600mV for write and 300mV for read, enabling ultra low energy operation, compatibility with energy constrained digital systems, and no need for charge pumps.

Introduction

This paper presents a non-volatile (NV) embedded memory macro based on conductive bridging RAM (CBRAM) technology that enables a 100X reduction in write energy compared to FG Flash and provides write operations down to 0.6V, compatible with ultra low power SoCs. Recent advances in low energy electronics are driving many new applications for which limited energy is the primary constraint. For example, the wireless body sensor node (BSN) SoC in [1] demonstrated operation exclusively from low levels of harvested power without a battery in the system. In energy harvesting scenarios, when blackouts in the incoming harvested power are possible, or in long life data collection situations for which the battery may fail prior to data recovery, NV memory (NVM) is essential for storing instructions and collected data. These wireless nodes and body sensors operate at 1V and below, but existing NVMs require several volts for write operations. While charge pumps can boost to these voltages, they incur energy and area overhead and require special processes with HV devices. Further, the energy required for a write access is typically greater than 1 nJ for existing NVMs, which is a substantial cost for a system like [1] for which the entire chip consumes only 19 µW. There is a clear need for NVM solutions that offer write energy in the pJ range and <1V VDDs that are compatible with existing ultra low power SoCs.

Cell Technology and Macro Design

The operational principle of CBRAM is the reversible creation of an electrochemically induced nanoscale conductive link in a special dielectric acting as a solid-electrolyte (Fig 1). The bipolar reduction and oxidation is extremely energy efficient in contrast to unipolar ReRAM technologies that require high energy thermal processes to PROGRAM and ERASE the cell. For this work, the dielectric is GeS and the active anode material is Ag. The cell technology in this paper is based on Adesto^{TM}'s commercially available CBRAM products having 10K endurance and 10yr/70^{o}C retention. A more detailed comparison of this CBRAM technology to other NVMs can be found in [2]. The storage element includes an access transistor and a programmable conductive bridge whose on-resistance is directly controlled by the amount of energy supplied during PROGRAM. In this work, we reduce the write energy by programming to higher resistances. Controlling the voltage at the access device gate (VWL) lets us set the PROGRAM resistance value and thereby control PROGRAM energy. A streamlined bipolar direct write scheme is used to maximize voltage head room and to control PROGRAM energy with the access device, resulting in the lowest write voltages (e.g. 0.6V, Fig. 2) and energies to date.

Fig. 3 shows the structure of the CBRAM macro and the voltages for different operations. A novel dual bit line (BL) approach, bit line anode (BLAN) and bit line source (BLS), improves cell isolation and optimizes energy requirements in the BL drivers, which drive the BLs directly to reduce the number of series transistors in the write path. The bipolar operation of the cell enables a simple PROGRAM/ERASE scheme of driving BLAN-to-BLS polarity positive for PROGRAM and negative for ERASE. This circuit scheme allows the word line (WL) voltage VWL choice to dictate PROGRAM current; VWL=0.4V sets a high RON, reducing read and ERASE energy. It also places more voltage across the cell during ERASE, which, along with restoring VWL to 0.6V, improves ERASE efficiency. The read is performed from the anode to reduce loading capacitance and eliminate read disturb of PROGRAMMED bits. Unselected BLAN and BLS lines are forced to 0V for maximum isolation.

Read. The read circuit (Fig. 4) senses the accessed cell current (via 8:1 col mux) versus a binary weighted set of pull ups, MPU. The combo of pull-up current, array leakage, maximum off resistance, and MPU dimensions are designed to set the BLAN voltage near VDD/2 at the onset of read. A programmable MPU strength of 138 nA to 2.13 µA adjusts for different target PROGRAM resistances, design margins, and array leakage compensation, and the accessed cell (if PROGRAMMED) overcomes MPU to pull BLAN low. An on-chip energy monitor (Fig. 5) was embedded as a power supply (VLOAD) in which delivered current is mirrored through M1 and monitored off chip at VMEAS, simplifying array energy characterization. Using this monitor, Fig. 6 shows the measured energy vs. delay for reading at three MPU strengths, illustrating the flexibility to read across different programmed resistances. At the highest supported resistance point, read energy is 0.39 pJ/B or 49 fJ/b.

Write. Fig 7 shows the write path with WL control. The drivers control the BLAN and BLS during PROGRAM, ERASE, and read with the desired data pattern (see Fig. 3). Using the energy monitor, Fig. 8 shows the measured dynamic current profile for PROGRAM and ERASE events. Significant energy consumption only occurs after the PROGRAMMING event, when the bias current flows through the lower on resistance of the CBRAM. This post-PROGRAM energy can be controlled using PROGRAM detection circuits or algorithmic variants like pulse/verify. After fitting our Verilog-A model of the CBRAM cell to measured data, we simulated the energy/bit for PROGRAM to a specific resistance or for ERASE from a specific resistance (Fig. 8). The optimum energy voltage is lower for higher resistances because the support circuitry energy begins to dominate earlier. The measured ERASE energy trace shows that the time to ERASE is the dominant factor for energy, while post-ERASE energy is set by the macro leakage. Driving VWL higher than VCC (e.g. by 400mV) also speeds the ERASE time, lowering ERASE energy. Simulations (Fig. 8) of ERASE show that voltages around 1V minimize energy (due to the higher ERASE current resulting in exponentially shorter times), but the energy to ERASE at lower voltages is smaller for higher PROGRAM resistance. Our measurements in Fig. 8 of the embedded CBRAM array confirm that we can PROGRAM at 0.6V for 1 pJ/b and ERASE at 0.6V for 8 pJ/b. The measurements for PROGRAM and ERASE are done through use of the energy monitor circuit (Fig. 5).

BSN SoC Integration and Measurement Results

To validate its applicability to low power systems, we embedded two CBRAM macros in a subthreshold SoC that provides a digital platform for BSNs (Fig. 9) that can process ECG, EEG, and EMG signals. The BSN architecture, derived from [1], includes a programmable RISC processor, custom node controller, DMA, and accelerators for heart-rate (RR) extraction, atrial fibrillation (AFib) detection, 30 tap FIR, and envelope detection. The CBRAMs act as instruction and data memories (IMEM, DMEM). Measurements in Fig. 9 show the chip executes correctly from the IMEM even after a day of power down, confirming non volatile storage and successful embedded operation of the low voltage arrays. In summary, this paper shows a sub-1V embedded NVM (Fig. 12) with over 3X lower write voltage and nearly 10X lower write energy than other NVMs (Fig. 10, Fig. 11). The low voltage operation supports integration with CMOS SoCs without requiring charge pumps or energy intensive write operations.

Acknowledgements

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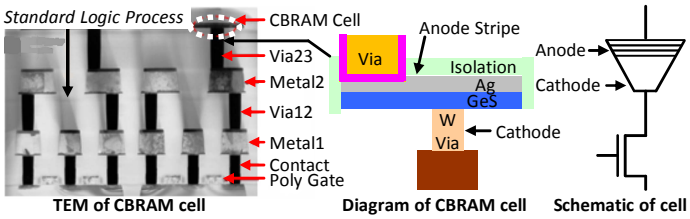


Fig. 1. CBRAM technology based on reversible creation of a conductive link in Ag/GeS.

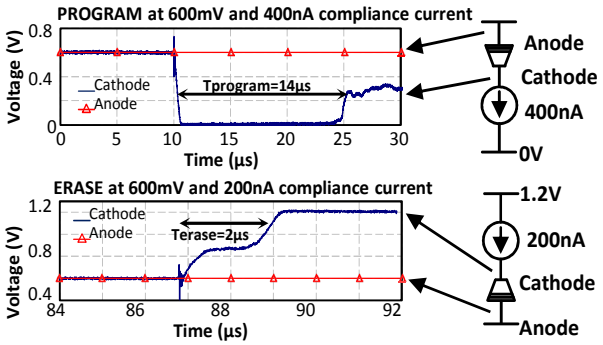


Fig. 2. Measured cell operations show low energy writes (program and erase) at 0.6V.

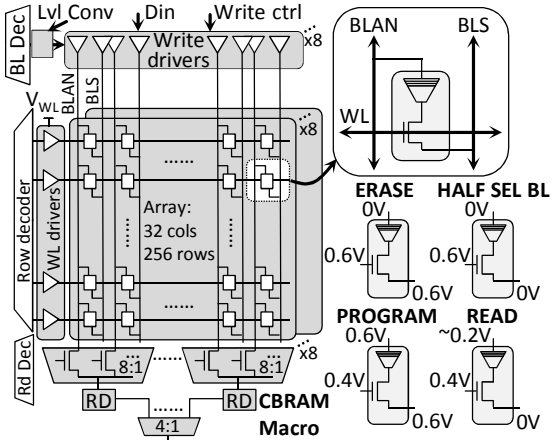


Fig. 3. The 64kb macro architecture. A streamlined dual-bit line cell access scheme improves low voltage read and write. Typical access voltages are shown.

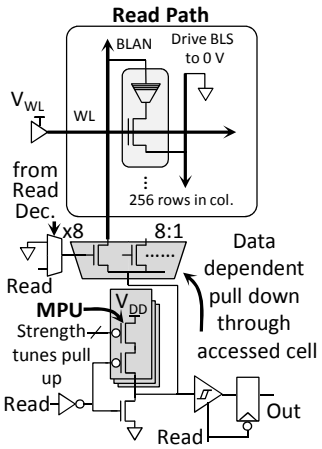


Fig. 4. Schematic of read path.

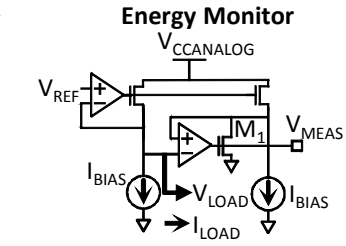


Fig. 5. On-chip energy monitor circuit.

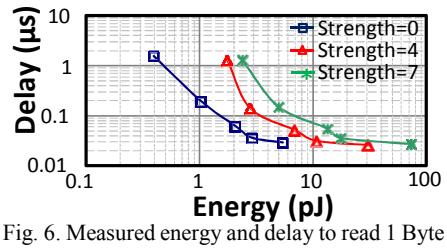


Fig. 6. Measured energy and delay to read 1 Byte for different read circuit strength values.

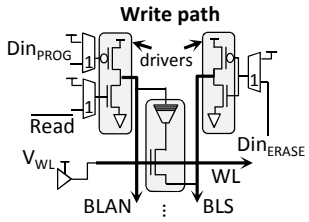


Fig. 7. Write circuits with short FET stacks work at compatible voltages with subthreshold digital chips, eliminating the need for charge pumps.

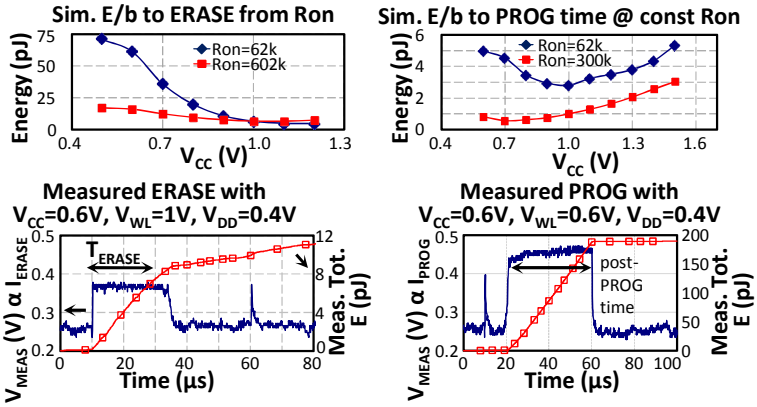


Fig. 8. Measured and simulated Program and Erase at 0.6V and low energy. →

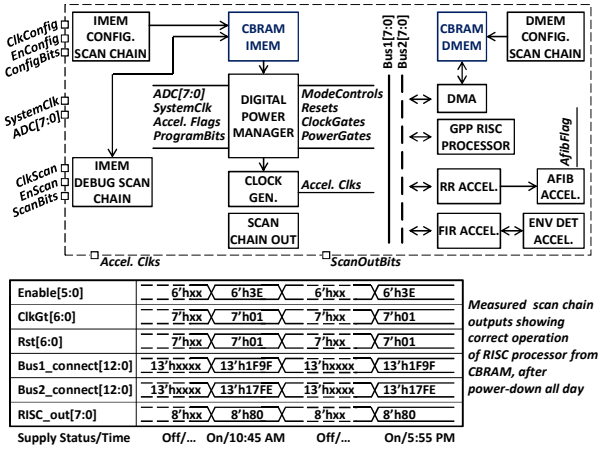
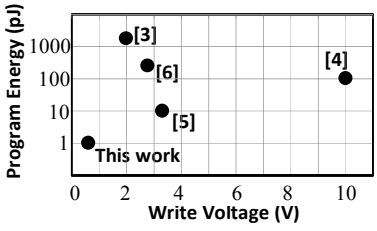


Fig. 9. Block diagram of a body sensor node digital platform using embedded CBRAM macros for non-volatile instruction memory and data memory. Measurements (bottom table) confirm non volatile storage overnight and successful SoC operation using the embedded arrays.

Metric	This work	[3]	[4]	[5]	[6]
Technology	CBRAM	ReRAM	FG Flash	MRAM	PCM
CMOS Compatibility	Yes	Yes	No	Yes	No
Read Core Voltage (V)	0.35	0.32	0.5	1.2	1.2
Write Core Voltage (V)	0.6	2.0	10	3.3	2.8
Program Energy/bit	1 pJ	2 nJ	100 pJ	10 pJ	250 pJ
Read Energy/bit	50 fJ	75 fJ	500 fJ	100 fJ	500 fJ
Charge pumps needed for <1 V SoC	No	Yes	Yes	Yes	Yes

Fig. 10. Comparison of this work with prior low voltage NVMs.



← Fig. 11. Energy/write and operating voltage. Our design is over 10X less energy, working at 0.6V.

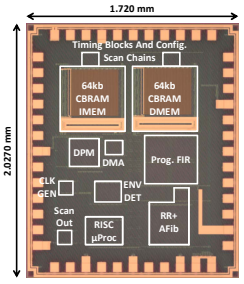


Fig. 12. Die photo showing 2 64kb macros integrated with BSN digital platform.