A 55nm Ultra Low Leakage Deeply Depleted Channel (DDC) Technology Optimized for Energy Minimization in Subthreshold SRAM and Logic

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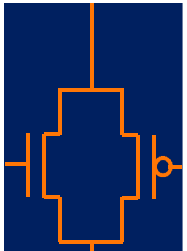
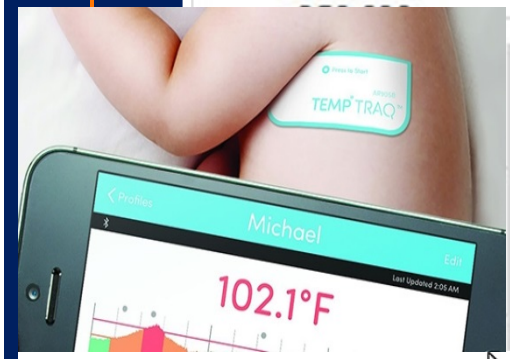
Robust Low Power VLSI

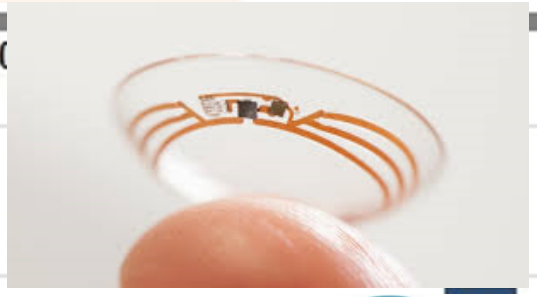


Outline

- Motivation
- Sub-threshold design challenges
- Technology overview
- Results: technology-circuit co-design
- Comparison

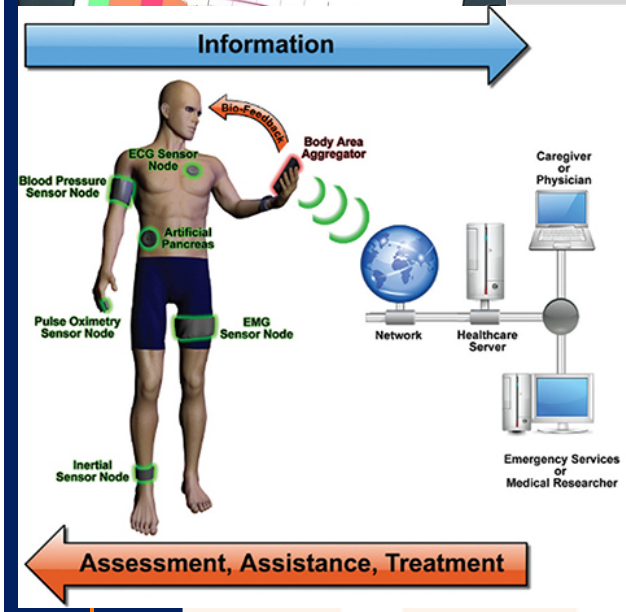
Motivation

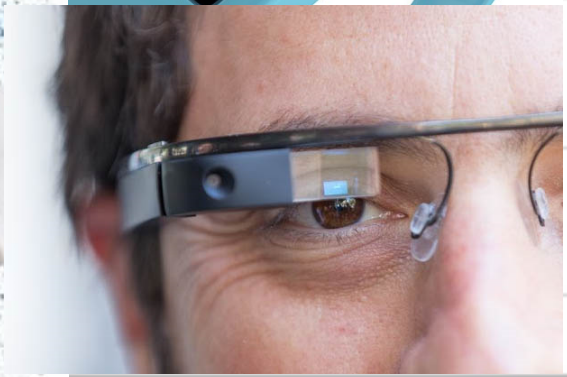




Wearable Device Shipments by [illegible] rkets: 20

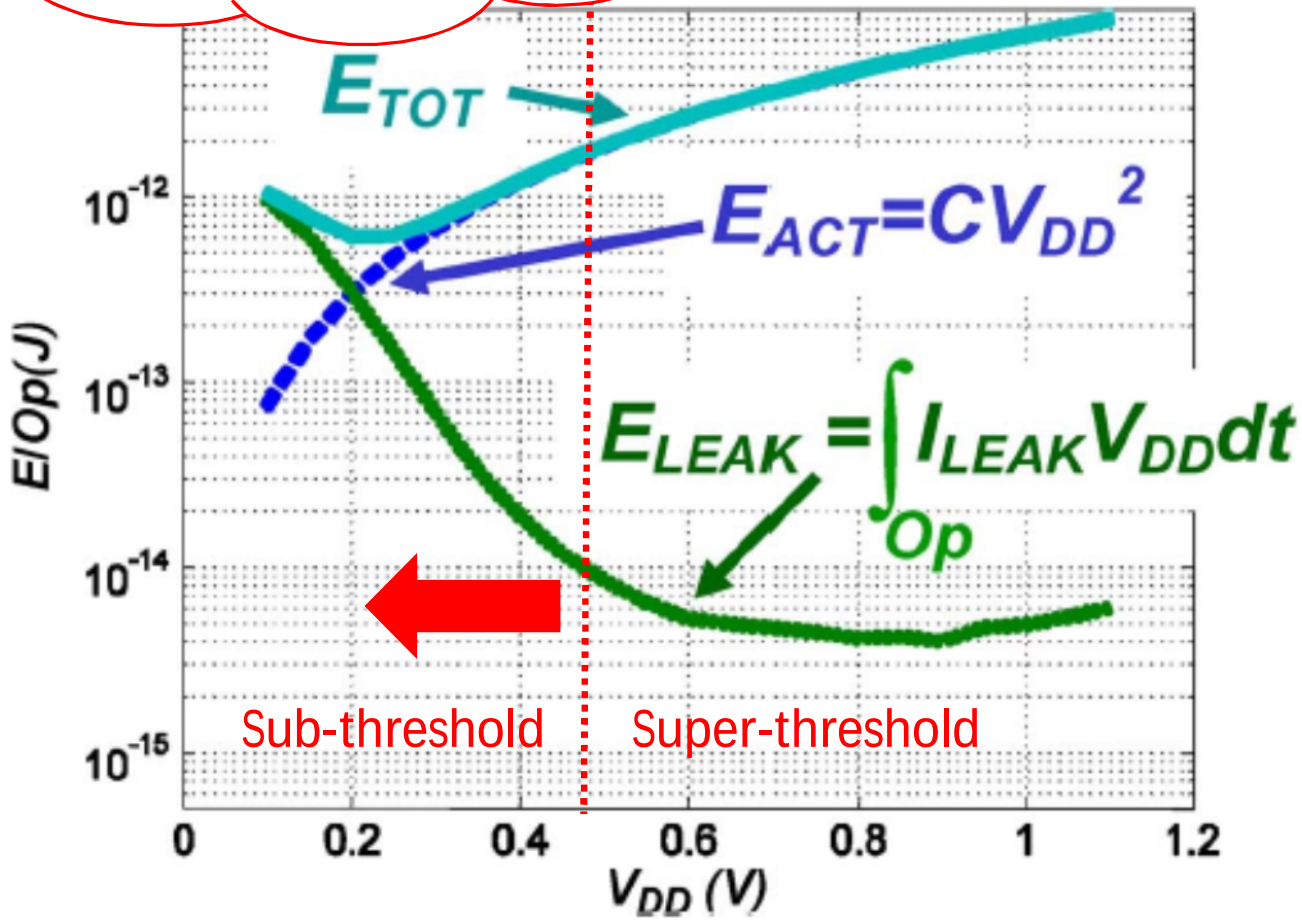
- Smart Watches
- Smart Glasses
- Smart Clothing
- Fitness Trackers
- Body Sensors
- Wearable Cameras
- Other Wearables



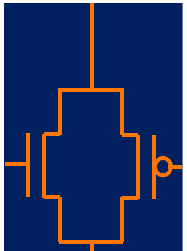


Motivation

Energy Minimization demands sub-threshold operations



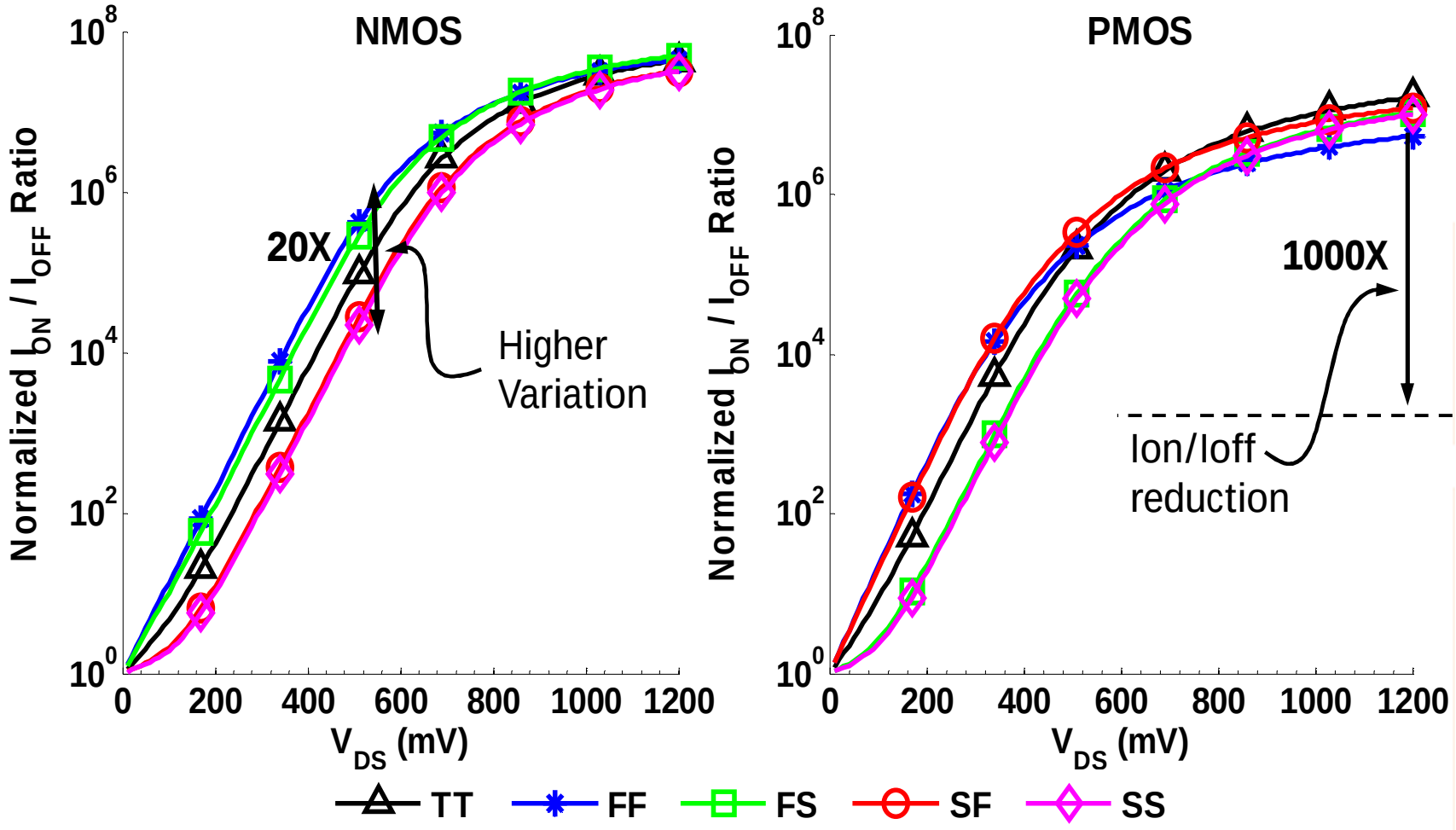
[Ref.] Naveen Verma Trans. on Elec. 2008



Sub-V_T Challenges

- Reduced drive current (I_{ON})
- Device-to-device mismatch due to huge V_T variation
- High Leakage
- Reduced noise margin

Sub-V_T Challenges



[Ref.] Harsh Patel et al., ISQED 2016

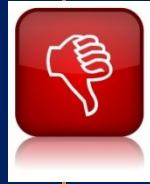
Available Solutions

Technologies:

[3]	[6]	[7]
32nm HK-MG	22nm ETSOI	FinFET
Provides higher I_{ON}; Reduced I_{OFF}	Improves performance	Improves performance
V_{DD} Scaling is limited to 1.0V (No sub-V_{TH} operation)	Doesn't address V_{TH} variation (No stable operation)	Still higher V_{TH} variation (No stable operation)

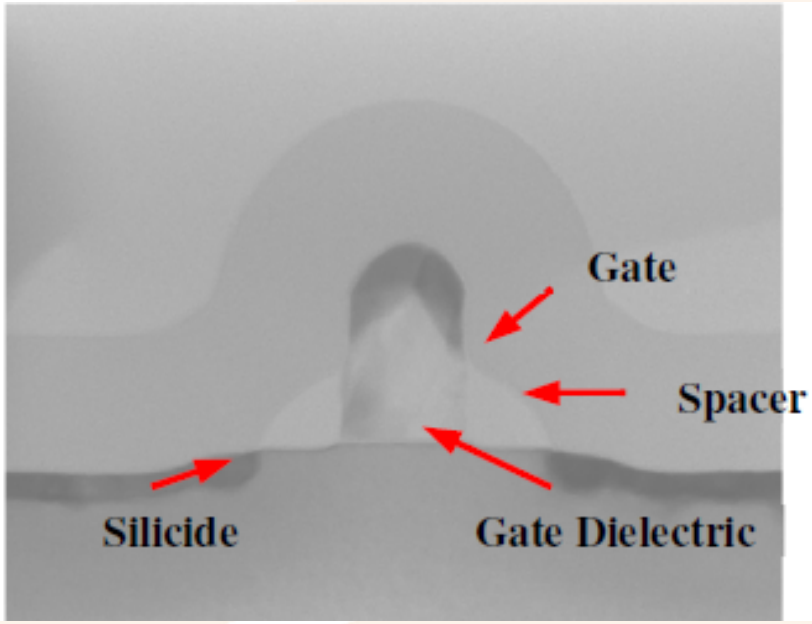
Available Solutions

Circuit Design:



High-V_T	Thick-Ox	Body Biasing
↑ channel impurities [9]	↑ Gate die-electric	Control body of FETs
↓ sub-threshold leakage (I_{OFF})	↓ Gate-leakage	↓ sub-threshold leakage (I_{OFF})
↑ RDF ↑ Junctional leakage	↑ V_T Variation ↑ Device mismatch	↑ Junctional leakage Saturates with increase in degree

Technology Overview



TEM view of DDC ULL device

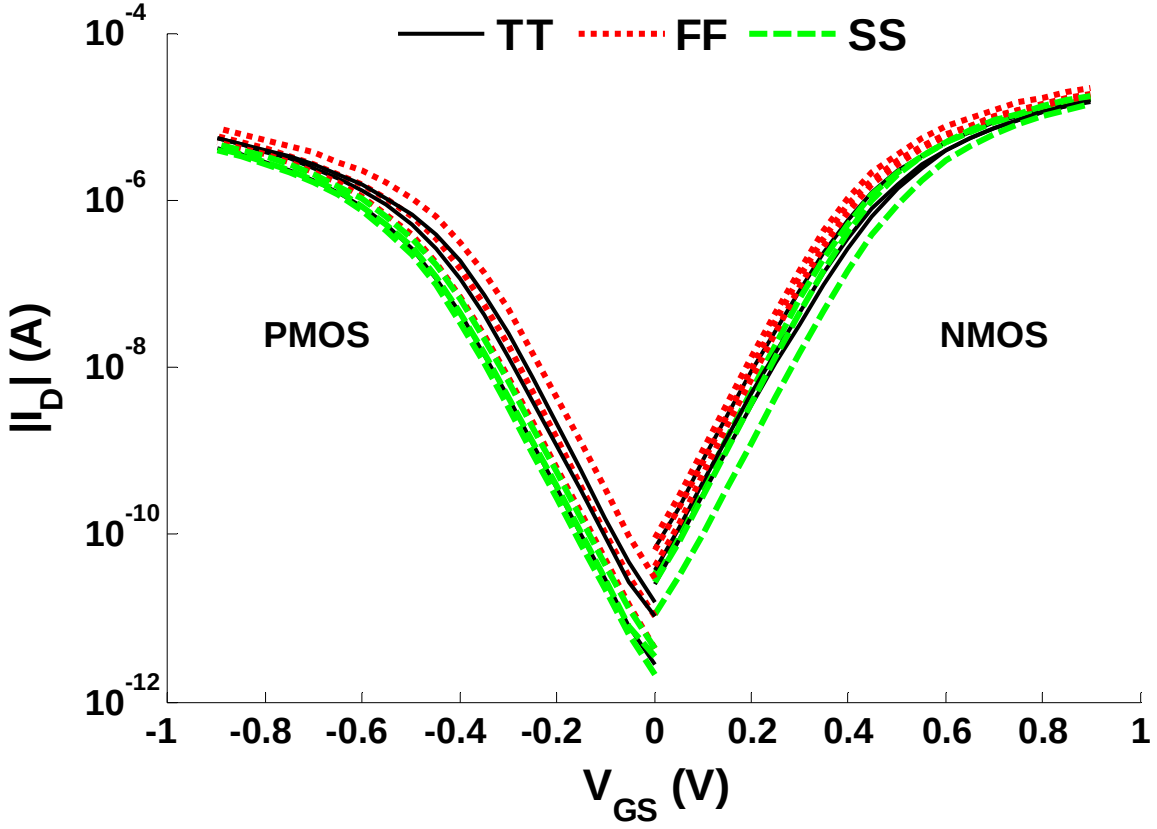
Technology:
Deeply Depleted Channel (DDC)

Gate Length (nm):
55

Devices:
Ultra-Low Leakage (ULL)

Enabling Circuit-level Technique:
Reverse Body Biasing (RBB)

Sub-V_T Challenges: Reduced I_{ON}

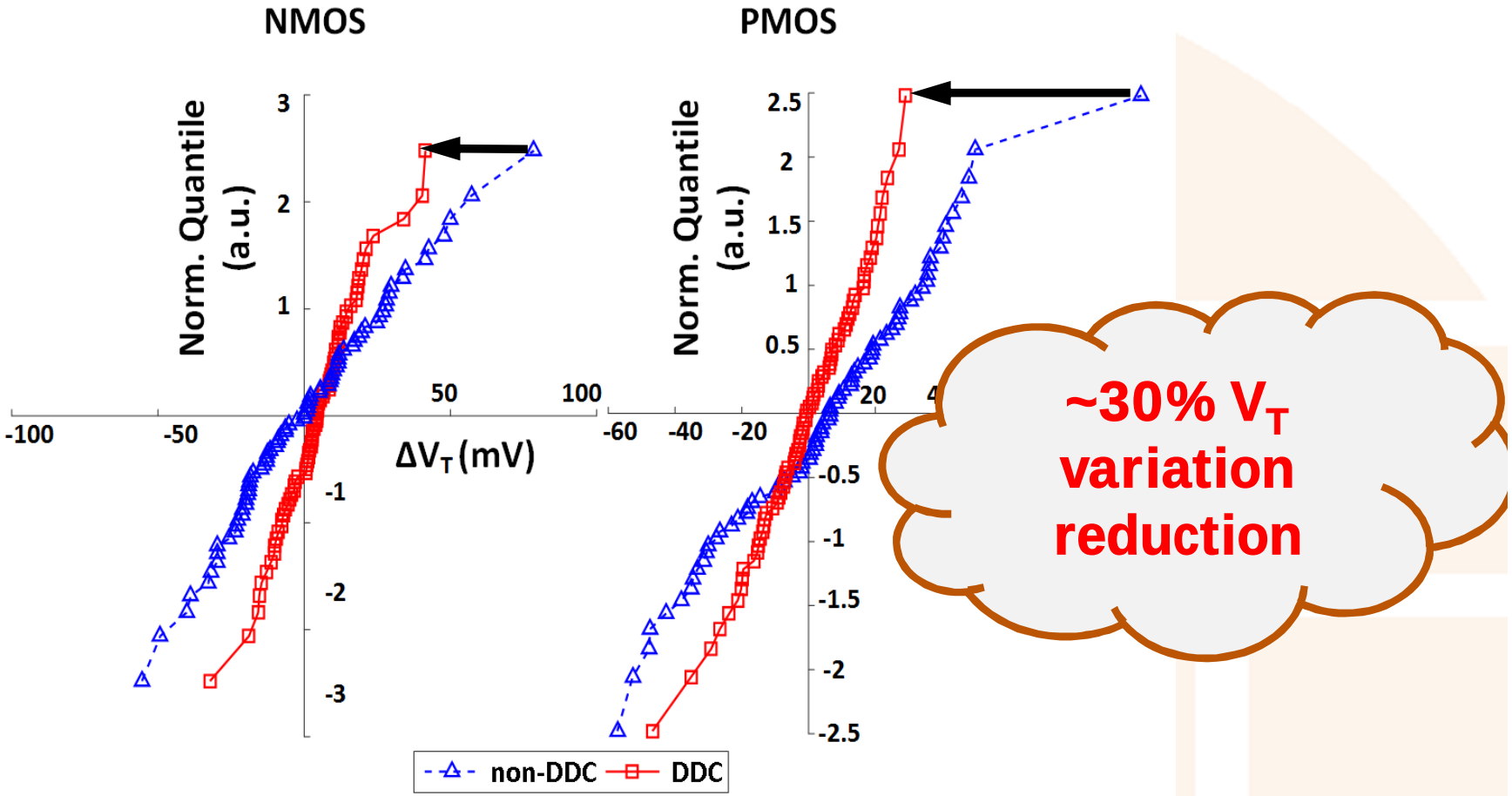


Measured I_D vs V_{GS} across multiple samples and across process corners

Sub-threshold Optimization:

- **DDC shows higher I_{ON}/um**

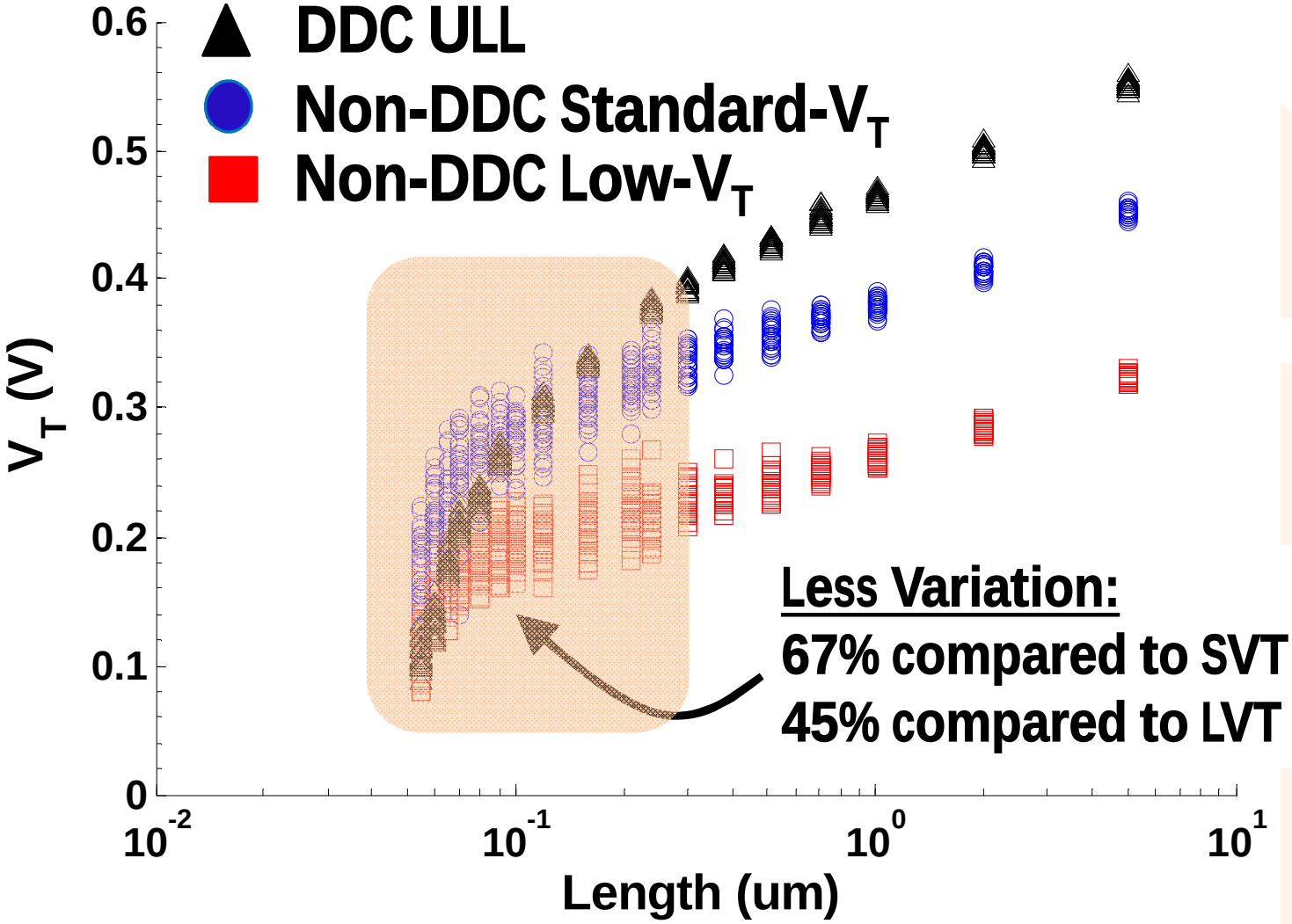
Sub-V_T Challenges: V_T variation



~30% V_T variation reduction

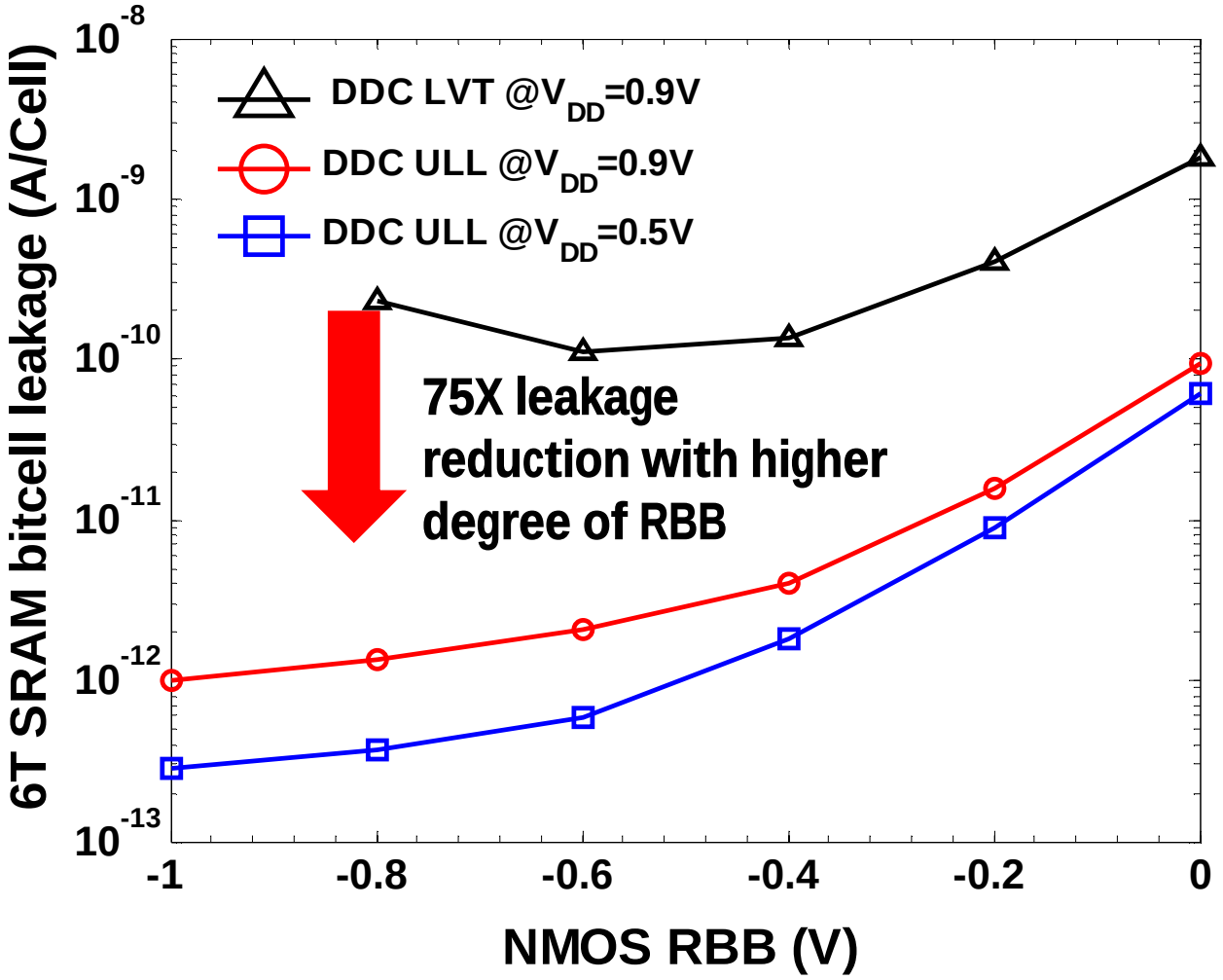
V_T variation spread comparison

Sub-V_T Challenges: V_T variation



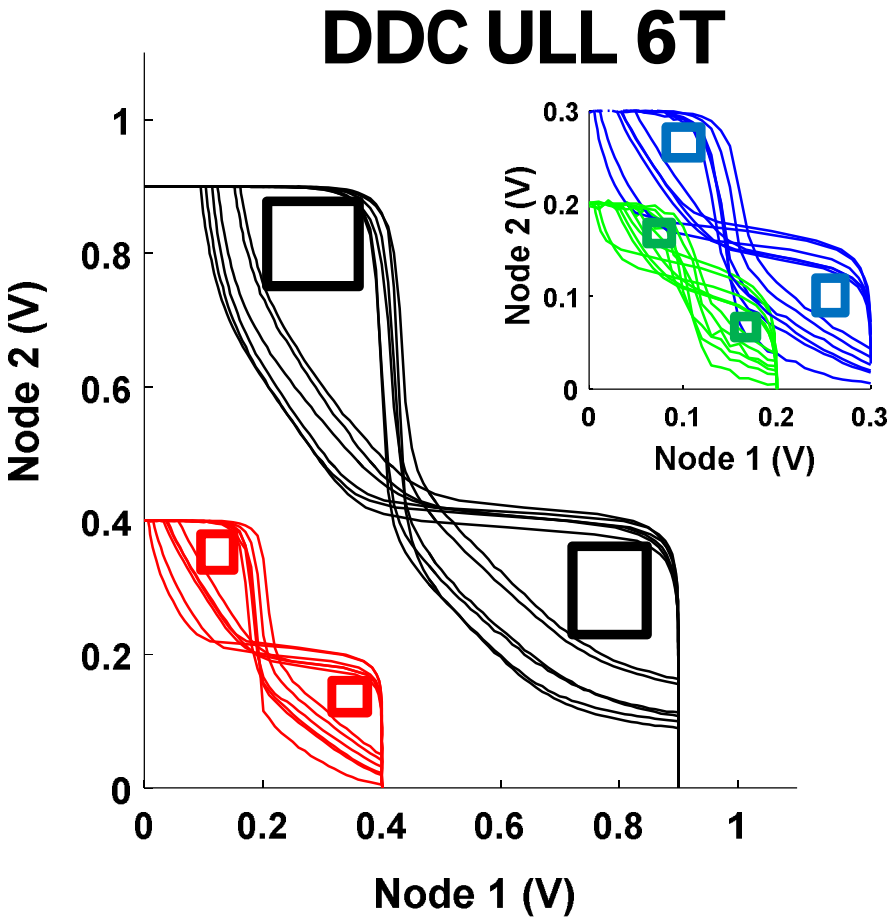
V_T roll-off comparison

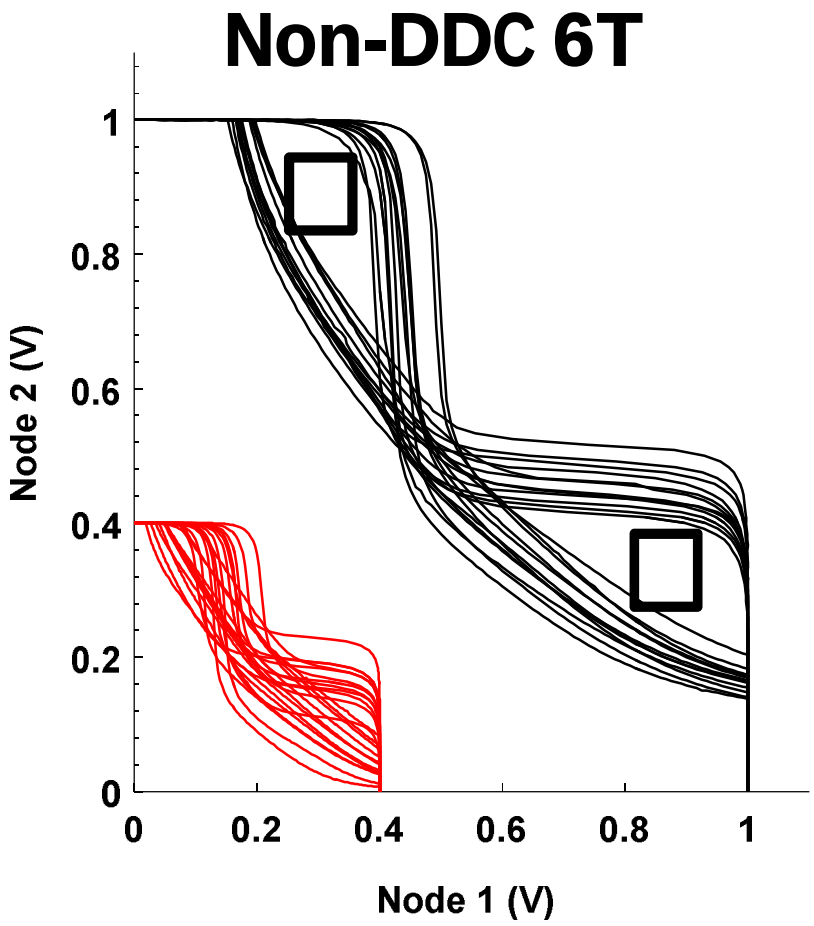
Sub-V_T Challenges: Leakage



75X 6T bitcell leakage minimization with a higher degree of RBB.

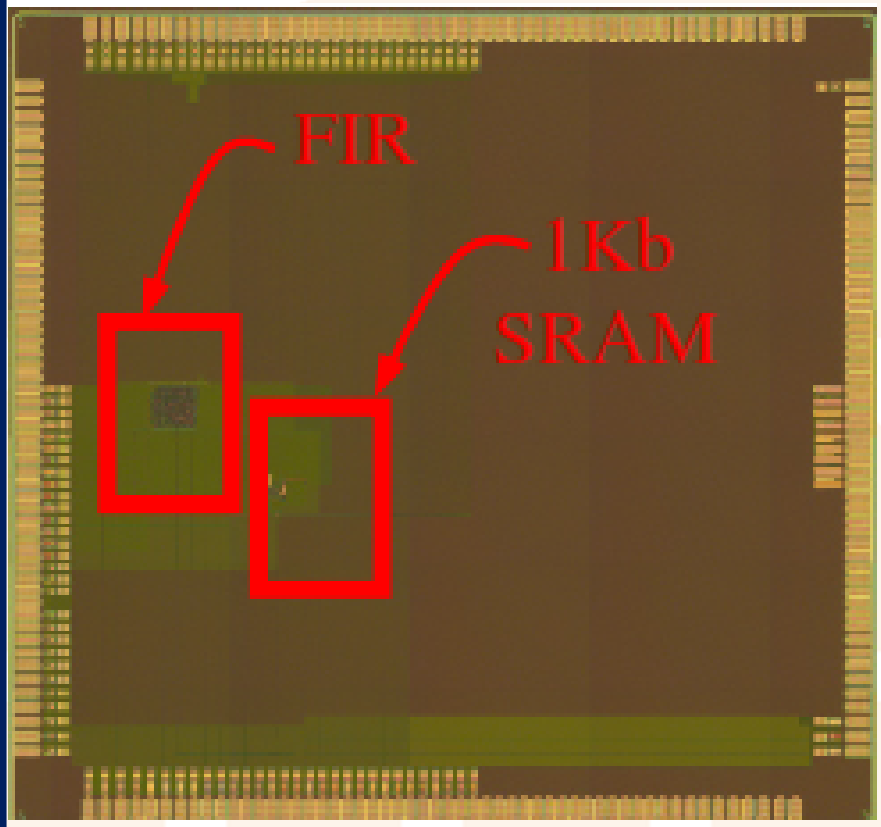
Sub-V_T Challenges: Noise Margin





Butterfly curves for SRAM 6T bitcell: DDC ULL vs. non-DDC (conventional) bitcell

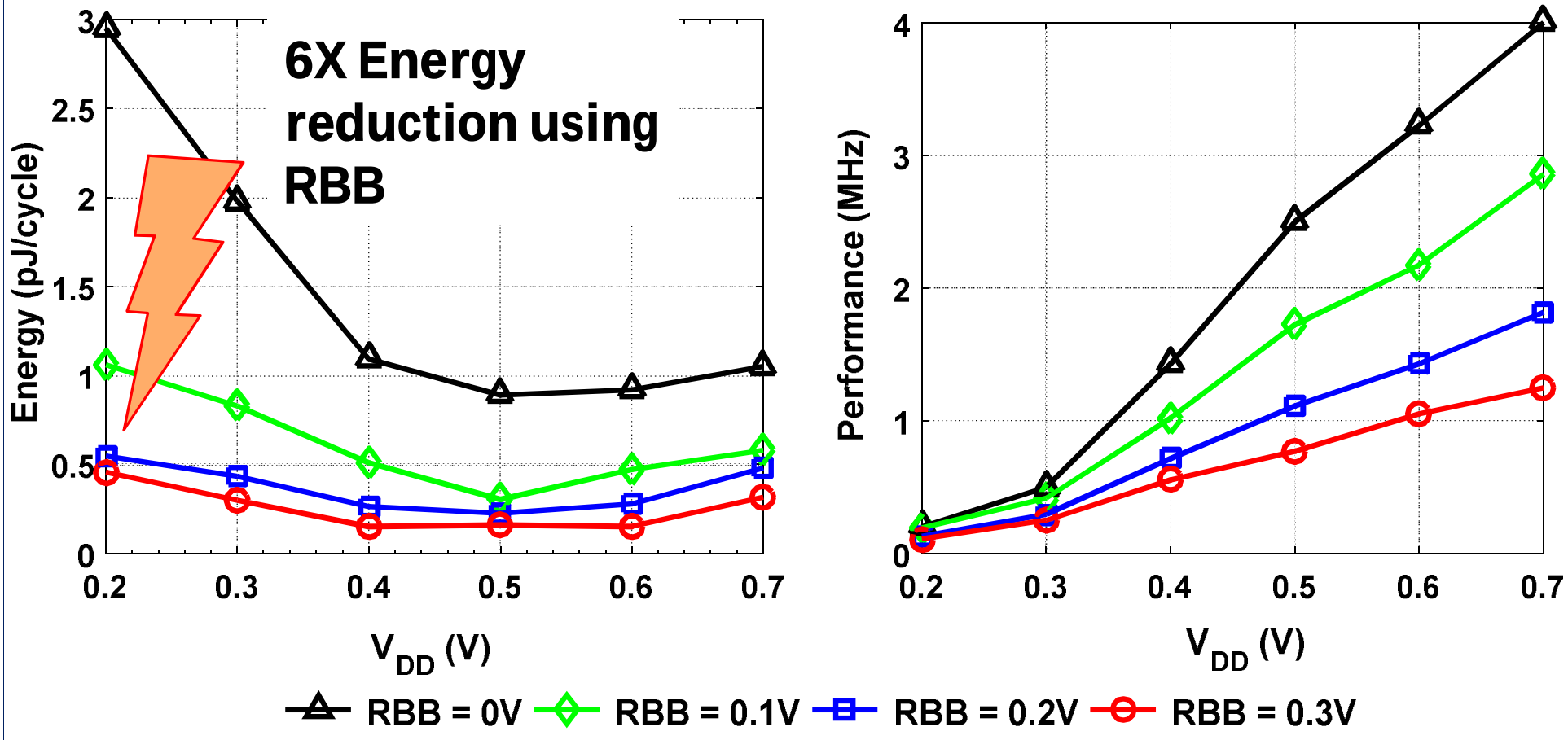
Test-Chip Results



Fabricated chip with 1kb SRAM and 16-bit FIR block

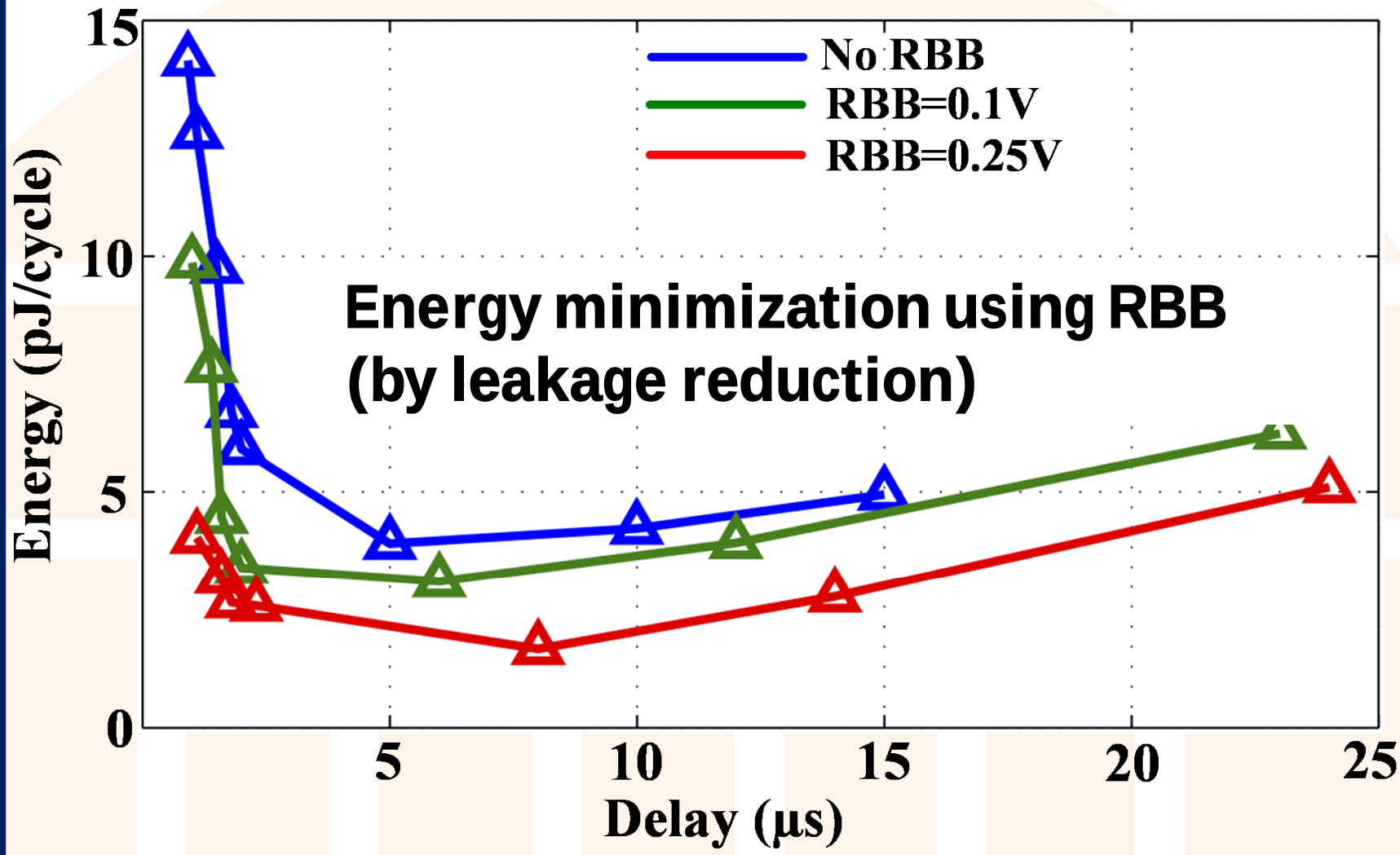
- Circuit techniques (sub-V_T operation and RBB) are co-designed with the technology to maximize the energy power saving.
- 1Kb 6T SRAM, 32-bit FIR, and Ring. Osc.

Test-Chip Results: SRAM

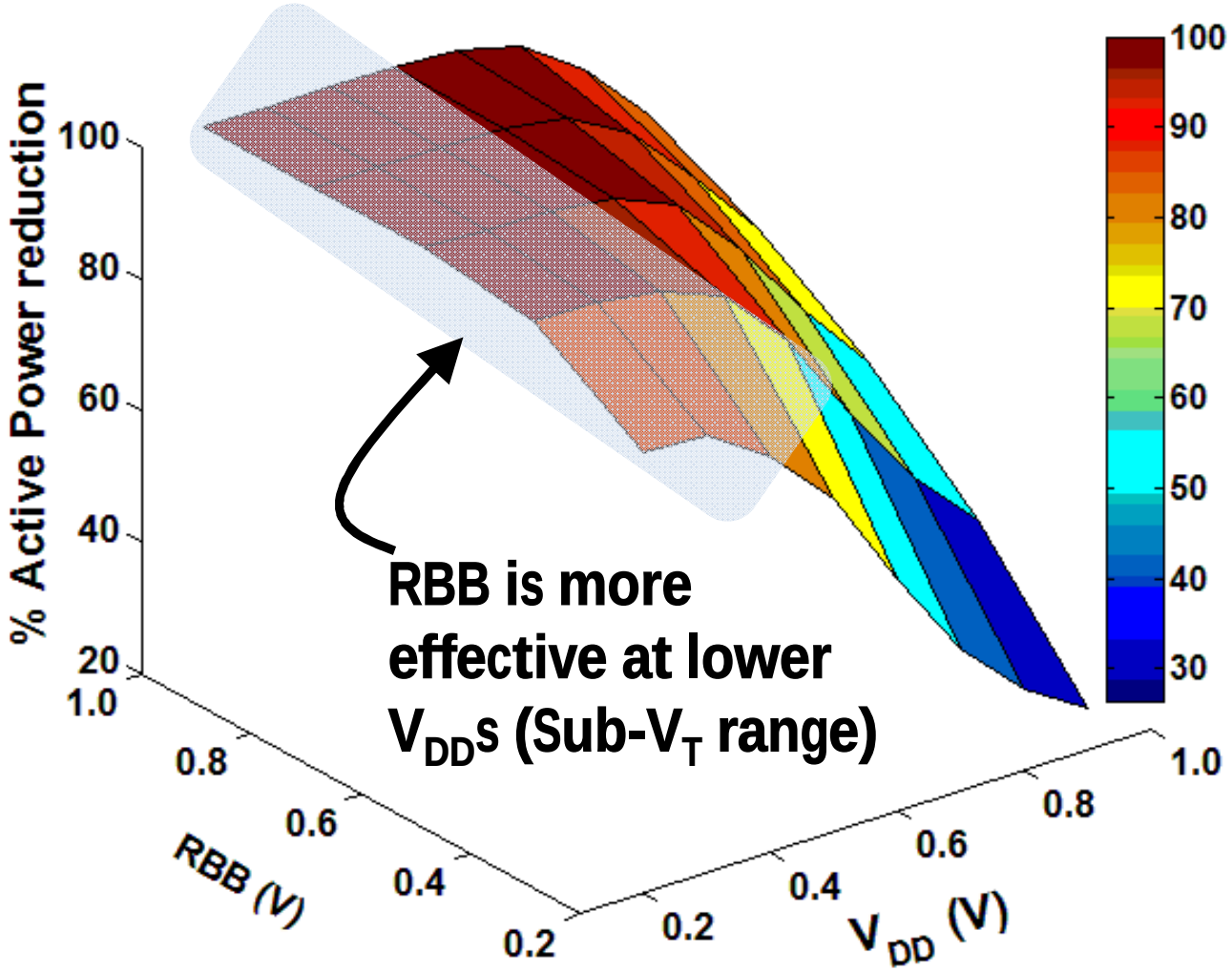


Effectiveness of RBB: Higher leakage reduction and lower I_{ON} reduction

Test-Chip Results: FIR



Test-Chip Results: RO



Comparison

	This work	[14]	[15]	[16]	[17]
Tech. (nm)	55	65	65	65	65
Cell Type	**6T**	8T	9T	14T	8T
Transistor Type	**ULL**	NA	Mixed V_T	High-V_T	Low-Power
Array V_{MIN}	**0.2V**	0.35V	0.3V	0.5V	0.4V
Energy (fJ/bit)	31.25	870	18.2	**14**	78

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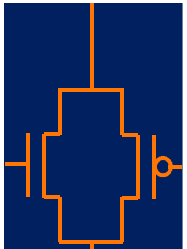
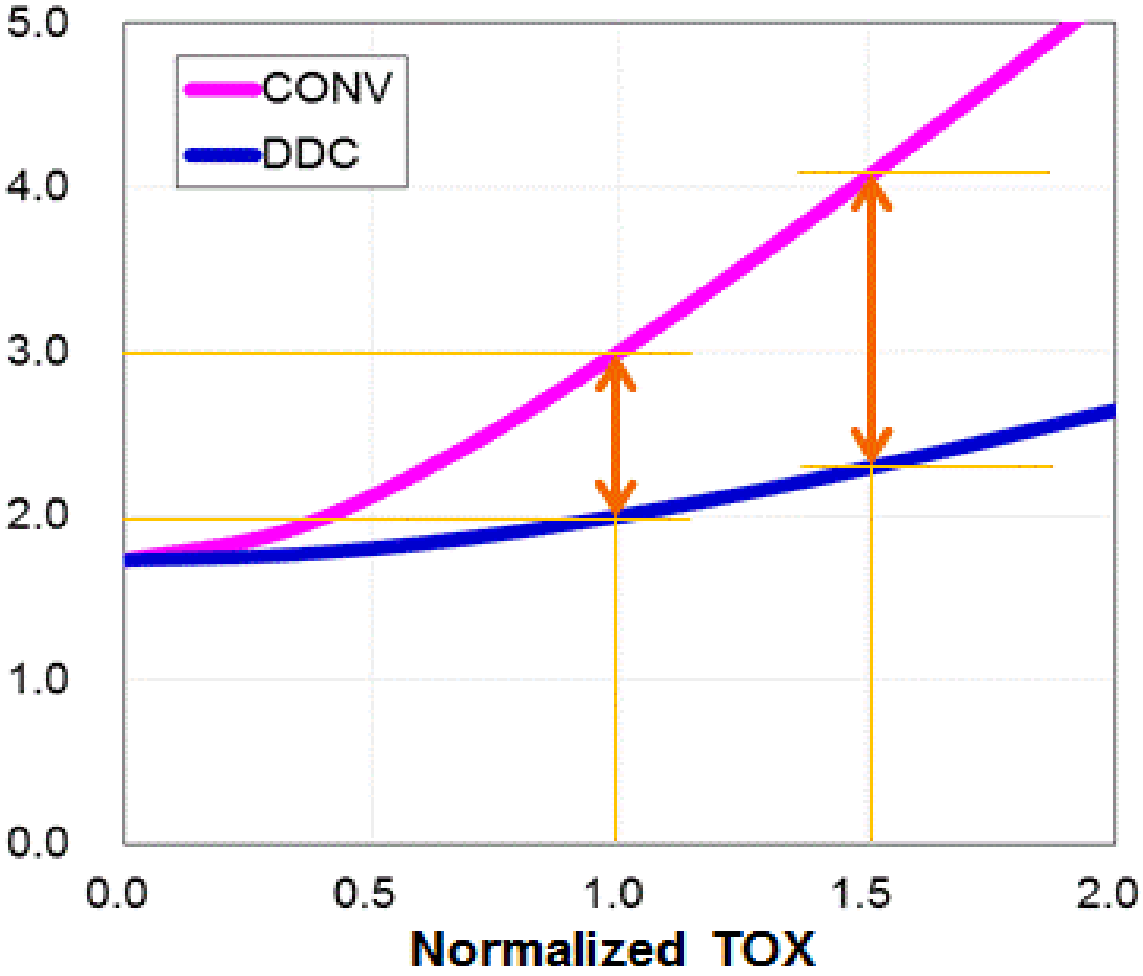


Thank you!

Sub-V_T Challenges: Increased I_{Gate}



Impact of increase in Gate-Oxide thickness (TOX) on V_T variation

Sub-threshold Optimization:

- **Reduced gate leakage** (by increasing TOX)
- **without impacting V_T variation**