Power Switch Characterization for Fine-Grained Dynamic Voltage Scaling

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***Abstract*—Dynamic voltage scaling (DVS) provides power savings for systems with varying performance requirements. One low overhead implementation of DVS uses PMOS power switches to connect DVS blocks to one of the available V_{DD} supplies. While power switches have been analyzed extensively for leakage power gating, proper design of power switches for DVS is less well understood. This paper characterizes power switches for DVS in terms of V_{DD}-switching delay and V_{DD}-switching energy. We show the impact of these switching overheads on a novel fine-grained DVS architecture and present an RC model that allows fast estimation of the overhead. Measurements of a DVS multiplier and adder on a 90nm CMOS test chip validate the model. Our model and measurements confirm that power switched DVS can provide sufficiently low overhead to give energy savings with only one clock cycle spent at a lower voltage, making this approach a flexible and enticing option for embedded portable systems.**

I. Introduction

With the proliferation of portable devices and the increase in leakage current associated with continued transistor scaling, power is quickly becoming the dominant metric in most integrated circuits. Dynamic voltage scaling (DVS) is a common technique utilized in low power design. DVS systems reduce power by lowering the frequency and voltage as allowed by performance requirements. In CMOS circuits, when voltage is reduced, energy per computation decreases quadratically, and the speed of each gate decreases roughly linearly [1-3]. The voltage to a given block can be changed by either adjusting the dc-dc converter [4] or by switching between different stable V_{DD}s using power switches [4]. Adjusting a converter or using chip-level power switches take a long time to settle to a new V_{DD}. The use of power switches enables an approach called voltage dithering [4] that uses a small set of discrete voltage and frequency pairs to approximate a broad range of energy/performance points. Voltage dithered DVS uses PMOS power switches, or headers, to connect the circuit to the lowest V_{DD} needed for proper performance [4].

The advantages of voltage dithered DVS can be amplified by distributing the power switches to local blocks on a chip [2]. This fine-grained DVS allows individual blocks to dither to the optimal energy/frequency point based on their own performance needs. Fig. 1 shows an example system set up to implement fine-grained voltage dithered DVS. Only one header connected to each block is on at a time, but blocks can connect to different V_{DD}s based on separate workloads. Turning off all of the headers for an idle block reduces leakage current. Multiple V_{DD}s (and the overhead associated with them) are already common for most chips, and our approach uses them in a more efficient manner.

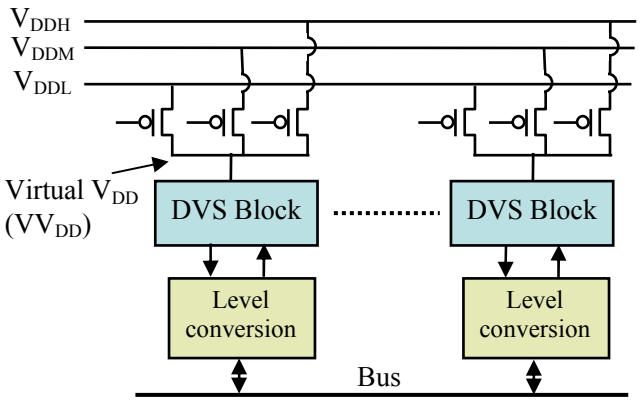

Fig. 1. Example of local fine-grained DVS using header switches and a small set of shared V_{DD}s, e.g.[2].

Previous work on header switch optimization has focused on power gating applications, for which leakage and active delay penalty considerations dominate [5-6]. The header switch puts a resistance in the V_{DD} path, resulting in a longer active delay. The linear relationship between active delay penalty and header switch size and the inverse relationship between leakage and header switch size have been established [6]. In emerging applications of local DVS to achieve fine grained power control [7], the speed at which the headers may be dithered on or off and the energy required to switch a circuit between two different V_{DD}s become important metrics. A significant V_{DD}-switching delay or energy overhead may negate the advantages of utilizing DVS and, as a result, prevent the full benefits of DVS from being exploited.

In this paper, we examine the overheads of V_{DD}-switching delay and V_{DD}-switching energy versus the size of the header devices. We present a high level RC-model for rapidly estimating the switching delay of the headers and derive equations for the V_{DD}-switching delay and V_{DD}-switching energy as a function of header size. A 90nm CMOS test chip provides measurements for V_{DD}-switching energy overhead that validate our models.

[1] Work performed while author was at the University of Virginia.

II. V_{DD}-SWITCHING METRICS

A. Motivation: Fine-Grained Sub-Block DVS

We propose an extension to the concept of local DVS that has the potential to reduce power consumption even further than standard DVS implementations. Recent research in low power design has introduced the potential of multiple energy-delay modes within a single chip. Utilizing local dithering allows the chip to achieve near-optimal low power operation [2]. This technique can be extended in larger designs, such that the voltage at which a particular portion of a chip operates is adjusted to achieve multiple operating modes [7-8]. We propose to combine this concept with local fine-grained DVS to allow voltage dithering at both a global and local block level, such that energy and performance may be traded off at many levels of granularity. Furthermore, we propose pushing DVS to an even finer granularity by implementing separate headers for some sub-blocks within a local DVS region, which we call sub-block DVS.

The data flow graph (DFG) in Fig. 2(a) is an example of an application that can use local DVS. The entire local block shares a single header switch set, so every sub-block (e.g. sub-blocks A, B, and C) must operate at the same V_{DD}, which can change based on the overall performance need. In order to take advantage of the slack in this DFG, the circuit is broken apart and a new header switch set is inserted in parallel to different sub-blocks in the local block (total area of headers can be constant), as shown in Fig. 2(b). Now sub-block C can operate at a lower voltage to take advantage of slack within the DFG. Notice that the DFG in Fig. 2(b) would be possible using standard, statically assigned multi-V_{DD}s. However, two copies of component C would be necessary to implement the DFG, since C must operate at the higher voltage in the next cycle. Sub-block DVS, on the other hand, can save area by implementing the DFG in Fig. 2(b) using a single copy of C and switching the voltages from V_{DDM} to V_{DDH} on consecutive cycles. Furthermore, the sub-block DVS approach provides more flexibility for reusing components in different modes and DFGs.

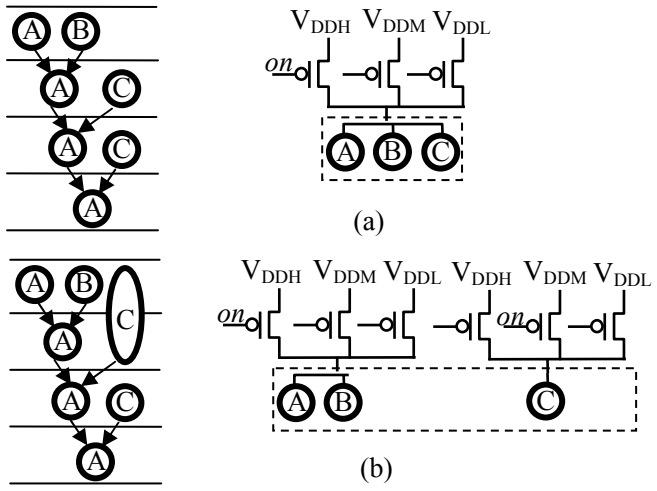

Fig. 2. DFGs for local DVS (a) and local DVS with sub-block DVS (b).

This simple example demonstrates the potential power savings of using local and sub-block DVS, since component C will trade off timing slack for lower power. However, the example also illustrates the importance of accounting for the energy and delay overhead of switching between V_{DD}s. It would not make sense in the second DFG to switch C to a lower voltage if either it takes too long to return to V_{DDH} for the following operation, or if the energy consumed by making the switch is larger than the energy saved by operating at a lower voltage. Thus, the time required to switch from one operating voltage to another operating voltage and the energy consumed by switching between two voltages are key constraints that impact the effectiveness of fine-grained DVS.

B. Header Switch Impact on V_{DD}-Switching Metrics

In DVS applications (e.g. [7-8]), logical blocks are cascaded with other circuit blocks, and each circuit block may be dithered to different energy-delay modes. In order to determine when it is practical to dither to a higher or lower voltage, the V_{DD}-switching delay overhead of dithering must be taken into account. The circuit block must be able to operate at the new voltage long enough to justify the energy and delay overheads incurred by switching voltages. This paper characterizes the impact of header sizing choices on V_{DD}-switching delay and V_{DD}-energy overhead.

The V_{DD}-switching delay depends directly on the size of the header switch and the bulk bias voltage of the PMOS switches and the devices being switched. A wider header switch has a lower drain to source resistance, resulting in faster switching. Increased bulk bias to the headers raises their V_Ts and slows down switching. An increase in the bulk bias voltage of the PMOS devices being switched results in a lower junction to substrate capacitance on each device and a lower load capacitance seen by the header switch. This results in faster switching.

On the other hand, a larger header switch will result in a larger energy overhead when dithering between voltages. A generic equation for the energy savings provided by dithering to a lower voltage for N cycles and then returning to the higher voltage is:

$$E_{saving} = E_{OPH}N - \left(E_{OPL}N + E_{Enter} + E_{Exit}\right) \quad (1)$$

where E_{OPH} and E_{OPL} are the energy per operation at the higher or the lower voltage, respectively, N is the number of operations performed, and E_{Enter} and E_{Exit} are the energy overheads of entering and exiting the low voltage mode. To justify scheduling the switch, these energy overheads must be less than the difference between the energy of N cycles at V_{DDH} and the energy of the same operations at V_{DDL}. A larger header switch has larger channel, overlap, and junction capacitances, which require more energy to charge and discharge.

Due to the larger charging and discharging energy, the faster V_{DD}-switching delay obtained by using a large header

switch comes with a higher V_{DD}-switching energy overhead. By adjusting sizing of the header switch and biasing of the circuit block in a DVS application, the delay overhead of DVS may be minimized while preventing energy overheads from overtaking the power savings of DVS.

As an example, simulation shows that a 32 bit Kogge Stone adder requires 390ps to complete an addition at 1V. Using a particular size of DVS header switches, it takes 200ps to switch the power supply of the adder from 0.7V to 1V (there is no V_{DD}-switching delay when switching to a lower voltage, since operation can continue as VV_{DD} settles downward). This corresponds to switching the adder from half its maximum operating rate to its maximum operating rate. Table 1 shows the switching delay and active delay of 16 bit, 32 bit, and 64 bit Kogge Stone adders. Clearly, the V_{DD}-switching delay of the adder is significant when compared to the active delay. As circuit block size increases, the V_{DD}-switching delay increases at a faster rate than the operating delay. The V_{DD}-switching delay increases quadratically due to the quadratic increase in the number of PMOS devices that must be switched as adder size increases. The operating delay of the Kogge Stone adder increases at a slower logarithmic rate due to the carry lookahead structure. Table 2 shows the V_{DD}-switching energy and energy per addition of the same Kogge Stone adders. For the same reasons stated above, the V_{DD}-switching energy increases quadratically, while the energy per addition increases linearly. In both situations, the switching overheads become more significant as the size of the circuit is increased. This means either that the area overhead of headers for large blocks must go up as a percentage of total area, or a longer V_{DD}-switching delay must be tolerated by stalling operations when switching back to higher voltages.

Table 1. V_{DD}-switching from half-rate (0.7V) to full-rate (1V) and active delay at full-rate (1V) versus adder size.

Adder Size (bits)	**V_{DD}-Switching Delay (ps)**	**Active Delay (ps)**
16	160	251
32	200	404
64	868	447

Table 2. VDD-switching energy from 0.7V to 1V and energy per addition at 1V versus adder size.

Adder Size (bits)	**V_{DD}-Switching Energy (pJ)**	**Active Energy (pJ)**
16	0.08	0.20
32	0.14	0.50
64	1.77	0.88

III. HEADER SWITCH RC MODEL

We can derive a simple RC model for the header switches from the basic structure of the transistors. Fig. 3(a) shows a two header system with parasitic capacitances included. We model the circuit block as a constant load capacitance C_L (including wiring cap at VV_{DD}) for V_{DD}-delay (e.g. Fig. 3(b)) and V_{DD}-energy models. While the capacitance looking into the source terminals of PMOS devices inside individual gates in the DVS block will vary in a data dependent fashion by up to 50%, our simulations show that this variation drops below 10 percent due to averaging effects when the circuit comprises several gates or more. The headers themselves are modeled as having channel capacitances C_{GS}, C_{GD}, overlap capacitances C_{GSO}, C_{GDO}, junction capacitances C_{SB}, C_{DB}, and a source to drain resistance R_{SD}. Since the header is operating in the triode region when it is on, the channel capacitance is distributed evenly between source and drain, resulting in:

$$C_{GS} = C_{GD} = \frac{C_{ox}WL}{2} \tag{2}$$

where W is the total width of the header, L is the length of the header device, and C_{ox} is the oxide capacitance per unit area. The overlap capacitances are given by:

$$C_{GSO} = C_{GDO} = C_O W \tag{3}$$

where C_O the overlap capacitance per unit transistor width. The junction capacitances are approximated for folded layout as:

$$C_{DB} = C_{SB} = C_j L_S W + C_{jsw}(2L_S) \tag{4}$$

where C_j is the bottom plate junction capacitance per unit area, C_{jsw} is the sidewall junction capacitance per unit area, and L_S is the sidewall length. The source to drain resistance, neglecting channel length modulation, is given by:

$$R_{DS} = \frac{1}{\left|\mu_p\right| C_{ox}\left(\frac{W}{L}\right)\left(\left|V_{GS}\right| - \left|V_{tp}\right| - \frac{\left|V_{DS}\right|}{2}\right)} \tag{5}$$

The parallel capacitances in the model above add, and Fig. 3(b) shows the equivalent RC model used for obtaining V_{DD}-switching delay. We can derive the switching time constant through the RC tree (for 2 headers) as:

$$\tau = R_{DS} \cdot (2C_{GDO} + 2C_{GD} + 2C_{DB} + C_L) \tag{6}$$

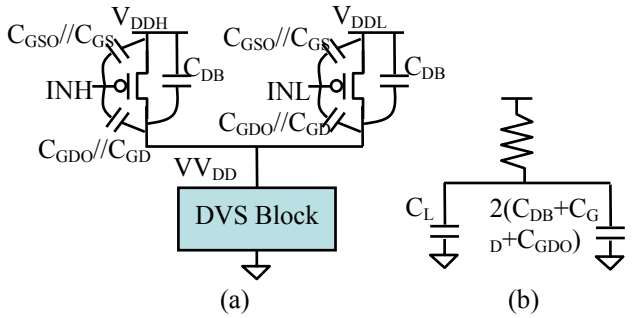

Fig. 3. Two header switch system with parasitic capacitances shown (a) and RC model of header switches and circuit block used for V_{DD}-switching delay (b).

Substituting equations (2) through (5) in the expression above and noting that V_{DS} of the on header is nearly zero, the switching time constant is given in terms of header switch width by:

$$\tau = \frac{2C_o W + C_{ox} WL + 2\left[C_j L_S W + 2C_{jsw} L_S\right] + C_L}{\left|\mu_p\right| C_{ox}\left(\frac{W}{L}\right)\left(\left|V_{GS}\right| - \left|V_{tp}\right| - \frac{\left|V_{DS}\right|}{2}\right)} \tag{7}$$

The time constant consists of a term that does not depend on header width and a term that varies inversely with header width. The header width dependent term arises due to the circuit block load capacitance and the junction capacitance of the header switch. As the width of the header switch increases, the drain to source resistance decreases and the V_{DD}-switching delay is reduced. Self loading by the header switches limits the maximum V_{DD}-switching speed.

The time constant may be used to find the actual V_{DD}-switching delay by applying the RC delay equation. The V_{DD}-switching delay is defined as the time required to switch the virtual V_{DD} node to the 50% point between the low voltage and the high voltage. The delay is thus given by:

$$T_{Switch} = -\ln\left(1 - \frac{V_H + V_L}{2V_L}\right)\tau \tag{8}$$

where V_H is the high voltage, V_L is the low voltage, and T_{Switch} is the V_{DD}-switching delay. Fig. 4 shows the V_{DD}-switching delay from 0.7V to 1.0V for an adder with two headers as a function of header switch size given by both simulation and equations (6) and (8) for a 90nm technology. The header switch size is given as a percentage of the total PMOS area of the adder. The delay given by (8) follows the same trend as the simulated delay but slightly underestimates the simulated delay, most likely due to inaccuracies in the estimates of header parasitic capacitances.

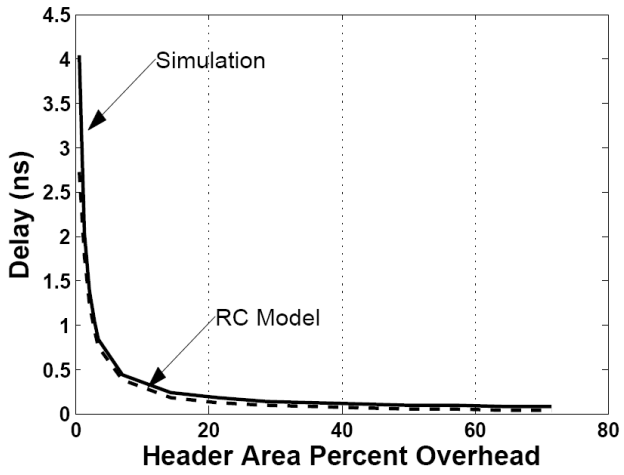

Fig. 4. RC model of V_{DD}-switching delay (8) and simulated V_{DD}-switching delay for a 32 bit adder switching from 0.7V to 1.0V vs. the area of the header as a percentage of total PMOS area in the adder.

IV. V_{DD}-Switching Energy Requirement

The energy overhead of V_{DD}-switching may be obtained by determining the total power dissipated by charging and discharging capacitances in the model during a high to low and then low to high switching transition. A capacitor discharging to V_{cap}=0V dissipates all of the energy initially stored on it, which is $0.5CV_{cap}^2$. Half of the energy drawn from the supply to charge a capacitor is likewise dissipated. The amount of energy dissipated by charging and discharging each capacitor shown in Fig. 3(a), is taken into account. The total energy dissipated, the sum of E_{Enter} and E_{Exit}, is given by:

$$E_T = (V_H - V_L)^2\left[C_L + 2C_{DB} + 2C_{GD}\right] + V_H^2\left(2C_{GD} + 2C_{GS}\right) \tag{9}$$

We assume that the high and low inputs (IN_H and IN_L) fully change before the virtual V_{DD} node changes, due to the significantly higher load capacitance present at virtual V_{DD}. This assumption makes the first order model simpler, but will neglect the impact of the Miller effect on the C_{GD} capacitors that will occur if the transitions partially overlap, leading to an underestimate of total energy. In equation (9), each capacitive term increases with increased header width. As a result, larger header switches consume more overhead energy during switching.

Fig. 5 shows the normalized V_{DD}-switching delay overhead versus energy overhead for a 32bit Kogge Stone adder in 90nm with two header switches. The V_{DD}-switching delay points on the curve are the same delays as in Fig. 4, so, for example, the lower right-hand point in Fig. 5 maps to the upper left-hand point in Fig.4. V_H and V_L are 1.0V and 0.7V, respectively.

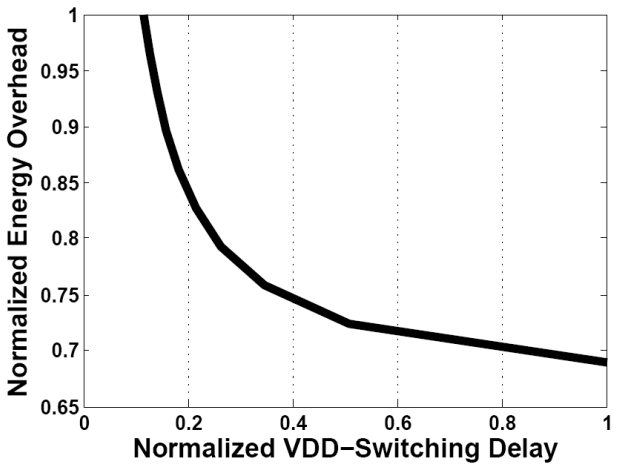

Fig. 5. Energy and delay overheads of DVS for a 32 bit adder.

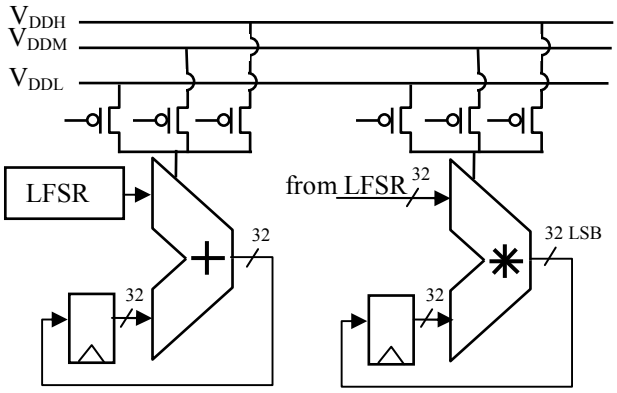

Fig. 6. Block diagram of the test chip circuit. Header switches are individually controllable from off-chip. The adder is a 32b Kogge Stone adder, and the multiplier is a 32b Baugh Wooley multiplier. Only the 32 least significant bits of the multiplier output are used in the loop.

V. Test Chip Implementation and Results

A test chip was implemented in 90 nm bulk CMOS to measure the switching overheads of fine-grained and sub-block DVS. Fig. 6 shows that the test chip contains a scan-chain connected 32 bit Kogge Stone adder, a 32 bit Baugh Wooley multiplier, and linear feedback shift register (LFSR). Data is initially scanned into an adder register, multiplier register, and LFSR. On each clock cycle, the contents of the adder register and the LFSR are added by the adder, and the result is written to the adder register. Likewise, the contents of the multiplier register and LFSR are multiplied by the multiplier and the lower 32 bits of the result are written to the multiplier register. The virtual V_{DD} rail of the adder and multiplier are each connected to three supply voltages, V_{DDH}, V_{DDM}, and V_{DDL}, via power switches. Note that the fine-grained placement of header switches requires us to replicate the section of the power supply grid between the supply pin and the header switch so that each V_{DD} rail supplies each set of headers. This creates routing area overhead, although the more dense power supply grid near the circuits (VV_{DD}) does not need to be replicated. To characterize the energy of the fabricated circuit compared to simulation and our model, we measured the active energy and V_{DD}-switching overhead energy of both the adder and multiplier.

The header switches were sized to have 15% area overhead compared to the total PMOS area of a 32 bit adder, which is a point that balances the increased V_{DD}-switching energy incurred by a larger header switch with the decreased V_{DD}-switching delay a smaller header switch provides, i.e. near the knee of the curve in Fig. 5. Simulation showed that further increases in the size of the header switches did not significantly affect switching delay due to self loading by the header switches. However, further increases in header size would adversely affect the switching energy.

To measure the active energy of the adder and multiplier, we shift an initial value into the LFSR and the component register, turn on one header connected to a variable V_{DD} rail for the component under test, and run the system. The selected component then executes at the specified clock frequency. As the voltage supply is varied from 1.0V to 0.5V, the current drawn by the voltage supply is measured to determine the average current drawn over a large number of computations (and average energy consumed) by each component.

Since we assume that the DVS operations will occur primarily at frequencies near the maximum operating rate, we primarily want to measure the switching energy per operation of the adder and multiplier. However, at lower frequencies, leakage currents can obscure this value by contributing substantially to, or even dominating total energy per operation. Fig. 7 shows the total measured energy per operation versus frequency at 1V for both the adder and the multiplier. At lower frequencies, leakage currents integrate to dominate the total measured energy. As frequency increases, the measured energy per operation levels off. This occurs when the active energy, which is independent of frequency, dominates the total energy. We used an average of the measurements of total energy at the

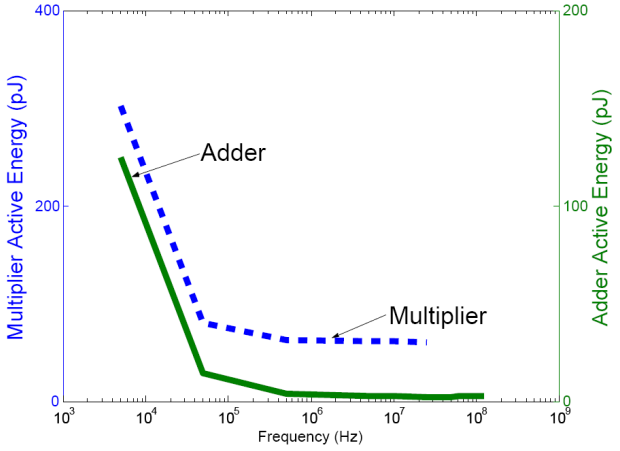

Fig. 7. Measured total energy per operation for the adder and multiplier versus frequency at 1V. Leakage energy dominates at lower frequencies. Active energy/op numbers are selected from the higher frequencies, where the frequency independence shows that active energy dominates.

higher frequencies where active energy dominates to isolate the active energy per operation of an addition and multiplication. Fig. 8 shows the measured active energy of the adder, and Fig. 9 shows the measured active energy of the multiplier as the operating voltage is varied on chip.

The V_{DD}-switching energy overheads are measured by connecting one header to a high supply voltage of 1V and connecting another header to low supply voltages ranging from 0.9V to 0.5V. The two headers are then dithered on and off without any active operations occurring and the resulting current through the high and low supply voltages are measured. The measurements include the current used to drive the logic that switches the headers and the current used to charge up VV_{DD}. The V_{DD}-switching energy is then given by:

$$E_{switch} = \frac{\left(I_{DDH}V_{DDH} + I_{DDL}V_{DDL}\right)}{2} T_{switch} - E_{active} \qquad (10)$$

where E_{active} is the active energy per operation, I_{DDH} is the average current through the high supply, V_{DDH} is the high voltage (maintained at 1 V), I_{DDL} is the average current through the low supply, V_{DDL} is the low voltage (varied from 0.5V to 0.9V), and T_{switch} is the period between consecutive switches. Again, to account for the dominance of leakage current through the circuit when switching at low frequencies, the switching energy of a multiplier is plotted as a function of switching frequency on a semilog plot in Fig. 10. The figure shows that the switching energy begins to level off at higher switching frequencies, indicating that the leakage energy no longer dominates. The figure also indicates that, at the maximum frequency with which our measurement equipment allows us to switch the headers, leakage is still non-negligible (e.g. the curve is not totally flat). Thus, the numbers that we present later in this section slightly overestimate the energy overhead for a V_{DD} switch, since they include some of the leakage energy that would be consumed with or without the switch happening.

Fig. 11 and Fig. 12 show the measured V_{DD}-switching energy of the adder and multiplier, respectively, along with the V_{DD}-switching energy given by simulation and given by the capacitive model. The model used in this plot is adjusted from that given in Equation (6) to account for the presence of capacitance from three headers per component.

Active energy decreases as the supply voltage is lowered, but the V_{DD}-switching energy increases when switching to a lower supply voltage, as expected. Differences between the energy given by the model and the energy given by simulation and measurement are due to the approximations used in determining the load capacitance used in the model. Differences between the simulated energy and measured energy are due to the inability of the simulation to precisely account for parasitics present in layout.

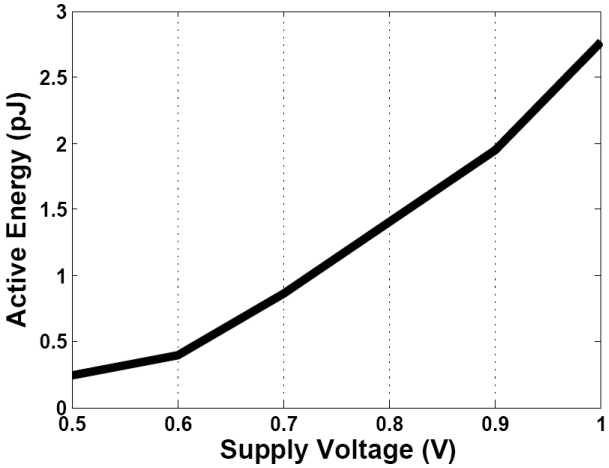

Fig. 8. Measured active energy per addition from the test chip.

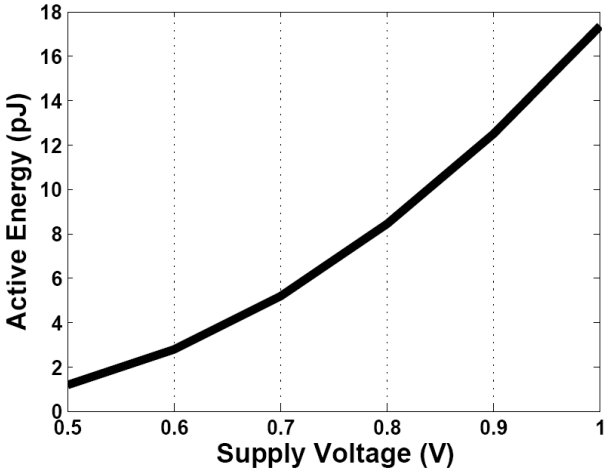

Fig. 9. Measured active energy per multiplication from the test chip.

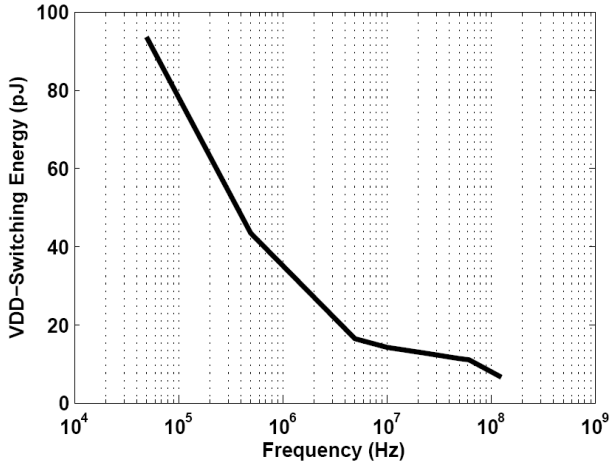

Fig. 10. Semi-log plot showing that the measured V_{DD}-switching energy of a multiplier levels off at higher frequencies where leakage contributions become negligible relative to actual switching energy.

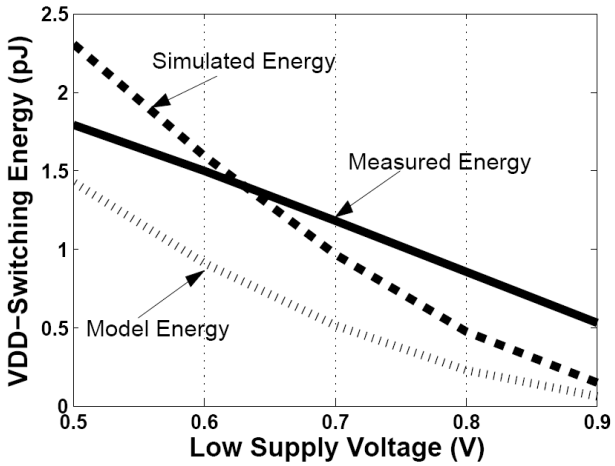

Fig. 11. Measured adder V_{DD}-switching energy.

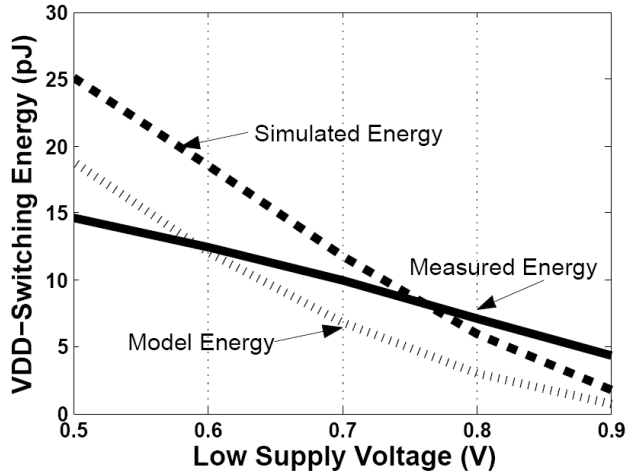

Fig. 12. Measured multiplier V_{DD}-switching energy.

The number of cycles required to break even and to justify switching to a lower voltage from an energy standpoint is:

$$N_{BE} = \frac{\left(E_{High} - E_{Low}\right)}{E_{switch}} \tag{11}$$

where E_{High} is the energy per operation at V_{DDH} and E_{Low} is the energy per operation at V_{DDL}. The number of break even cycles required to dither to various voltages, based on measured data, is shown for both the adder and the multiplier in Table 3. For both the adder and the multiplier, the number of break even cycles required is less than one for all switching scenarios, indicating that performing at least one operation at the lower voltage will justify the cost incurred by V_{DD}-switching energy. This result, based on measurements of V_{DD}-switching overhead, shows that fine-grained DVS applications, such as represented by the DFG in Fig. 2, can take advantage of extremely short changes in workload or brief regions of slack in the operating schedule.

Table 3. Adder and multiplier break even cycles using measured data.

Low Supply Voltage	Adder Break Even Cycles	Multiplier Break Even Cycles
0.9	0.689	0.436
0.8	0.579	0.408
0.7	0.607	0.263
0.6	0.721	0.328
0.5	0.826	0.359

VI. Conclusion

We have proposed an extension of fine-grained DVS by implementing DVS with local header switches that are inserted down to the sub-block level. Characterization of the power switches allows us to estimate the impact of header size on V_{DD}-switching delay and V_{DD}-switching energy overheads for DVS applications. We have presented a first order RC model, based on analysis of the header switches, that allows a good estimation of the overhead of fine-grained DVS switches. The model clarifies the tradeoffs for sizing headers designed for switching power supply rails in fine-grained DVS applications. A test chip fabricated in 90nm silicon provides us with experimental switching overhead measurements. The overhead measurements confirm that the models we derived provide adequate estimation of the energy overhead, and they show that fine-grained DVS can provide decreases in energy consumption by taking advantage of switching to lower V_{DD}s for as short as one arithmetic operation.

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