Modeling and Sizing for Minimum Energy Operation in Subthreshold Circuits

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***Abstract*—This paper examines energy minimization for circuits operating in the subthreshold region. Subthreshold operation is emerging as an energy-saving approach to many energy-constrained applications where processor speed is less important. In this paper, we solve equations for total energy to provide an analytical solution for the optimum $V_{\rm DD}$ and $V_{\rm T}$ to minimize energy for a given frequency in subthreshold operation. We show the dependence of the optimum $V_{\rm DD}$ for a given technology on design characteristics and operating conditions. This paper also examines the effect of sizing on energy consumption for subthreshold circuits. We show that minimum sized devices are theoretically optimal for reducing energy. A fabricated 0.18-μm test chip is used to compare normal sizing and sizing to minimize operational $V_{\rm DD}$ and to verify the energy models. Measurements show that existing standard cell libraries offer a good solution for minimizing energy in subthreshold circuits.**

***Index Terms*—Energy model, low voltage operation, minimum energy point, subthreshold logic.**

I. Introduction

THE INCREASING attention on power consumption in circuit design has motivated a significant investigation of the optimum design for minimizing energy or power for a given performance constraint. Almost all of these efforts have targeted high-performance strong inversion operation. Emerging applications such as distributed sensor networks or medical applications have low energy as the primary concern instead of performance, with the eventual goal of harvesting energy from the environment (e.g., [1]). Subthreshold operation is ideal for this class of applications because it allows minimum energy operation for low-performance situations [2], [3]. This paper analyzes energy minimization for circuits operating in the subthreshold region. We develop a subthreshold energy model for determining the optimum supply voltage ($V_{\rm DD}$) for a fixed threshold voltage ($V_{\rm T}$) when minimizing energy is the primary concern. The subthreshold energy model shows the dependence of the minimum energy point on design characteristics and operating conditions. It also provides an analytical solution for $V_{\rm DD}$ and $V_{\rm T}$ to minimize energy for a given frequency in the subthreshold region. This paper also examines the effect of device sizing on minimum energy operation. After considering theoretically optimal sizing, we evaluate standard cell designs for minimum energy operation. A fabricated 0.18-μm test chip provides measurements for analysis.

Many previous works address optimal power or energy operation for a given performance constraint using various metrics. Early solutions for minimizing the energy-delay product (EDP) [3] are extended to account for process variation [4] and buffering options [5], and they show that EDP is minimized in superthreshold operation. Analytical expressions for the optimum ($V_{\rm DD}$, $V_{\rm T}$) point to minimize power at a given performance are shown for transregional models based on fitted [6] or physical [7] parameters. Measurements of a test chip with adaptive $V_{\rm DD}$ and adaptive body bias demonstrate the minimum power point for a given performance, but they also show how forward-biased diode currents (from body biasing) can make the theoretical optimum unreachable in practice [8]. Derivations of the sensitivities of energy and delay to different parameters support a methodology for building optimum energy circuits [9]. Taken together, these and other works give thorough attention to power optimization for strong inversion circuits. Optimizing subthreshold circuits has received less attention.

Subthreshold operation (where $V_{\rm T} > V_{\rm DD}$) is currently used for some low-power applications such as watches [10] and hearing aids [11]. Emerging ultralow-power applications such as distributed sensor networks are a natural fit with subthreshold circuits. Special circuit techniques for improving robustness in deep subthreshold have been explored [12], [13]. Examining the energy-delay contours for digital circuits over $V_{\rm DD}$ and $V_{\rm T}$ shows that minimum energy operation occurs in the subthreshold operation regime for low-to-medium performance systems, and the optimum point changes depending on activity factor and threshold variation [2].

II. Modeling for Subthreshold Operation

This section develops the models for subthreshold energy analysis. None of the strong inversion optimization work accounts for gate leakage even though gate leakage contributes significantly to total leakage in deep-submicron technologies. In the subthreshold region, however, gate current is negligible relative to subthreshold current because it rolls off much faster with $V_{\rm DD}$. Other leakage components such as gate-induced drain leakage (GIDL) and pn-junction leakage are also negligible in sub-threshold. Thus, the following analysis justifiably equates total current to subthreshold current for $V_{\rm DD}$ in the subthreshold region.

The basic equation for modeling subthreshold current and total off current is

$$I_{\rm SUB} = I_o e^{(V_{\rm GS}-V_{\rm T})/nV_{\rm th}} \quad I_o = \mu_o C_{\rm ox} \frac{W}{L} (n-1) V_{\rm th}^2 \quad (1)$$

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where n is the subthreshold slope factor ($1 + C_d/C_{\rm ox}$), and $V_{\rm th}$ is kT/q. The model we develop uses fitting parameters that are normalized to a characteristic inverter in the technology of interest. Equation (2) shows the propagation delay of a characteristic inverter with output capacitance C_g in subthreshold:

$$t_d = \frac{KC_gV_{\rm DD}}{I_{o,g}e^{(V_{\rm GS}-V_{{\rm T},g})/nV_{\rm th}}} \tag{2}$$

where K is a delay fitting parameter. The expression for current in the denominator of (2) models the *on* current of the characteristic inverter, so it accounts for transitions through both nMOS and pMOS devices. Unless the pMOS and nMOS are perfectly symmetrical, the terms $I_{o,g}$ and $V_{{\rm T},g}$ are fitted parameters that do not correspond exactly with the MOSFET parameters of the same name. Operational frequency is simply

$$f = \frac{1}{t_dL_{\rm DP}} \tag{3}$$

where $L_{\rm DP}$ is the depth of the critical path in characteristic inverter delays. Dynamic ($E_{\rm DYN}$), leakage (E_L), and total energy ($E_{\rm T}$) per cycle are expressed in (4)–(6) [14], assuming rail-to-rail swing ($V_{\rm GS} = V_{\rm DD}$ for *on* current).

$$E_{\rm DYN} = C_{\rm eff}V_{\rm DD}^2 \tag{4}$$

$$\begin{aligned} E_L &= W_{\rm eff}I_{o,g}e^{-V_{{\rm T},g}/nV_{\rm th}}t_dL_{\rm DP}V_{\rm DD} \\ &= W_{\rm eff}KC_gL_{\rm DP}V_{\rm DD}^2e^{-V_{\rm DD}/nV_{\rm th}} \end{aligned} \tag{5}$$

$$\begin{aligned} E_T &= E_{\rm DYN} + E_L \\ &= V_{\rm DD}^2\left(C_{\rm eff} + W_{\rm eff}KC_gL_{\rm DP}e^{-V_{\rm DD}/nV_{\rm th}}\right). \end{aligned} \tag{6}$$

Equations (4)–(6) extend the expressions for current and delay of an inverter to arbitrary larger circuits. This extension sacrifices accuracy for simplicity since the fitted parameters cannot account for all of the details of every circuit. Thus, $C_{\rm eff}$ is the average effective switched capacitance of the entire circuit, including the average activity factor over all of its nodes, short circuit current, glitching effects, etc. To calibrate the model, $C_{\rm eff}$ is estimated by measuring average supply current for an average simulation and solving $C_{\rm eff} = I_{\rm avg}/(fV_{\rm DD})$. $\rm W_{eff}$ estimates the average total width, relative to the characteristic inverter, that contributes to leakage current. $\rm W_{eff}$ is determined by simulating the circuit's steady-state leakage current and normalizing to the characteristic inverter. Since $\rm W_{eff}$ is a function of circuit state, averaging the circuit leakage current for simulations over many states improves the total leakage estimate. Simulating to exercise the circuit's critical path provides the logic depth, $L_{\rm DP}$. Solving this set of equations provides a good estimate of the optimum for the average case and shows how the optimum point depends on the major parameters.

Differentiating (6) and equating to 0 allows us to solve for $V_{\rm DDopt}$

$$\begin{aligned} \frac{\partial E_T}{\partial V_{\rm DD}} &= 2C_{\rm eff}V_{\rm DD} + 2W_{\rm eff}L_{\rm DP}KC_gV_{\rm DD}e^{-V_{\rm DD}/nV_{\rm th}} \\ &\quad + \frac{-W_{\rm eff}L_{\rm DP}KC_gV_{\rm DD}^2}{nV_{\rm th}}e^{-V_{\rm DD}/nV_{\rm th}} = 0. \end{aligned} \tag{7}$$

The analytical solution for $V_{\rm DDopt}$ is given in (8), with the constraint in (9):

$$V_{\rm DDopt} = nV_{\rm th}(2 - {\rm lambert}W(\beta)) \tag{8}$$

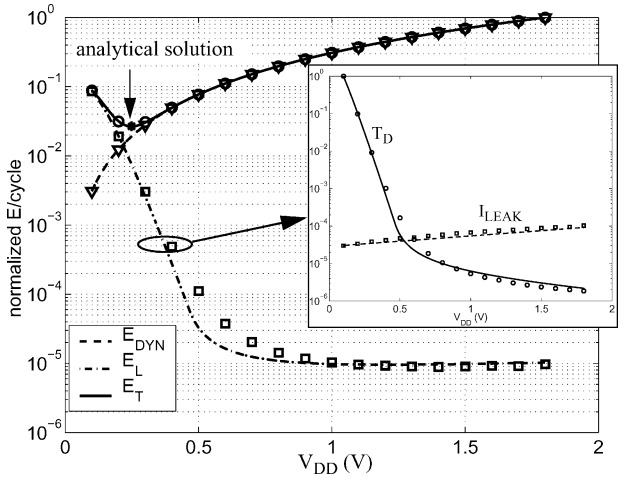

Fig. 1. Model versus simulation of FIR filter showing minimum energy point and contribution of active and leakage energy. Inset shows $I_{\rm LEAK}$ and T_D effect on E_L. Markers are simulation values, lines are model [7]. Analytical solution from (8) and (6) is shown.

$$\beta = \frac{-2C_{\rm eff}}{W_{\rm eff}L_{\rm DP}KC_g}e^2 > -e^{-1}. \tag{9}$$

The Lambert W function, $W = {\rm lambert}W(x)$, gives the solution to the equation $We^W = x$, just as $W = \ln x$ is the solution to $e^W = x$ [15]. Now, substituting (2) into (3) allows us to solve for the $V_{\rm Topt}$ to achieve a given f

$$V_{\rm Topt} = V_{\rm DDopt} - nV_{\rm th}\ln\left(\frac{fKC_gL_{\rm DP}V_{\rm DDopt}}{I_{o,g}}\right). \tag{10}$$

If the argument to the natural log in (10) exceeds 1, then the assumption of subthreshold operation no longer holds because $V_{\rm Topt} < V_{\rm DD}$. This constraint shows that there is a maximum achievable frequency for a given circuit in the subthreshold region. Equations (8) and (10) give the optimum supply voltage and threshold voltage for a subthreshold circuit consuming the minimum energy for a given frequency. Some ultralow-power applications, such as energy scavenging sensor nodes, might consider minimizing energy to be more important than any performance requirement. Assuming a standard technology where $V_{\rm T}$ is fixed (i.e., no triple wells for body biasing), the problem becomes finding the optimum $V_{\rm DD}$ to minimize energy per operation for a given design. The optimum $V_{\rm DD}$ for minimizing energy per cycle in this scenario still is given by (8), and the optimum frequency is given by (3) at $V_{\rm DDopt}$.

Fig. 1 shows the energy profile of an 8-bit, 8-tap parallel programmable FIR filter versus $V_{\rm DD}$. The contributions of active and leakage energy are both shown. The lines on the plot show the results of numerical equations using a transregional current model [6], and the markers show the simulation values. The analytical solution (small star) matches the numerical model and simulations with less than 0.1% error. The optimum point is $V_{\rm DDopt} = 250$ mV with a frequency of 30 kHz. Equation (8) provided the optimum $V_{\rm DD}$ for the analytical solution, and substituting this value into (6) gave the total energy. The inset in Fig. 1 shows how the delay (T_D) and current ($I_{\rm LEAK}$) components of leakage energy per cycle (E_L) vary with supply voltage. As $V_{\rm DD}$ reduces, the current decreases due to the DIBL effect,

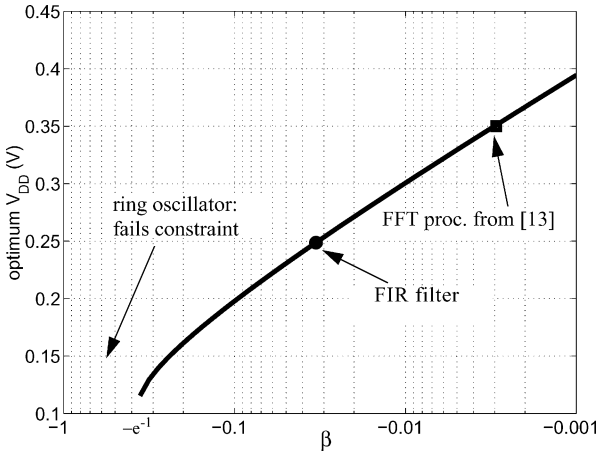

Fig. 2. $V_{\rm DD}$ optimum calculated with (8). β for ring oscillator ($L_{\rm DP} = 21$) fails constraint. β for 8×8 parallel FIR filter and scalable FFT processor also shown.

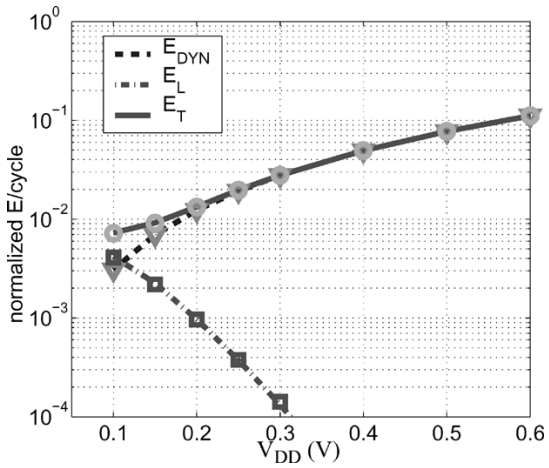

Fig. 3. Energy per operation versus $V_{\rm DD}$ for a 21-stage ring oscillator has no minimum point. Markers show simulation data and lines show equations.

but the delay increases exponentially in the subthreshold region, leading to the increase in subthreshold E_L.

Equation (8) shows that the optimum $V_{\rm DD}$ value is independent of frequency and $V_{\rm T}$. Instead, it is set by the relative significance of dynamic and leakage energy components as expressed in (9). E_L increases compared to the characteristic inverter in two ways. First, the ratio of $C_{\rm eff}/{\rm W}_{\rm eff}$ decreases, indicating that a greater fraction of the total width is idle and thereby drawing static current without switching. Second, $L_{\rm DP}$ can increase. The larger resulting period gives more time for leakage currents to integrate, raising E_L. Fig. 2 shows the optimum $V_{\rm DD}$ values versus β for three examples. An FFT processor [13] and the FIR filter previously described have $V_{\rm DDopt}$ at 350 and 250 mV, respectively. The figure shows that a ring oscillator fails to meet the constraint. To see why, consider a single inverter with activity factor of one; ${\rm W}_{\rm eff}$ and $L_{\rm DP}$ equal one, $C_{\rm eff}$ is close to C_g, and β does not meet the constraint in (9). Mathematically, this means that the derivative of $E_{\rm T}$ never equals zero. Physically, the leakage component for the single inverter or ring oscillator with high activity remains insignificant compared to dynamic energy over all supply voltages, as shown in Fig. 3. The true

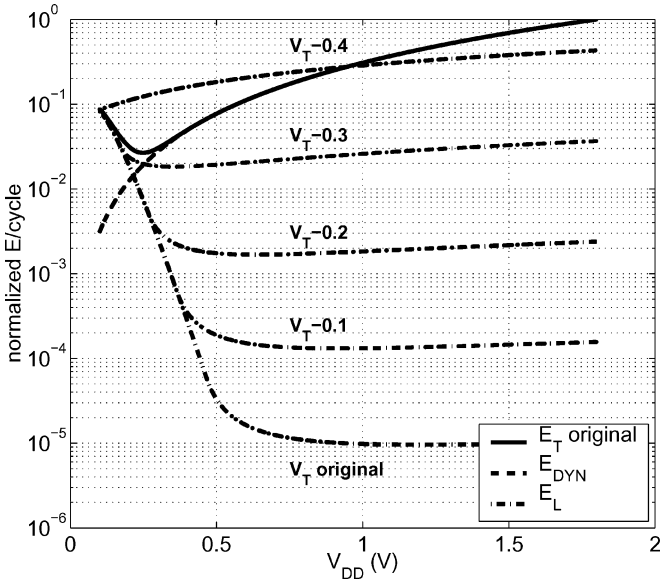

Fig. 4. Lowering $V_{\rm T}$ does not improve the energy per operation in the subthreshold region.

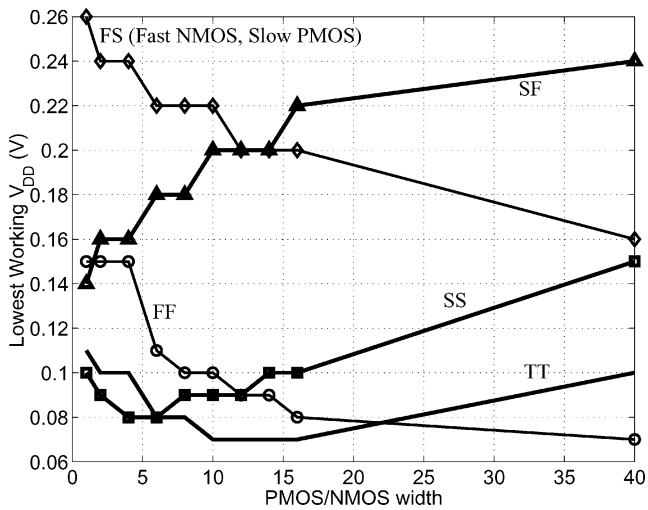

Fig. 5. Minimum achievable voltage retaining 10%–90% output swing for 0.18-μm ring oscillator across process corners (simulation).

optimum $V_{\rm DD}$ in this case is the lowest voltage for which the circuit functions. Circuits with higher relative leakage energy, like the FIR filter or FFT processor, have less negative β and thus higher optimum $V_{\rm DD}$.

Fig. 4 shows theoretically why the optimum $V_{\rm DD}$ is independent of $V_{\rm T}$. As $V_{\rm T}$ decreases in the figure, the subthreshold current increases exponentially as shown by the rise in E_L at super$V_{\rm T}$ voltages. The subthreshold *on* current also increases exponentially, so T_D decreases exponentially in subthreshold and offsets the rise in $I_{\rm LEAK}$ such that E_L does not change in the subthreshold region. When $V_{\rm T}$ decreases too far, then $V_{\rm DDopt} > V_{\rm T}$ so the subthreshold equations become invalid. The figure shows that E_L physically exceeds $E_{\rm DYN}$ for extremely low $V_{\rm T}$ in this filter example. Of course, the advantage to lowering $V_{\rm T}$ is increased performance in the subthreshold region for the same energy per operation.

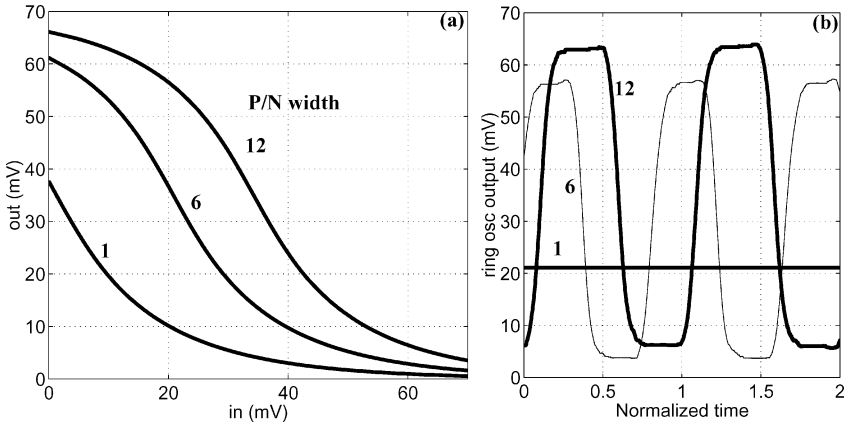

Fig. 6. (a) VTC and (b) 9-stage ring oscillator output at the minimum $V_{\rm DD}$ for the typical corner (simulation). PMOS/NMOS width ratio of 12 minimizes operational $V_{\rm DD}$ but increases energy consumption.

III. Sizing and Minimum Operating Voltage

Transistor sizing impacts the functionality of CMOS circuits at low supply voltages. Minimum $V_{\rm DD}$ operation occurs when the pMOS and nMOS devices have the same current (e.g., [16]). Previous efforts have explored well biasing to match the device currents for minimum voltage operation of ring oscillators [12]. Sizing can create the same symmetry in device current. Fig. 5 shows the minimum voltage for which a ring oscillator maintains 10%–90% voltage swing. The optimum pMOS/nMOS width across all process corners for this 0.18-μm technology is 12, because this size matches the subthreshold currents through the two types of devices. Fig. 6(a) shows the voltage transfer characteristics (VTCs) at the minimum $V_{\rm DD}$ of 70 mV for several $\rm P/N$ ratios. The gain is somewhat degraded, but the curve with $\rm P/N$ of 12 is symmetrical and shows good noise margins. Fig. 6(b) shows the output of a 9-stage ring oscillator at the minimum voltage for the same sizes.

Sizing according to this ratio allows for operation at lower $V_{\rm DD}$ but increases the energy consumed for a given $V_{\rm DD}$ (6). The energy savings from lowering $V_{\rm DD}$ are at best proportional to $V_{\rm DD}^2$ if leakage is still negligible. Fig. 5 shows that changing the $\rm P/N$ ratio in an inverter only decreases the minimum supply voltage by 60 mV, producing best case energy savings of $0.20^2/0.26^2 = 0.6\times$ due to voltage reduction. This improvement is not worthwhile if all pMOS devices are increased in size by $12\times$. Thus, minimum sized devices are theoretically optimal for reducing energy per operation when accounting for the impact of sizing on voltage and energy consumed [17]. Process variation in deep-submicron processes imposes one restriction to applying this rule blanketly. The sigma for $V_{\rm T}$ variation due to random doping fluctuations is proportional to $1/\sqrt{WL}$, so minimum sized devices produce the worst case random $V_{\rm T}$ mismatch. Statistical analysis is necessary to confirm functionality in the face of process variation, and some devices might need to increase in size to ensure acceptable yield.

A. Standard Cells and Minimum Energy

Standard cell libraries help digital circuit designers to reduce the design time for complex circuits through synthesis. Most standard cell libraries focus on high performance, although including low-power cells is becoming more popular [18]. Lower power cells generally use smaller sizes. One standard cell library geared specifically for low power uses a reduced set of standard cells and branch-based static logic, to reduce parasitic capacitances. Eliminating complicated cells with large stacks of devices and using a smaller total number of logic functions was shown to reduce power and improve performance [19]. Standard cell libraries have not been designed specifically for subthreshold operation. This section evaluates the performance of a 0.18-μm standard cell library in subthreshold operation.

We use the 8-bit, 8-tap FIR filter to compare normal cell selection with cells sized to minimize the operating voltage. Fig. 7 shows the minimum operating voltages for the different standard cells appearing in a normal synthesis of the FIR filter. The typical (TT) and worst case (FS and SF) process corners are shown. All of the cells operate at 200 mV at the typical corner, showing the robustness of static CMOS logic. Additionally, most of the cells operate at 300 mV in the worst case, which is close to the optimum performance shown in the previous section for the FIR filter. The cells which exhibit the worst case (failing below 400 mV) are flip-flops and complex logic gates with stacks of series devices (e.g., AOI). We eliminated the problematic cells by preventing the synthesis tool from selecting logic gates with large device stacks and by re-sizing the offending flip-flop cell [17].

Fig. 8 shows a schematic of the D-flip-flop. In the standard implementation, all of the inverters use small nMOS and only slightly larger pMOS devices except I3, which is several times larger to reduce C–Q delay. At the FS corner (fast nMOS, slow pMOS), the narrow pMOS in I6 cannot hold N3 at a one when CK is low. This is because the combined, strong off current in the nMOS devices in I6 and I3 (larger sized) overcomes the weakened, narrow pMOS device in I6. Tying back to the ring oscillator in Fig. 5, the combined nMOS devices create an effective $\rm P/N$ ratio that is less than one. To prevent this, we reduced the size of I3 and strengthened I6. The larger feedback inverter creates some energy overhead. However, the resized flip-flop can operate at 300 mV at all process corners in simulation. Fig. 9 shows the lowest operating voltage for the cells in the minimum-$V_{\rm DD}$ FIR filter. The number of cell types has

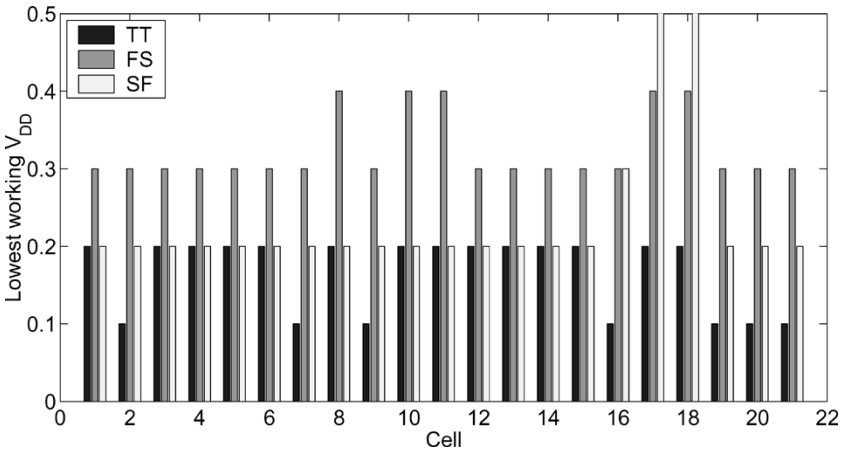

Fig. 7. Standard cell functionality in synthesized FIR filter using normal cell selection over process corners (simulation).

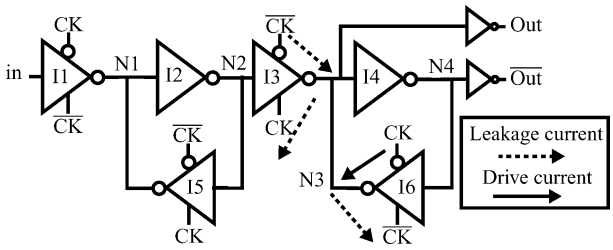

Fig. 8. Standard cell flip-flop at worst case failure point where $\mathrm{CK} = 0$ at FS corner (fast nMOS, slow pMOS).

reduced, and all of the cells work at 300 mV across all corners. The next section uses test chip measurements to compare the filter sized for minimum V_{DD} with the normal filter.

IV. Measured Results From Test Chip

A 0.18-μm, six metal layer, 1.8-V, 7 mm^2 test chip was fabricated to measure the impact of sizing on minimum energy operation of standard cells. The test chip features two programmable 8-bit, 8-tap FIR filters. Both filters produce nontruncated 19-bit outputs. The first filter was synthesized using the unmodified synthesis flow and normal cells (Fig. 7). The second filter was synthesized using the modified flow in which some cells were omitted and some cells were resized to minimize V_{DD} (Fig. 9). Both filters can operate using an external clock or an on-chip clock generated by a ring oscillator that matches the respective critical path delay of the filters.

Fig. 10 shows the measured performance versus V_{DD} for the two filters using their respective critical path ring oscillators. The minimum-V_{DD} filter exhibits a 10% delay penalty over the standard filter. Both filters operate in the range of 3 kHz to 5 MHz over V_{DD} values of 150 mV to 1 V. Both filters are fully functional to below 200 mV.

Fig. 11 shows an oscilloscope plot of the standard filter working correctly at $V_{\mathrm{DD}} = 150$ mV. The clock in this plot is produced by the ring oscillator on-chip. The reduced drive current and large capacitance in the output pads of the chip cause the slow rise and fall times in the clock, but the signal is still full swing. One bit of the output is shown.

Fig. 12 shows the measured total energy per output sample of the two FIR filters versus V_{DD}. The solid line is an extrapolation of $C_{\mathrm{eff}}V_{\mathrm{DD}}^2$ for each filter, and the dashed lines show the measured leakage energy per cycle. Both filters exhibit an optimum supply voltage for minimizing the total energy per cycle between 250 and 300 mV. There is a measured overhead energy per cycle of 50% in the filter sized for minimum V_{DD}. The figure also shows the worst case minimum V_{DD} for the two filters (cf. Figs. 7 and 8). Accounting for overhead at the worst case minimum V_{DD}, the minimum-V_{DD} FIR offers a reduction in total energy of less than 10% at the worst case process corner, but this improvement comes at a cost of 50% at the typical corner.

Simulations show that the measured overhead cost in the minimum-V_{DD} filter primarily results from restricting the cell set that the synthesis tool could use. Since the tool was not optimized for the smaller set of cells, we did not see the improvements that are possible through this approach [19]. Using only sizing to create the minimum V_{DD} filter would have decreased the overhead. However, the shallow nature of the optimum point in Fig. 12 shows that the unmodified standard cell library does not use much extra energy by failing at a higher V_{DD} at the worst case corner. Thus, existing libraries provide good solutions for subthreshold operation. Simulation shows that a minimum-sized implementation of the FIR filter has $2\times$ less switched capacitance than the standard FIR, so a mostly minimum-sized library theoretically would provide minimum energy circuits [17].

V. Movement of Minimum Energy Point

This section examines the minimum energy point for a subthreshold system whose energy is the primary constraint. We assume that the system is implemented in a standard technology whose V_{T} is fixed (i.e., – no triple wells for body biasing). In this scenario, we examine the problem of setting V_{DD} to minimize energy per operation. The following section demonstrates how this solution can change based on operating parameters.

A. Operating Conditions

Equations (8) and (9) show that any relative increase in the leakage component of energy per cycle will push the optimum

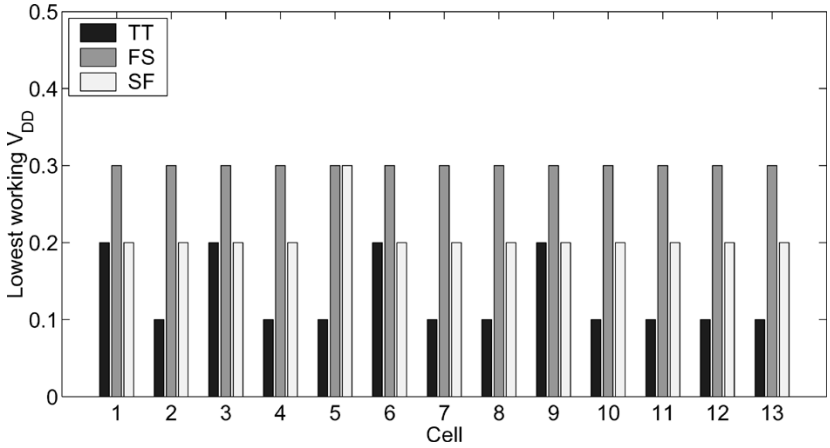

Fig. 9. Standard cell functionality in synthesized FIR filter using cells sized to minimize $V_{\rm DD}$ over process corners (simulation).

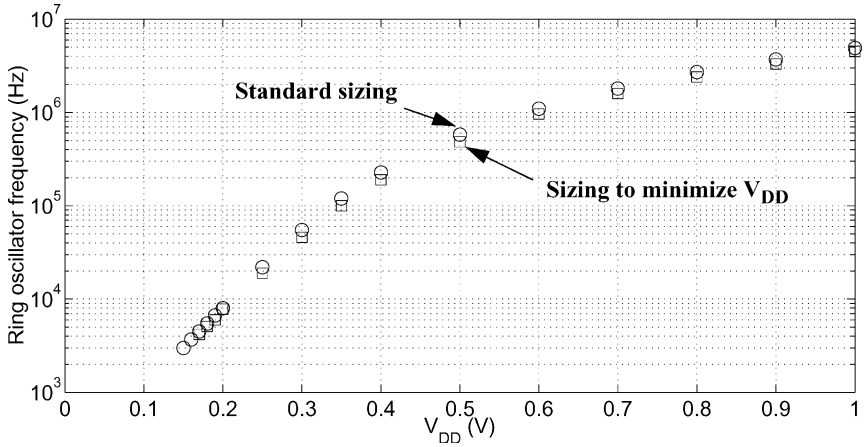

Fig. 10. Measured performance of programmable FIR filters on the test chip. Standard FIR is 10% faster than the minimum-voltage FIR.

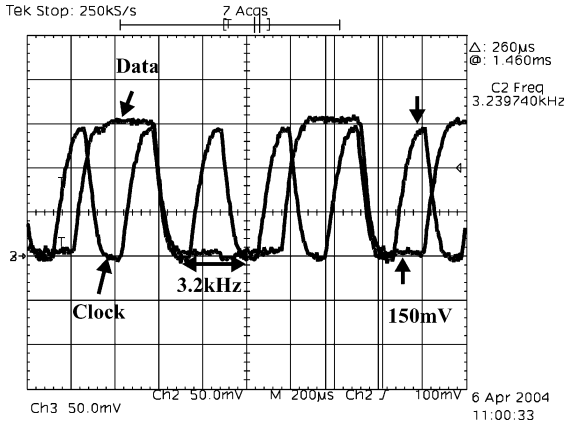

Fig. 11. Oscilloscope plot from the test chip showing $V_{\rm DD} = 150$ mV filtering operation with ring oscillator clock at 3.2 kHz.

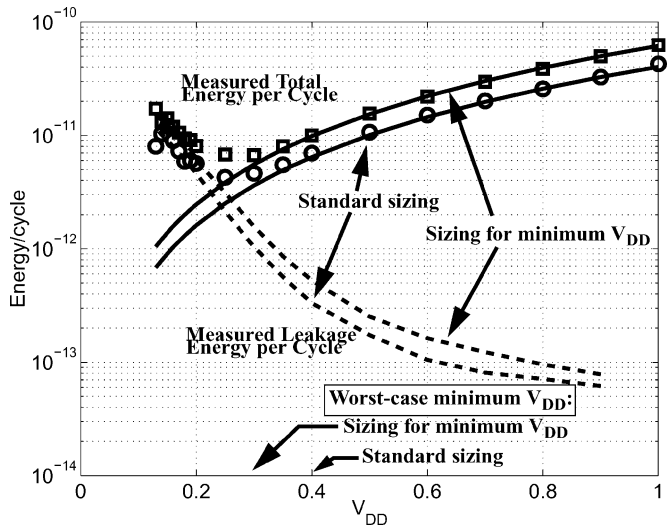

Fig. 12. Measured energy per operation of the FIR filters on the test chip.

$V_{\rm DD}$ higher, and the frequency at the optimum point also increases. This corresponds to any decrease in $E_{\rm DYN}$ or increase in E_L. Likewise, any decrease in E_L or increase in $E_{\rm DYN}$ will lower the optimum $V_{\rm DD}$. These types of changes can occur for a given circuit without changing its intrinsic attributes.

For example, consider using the FIR filter in a system whose workload, ω, changes widely. This might be in a video context where the processing per frame depends on the difference between consecutive frames. If the current frame is nearly identical to the previous, then very little work is required. A scene change, on the other hand, could demand the maximum number of computations. Assuming the clock is gated when no computation is required and normalizing to one cycle, $C_{\rm eff}$ per cycle becomes $\omega C_{\rm eff}$ in (4).

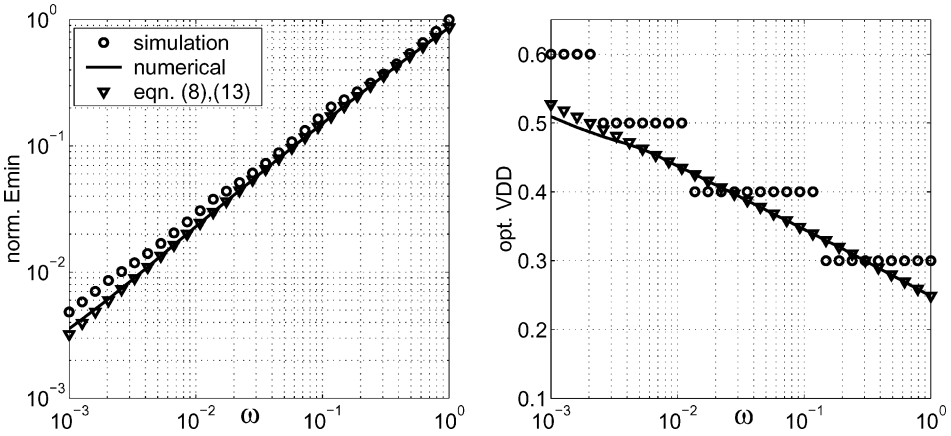

Fig. 13. Normalized energy (left) and optimum $V_{\rm DD}$ (right) for FIR versus workload, ω. Simulation $V_{\rm DD}$ quantized to 100 mV.

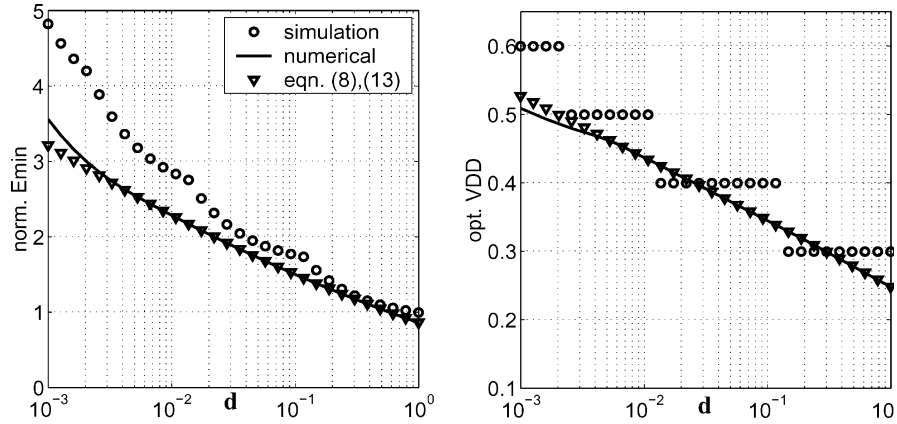

Fig. 14. Normalized energy (left) and optimum $V_{\rm DD}$ (right) for FIR versus duty cycle, d. Simulation $V_{\rm DD}$ quantized to 100 mV.

Duty cycle d also can vary widely. A lower duty cycle means that the circuit spends more idle cycles (e.g., waiting for data) per active cycle. Consequently, the leakage contribution per operation increases, which corresponds to replacing $W_{\rm eff}$ with $W_{\rm eff}/d$ in (5). Normalizing to one cycle, we include duty cycle and workload in the analytical model and solve the equation set again to find the optimum $V_{\rm DD}$, resulting in a new equation for β

$$\beta = \frac{-2\omega C_{\rm eff}}{\frac{W_{\rm eff}}{d} L_{\rm DP} K C_g} e^2 > -e^{-1}.$$

Figs. 13 and 14 show the effects of our simplified workload and duty cycle examples on the minimum energy and optimum $V_{\rm DD}$ of the FIR filter. The figures compare the numerical result with the analytical model and with simulation. The supply voltage for the simulations was quantized to 100 mV increments. The quantization causes most of the error for values of ω and d close to one. The error in modeled energy at low values of ω and d occurs because the optimum $V_{\rm DD}$ has exceeded $V_{\rm T}$. Thus, the assumption of subthreshold operation implicit to the analytical model becomes invalid. The numerical model is also less accurate in that region. The analytical result matches the numerical values quite well until $V_{\rm DDopt}$ nears $V_{\rm T}$.

Large reductions in either ω or d result in increased optimum $V_{\rm DD}$, but the total energy per operation (normalized to one cycle) decreases as workload decreases and increases when duty cycle decreases. Clearly, knowing the average workload and duty cycle of a circuit can impact the choice of optimum supply voltage. The operational frequency, and thus the data rate, implicitly changes with $V_{\rm DD}$ in these figures. A system in which these parameters vary widely would benefit from closed-loop tracking of the optimum point since Figs. 13 and 14 show a large variation in the minimum energy.

The optimum point also depends on temperature, but the sensitivity over the range of possible operating temperatures is not as large. Fig. 15 shows the effect of temperature on the components of energy. The numerical model shown in Fig. 15 accounts for temperature dependence by decreasing the effective threshold voltage and increasing mobility ($I_{\rm off}$) at higher temperatures as in [20]. These changes to the numerical model match well with simulation across most of the temperature range, but they underestimate the leakage energy at high temperatures. The threshold voltage drop accompanying a temperature increase raises the leakage current exponentially. This effect appears in the figure at higher $V_{\rm DD}$ where $I_{\rm LEAK}$ dominates E_L. The lower $V_{\rm T}$ also causes the delay to decrease, countering the rise in $I_{\rm LEAK}$, so the total effect on E_L is not so pronounced at lower $V_{\rm DD}$ where the delay component dominates. Consequently, the total leakage energy does not change enormously near the minimum energy point. It does increase by several times, however, and the optimum $V_{\rm DD}$ increases by about 100 mV over the full temperature range.

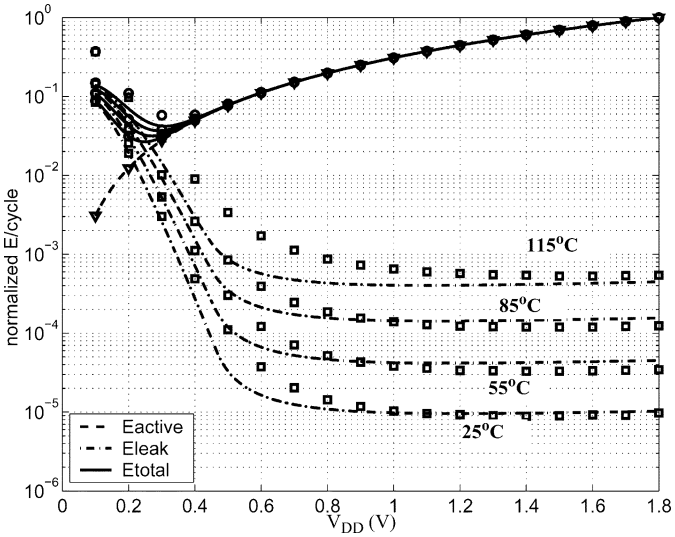

Fig. 15. Dependence of minimum energy point on temperature shown in simulation (markers) and by the numerical model (lines). Temperature varies from 25 °C to 115 °C.

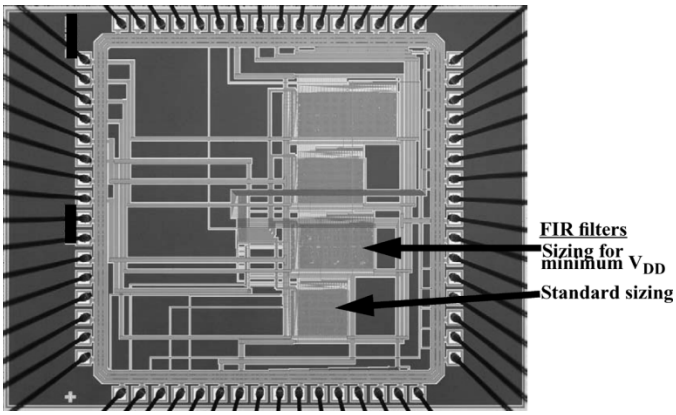

Fig. 16. Annotated die photograph of 0.18-μm subthreshold FIR test chip.

VI. Conclusion

This paper has examined minimum energy operation for subthreshold circuits. We have shown that the minimum energy point depends on the technology, the characteristics of the design, and on operating conditions such as temperature, duty cycle, and workload. The optimum $V_{\rm DD}$ for minimizing energy per operation changes over several hundred millivolts when these parameters vary, pointing to the importance of tracking the optimum point or carefully characterizing a design before choosing $V_{\rm DDopt}$. We introduced an analytical solution for the optimum $V_{\rm DD}$ and $V_{\rm T}$ to minimize energy for a given frequency in the subthreshold region. Simulations matched the analytical value within a few percent as long as the subthreshold assumption was valid. We also examined device sizing for subthreshold operation. For typical circuits and modern technologies, the optimum supply voltage for minimizing power is higher than the failure point for minimum sized devices at the typical corner. Thus, minimum sized devices are theoretically optimal for minimizing power. Even if the minimum energy point for a certain process corner or unusual circuit occurs at a supply voltage where minimum sized devices cannot function, the shallow nature of the optimum prevents up-sizing to reduce the minimum possible operating voltage from being worthwhile. Measurements from a test chip, shown in Fig. 16, confirm that existing static CMOS standard cell libraries function well in sub-threshold. Resizing or restricting cell usage in such libraries can lower the worst case minimum $V_{\rm DD}$, but the overhead increases energy consumption at the typical corner. In theory, a standard cell library primarily using minimum-sized devices would minimize energy per operation.

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