Sub-threshold Circuit Design with Shrinking CMOS Devices

Benton H. Calhoun, Sudhanshu Khanna,
Randy Mann, and Jiajing Wang

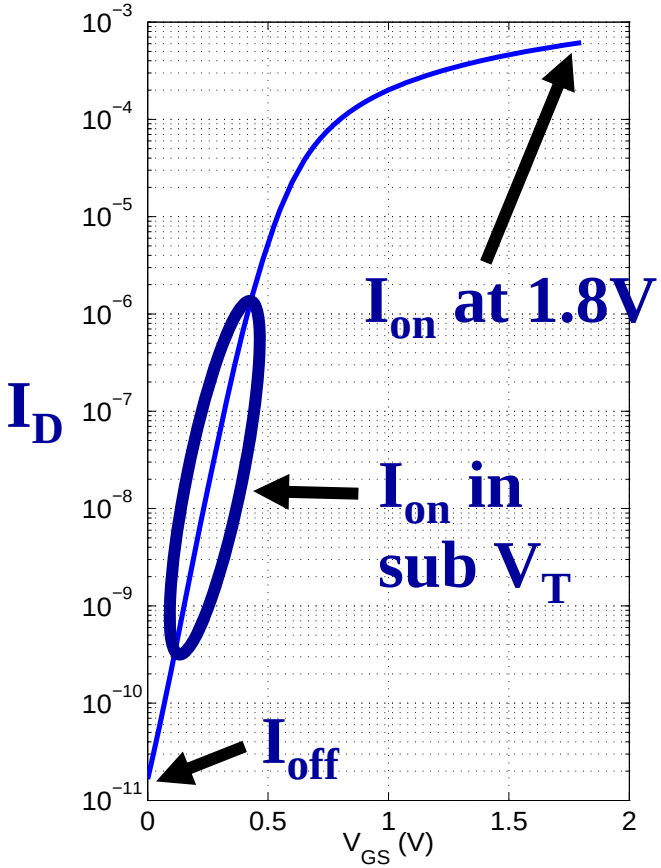
Electrical and Computer Engineering
University of Virginia
Charlottesville, VA, USA

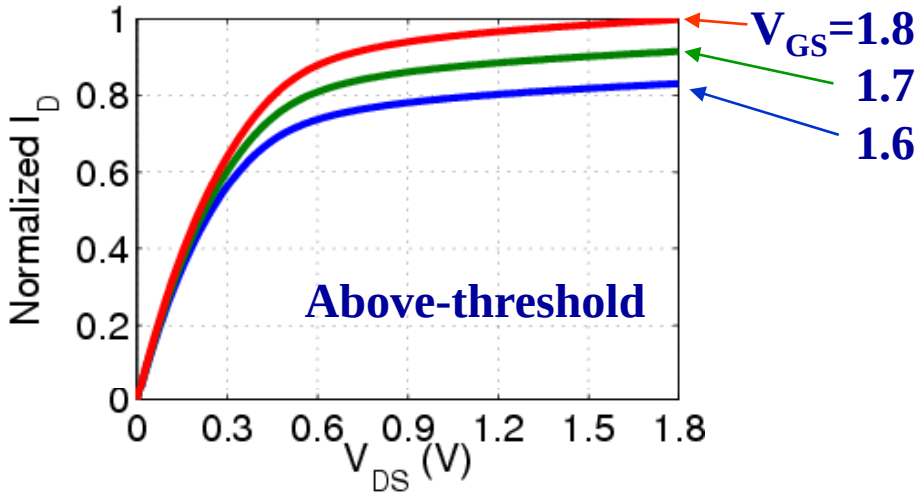
Outline

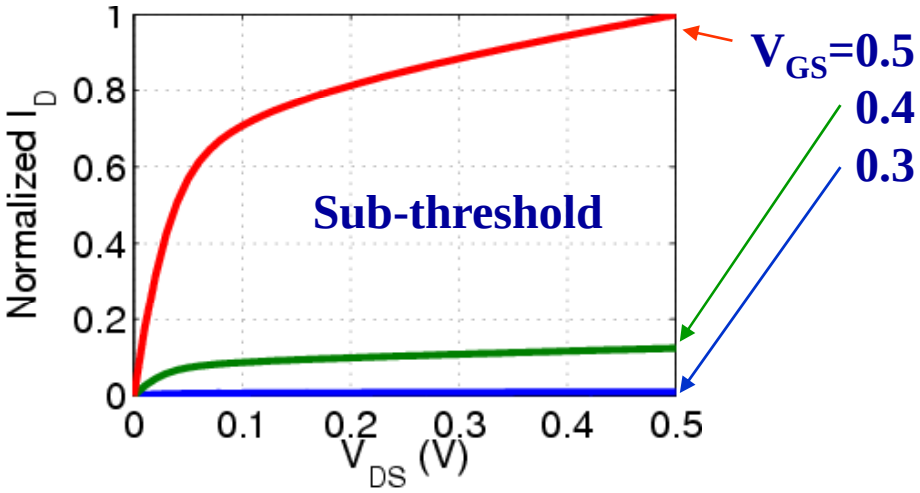
- Sub-threshold Circuits
- Predictive Technology Models
- Obstacles to Sub-threshold Scaling
- Minimizing Energy with Scaling
- Extending Sub-threshold Scaling
- Conclusions

Sub-threshold Operation

- Sub-threshold logic operates with $V_{DD} < V_T$
- Both *on* and *off* current are sub-threshold "leakage"







Benefits of Sub-threshold

- Sub-threshold benefits: V_{DD} from [1.8,1.0]V to [0.4,0.2]V

Leakage Power Decreases: Power = V_{DD} I_{off}

V_{DD} goes down: 2.5X to 9X

DIBL reduces $I_{sub\text{-}threshold}$: 2X to 10X

I_{gate} and I_{GIDL} become negligible

Pleak: 5X to 90X

Energy Consumption Decreases

$E_{active} = CV_{DD}^2$

E_{total}/operation minimized in sub-V_T

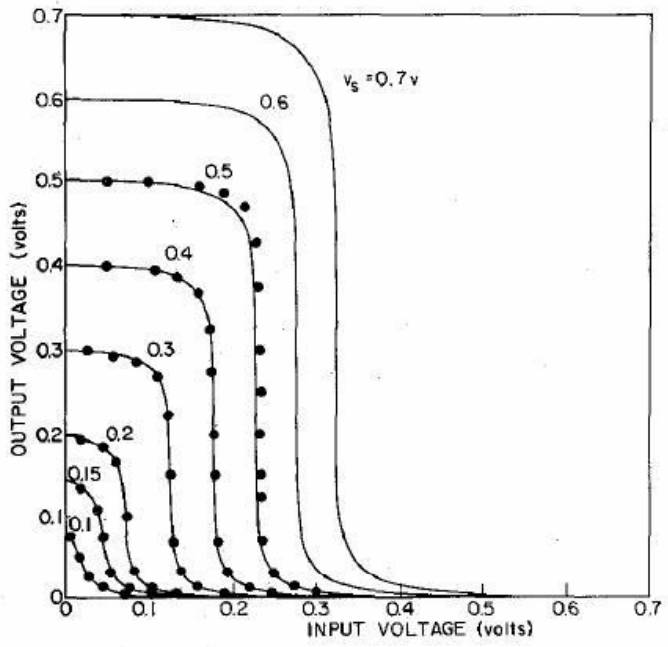
Reliability Effects Improve

NBTI, EM, TDDB

Main Limitation: Slow Speed, but OK for certain apps

Sub-Threshold Digital Circuits Overview

- 1972: Sub-threshold theorized for minimum V_{DD} operation (*Swanson & Meindl, JSSC*)
- Major challenges:
  - Reduced Ion/Ioff
  - Variation (local V_T variation, especially)
- Last 5 years: sub-threshold demos of components
  - Logic
  - Memory (SRAM)
  - Micro-processors



Swanson & Meindl, 1972

Primary Use of Sub-threshold Circuits (to date)

- Ultra Low Power (ULP) operation (microsensors, etc.)
- Often long sleep times
- Use an older technology – Is the talk over?

PTM (nm)	T_{sleep}=0	T_{on} + T_{sleep} = 0.1ms	T_{on} + T_{sleep} = 1ms
90	107	107	129
65	77.7	85.5	147
45	58.4	69.8	193
32	47.2	84.0	428
22	41.2	222	1860

Assume 10X less leakage in standby

Alternative Uses for Sub-threshold

1. Wide range dynamic voltage scaling (UltraDVS)
   [Calhoun & Chandrakasan, ISSCC, 2005]
   – e.g. Watchdog sensor, safety critical sensor, etc.
2. Support for high performance
   – e.g. Standby monitor, wakeup circuit, etc.

When to use sub-threshold with scaling:

- Other factors push scaling
- Still need min E for some components *or* times

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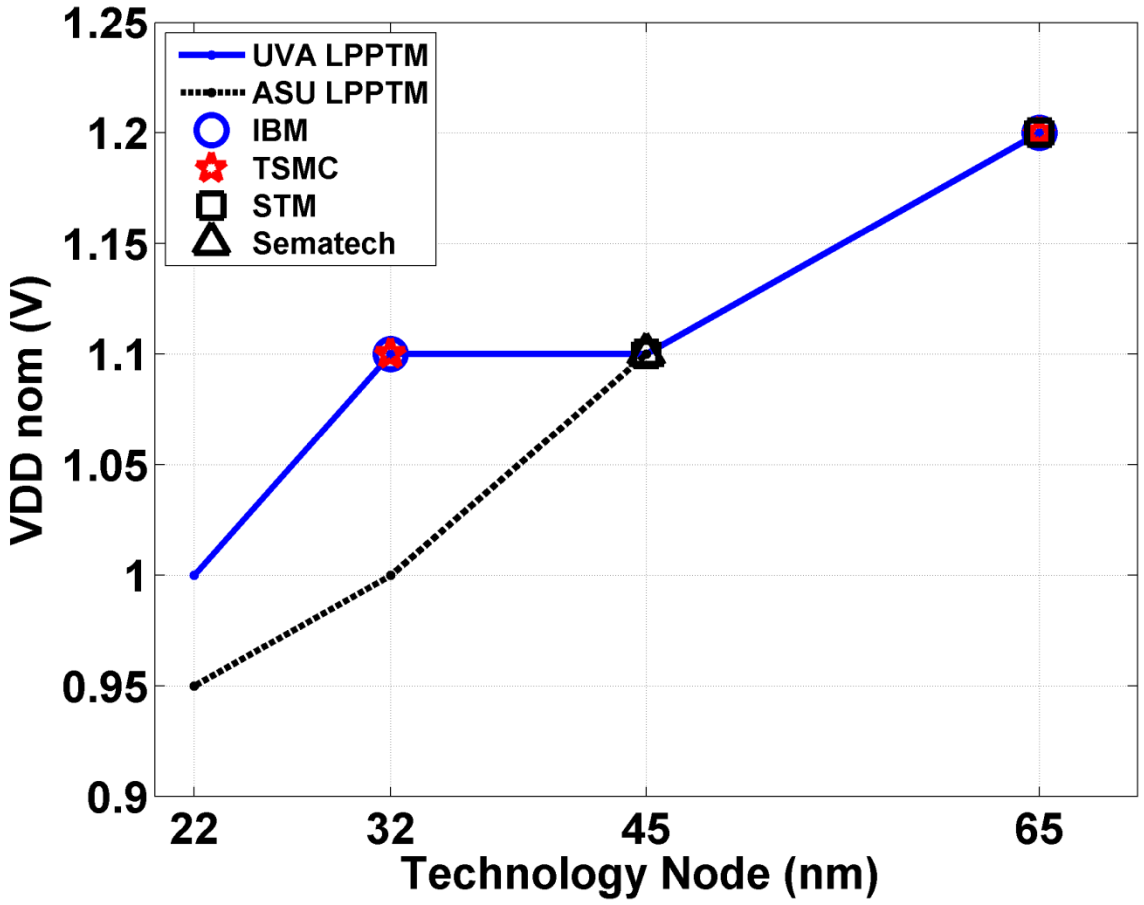
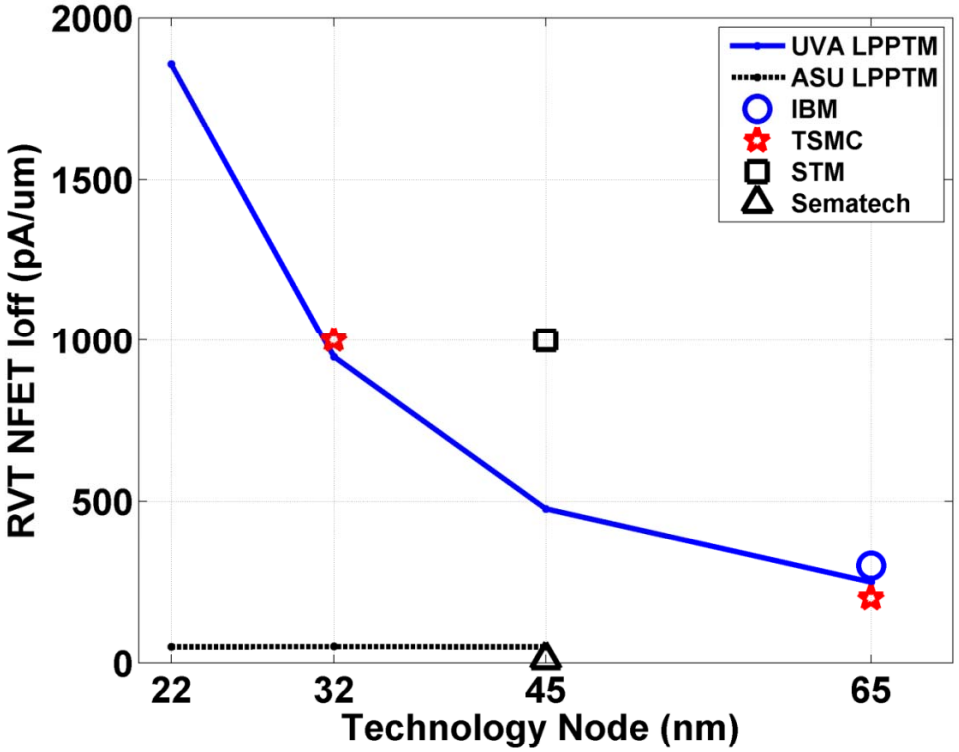
Predictive Technology Models

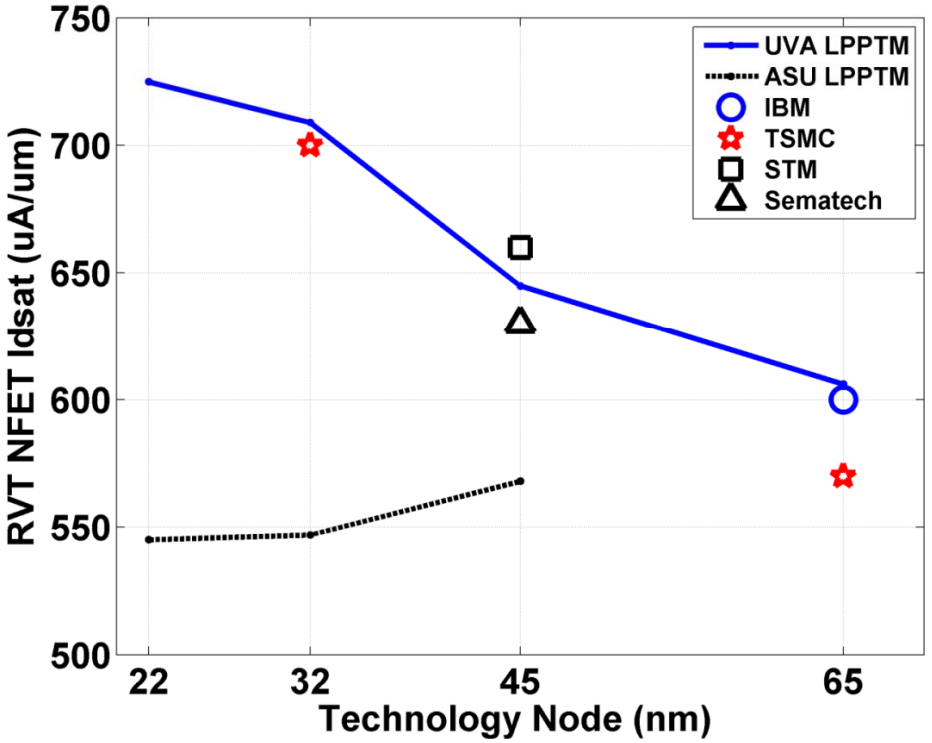
- PTMs from Arizona State (thank you!)
- But, we needed our own version
  - for low power technologies
  - support variation
- Fit to data from industry, papers
- ASU low power PTMs
  - Since became available
  - Fit to ITRS

PTM V_{DD} Scaling

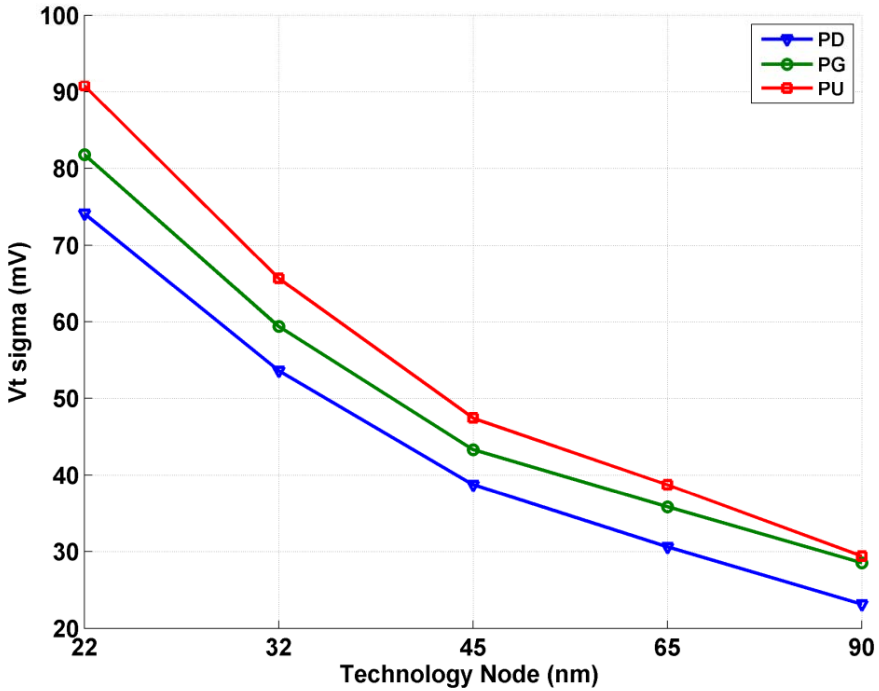


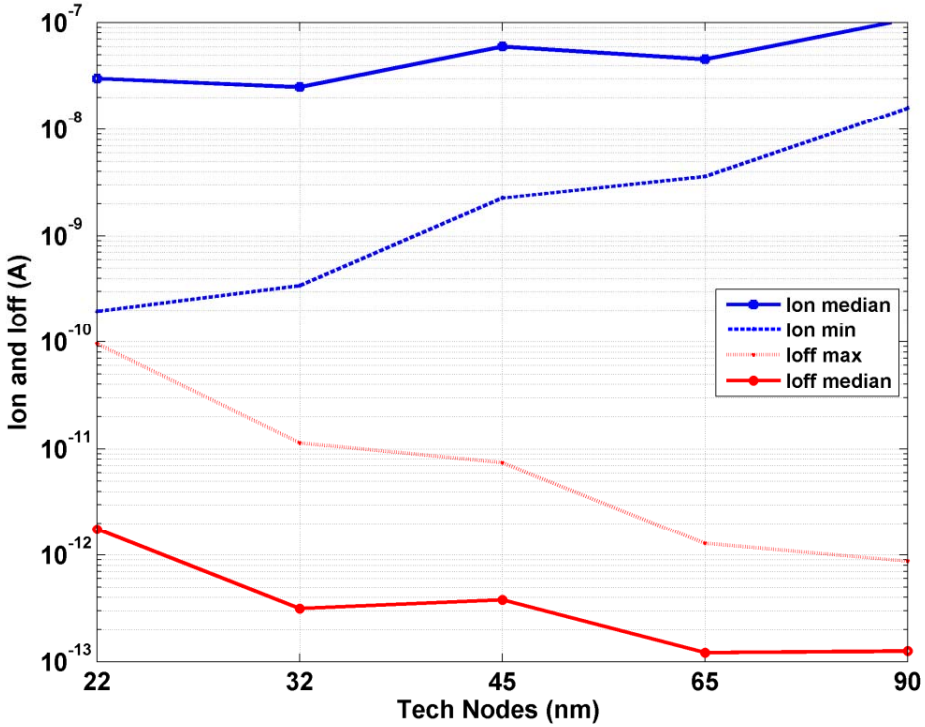
PTM MOS Current Scaling





PTMs and variation





- V_T and L variation
- Select σ based on literature
- Variability impacts functionality (I_{on} vs. I_{off})

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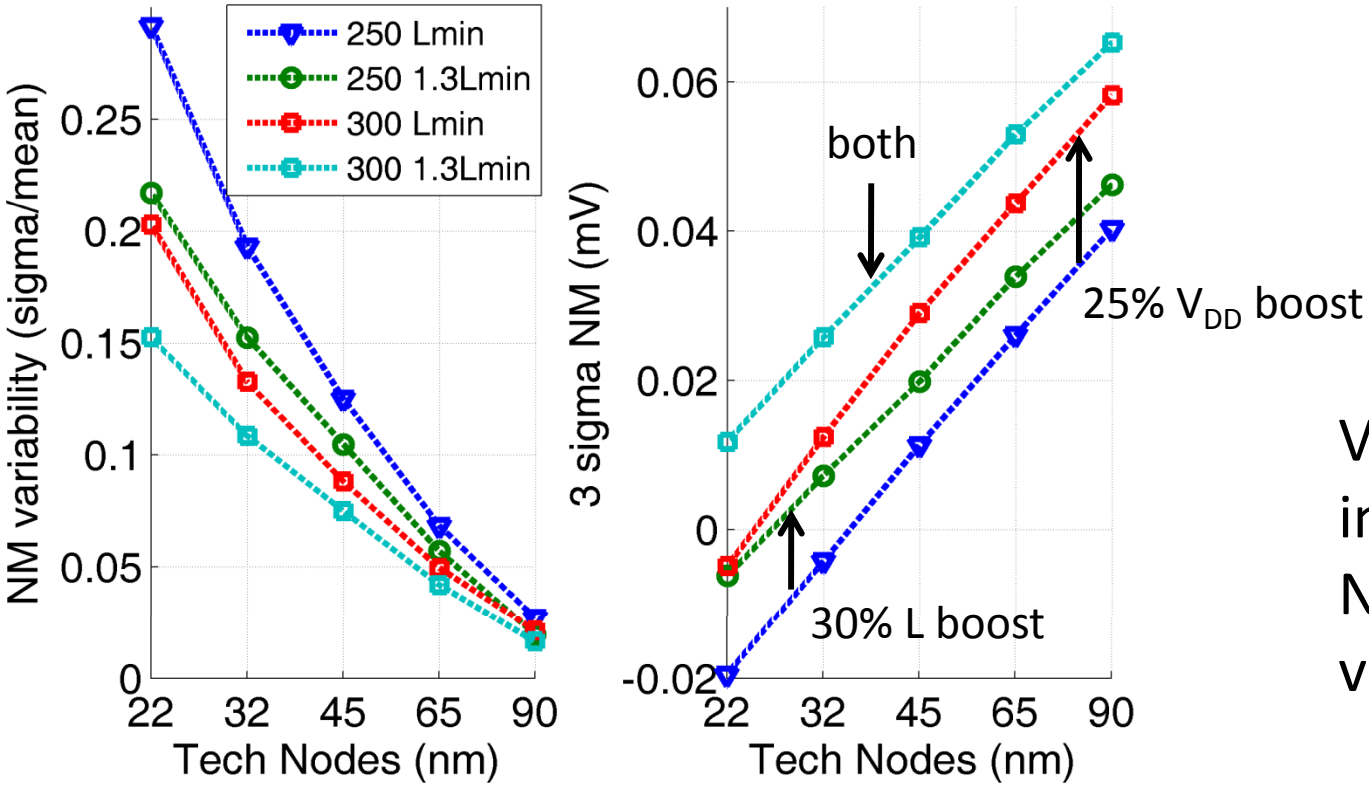
Variation Impacts Noise Margin

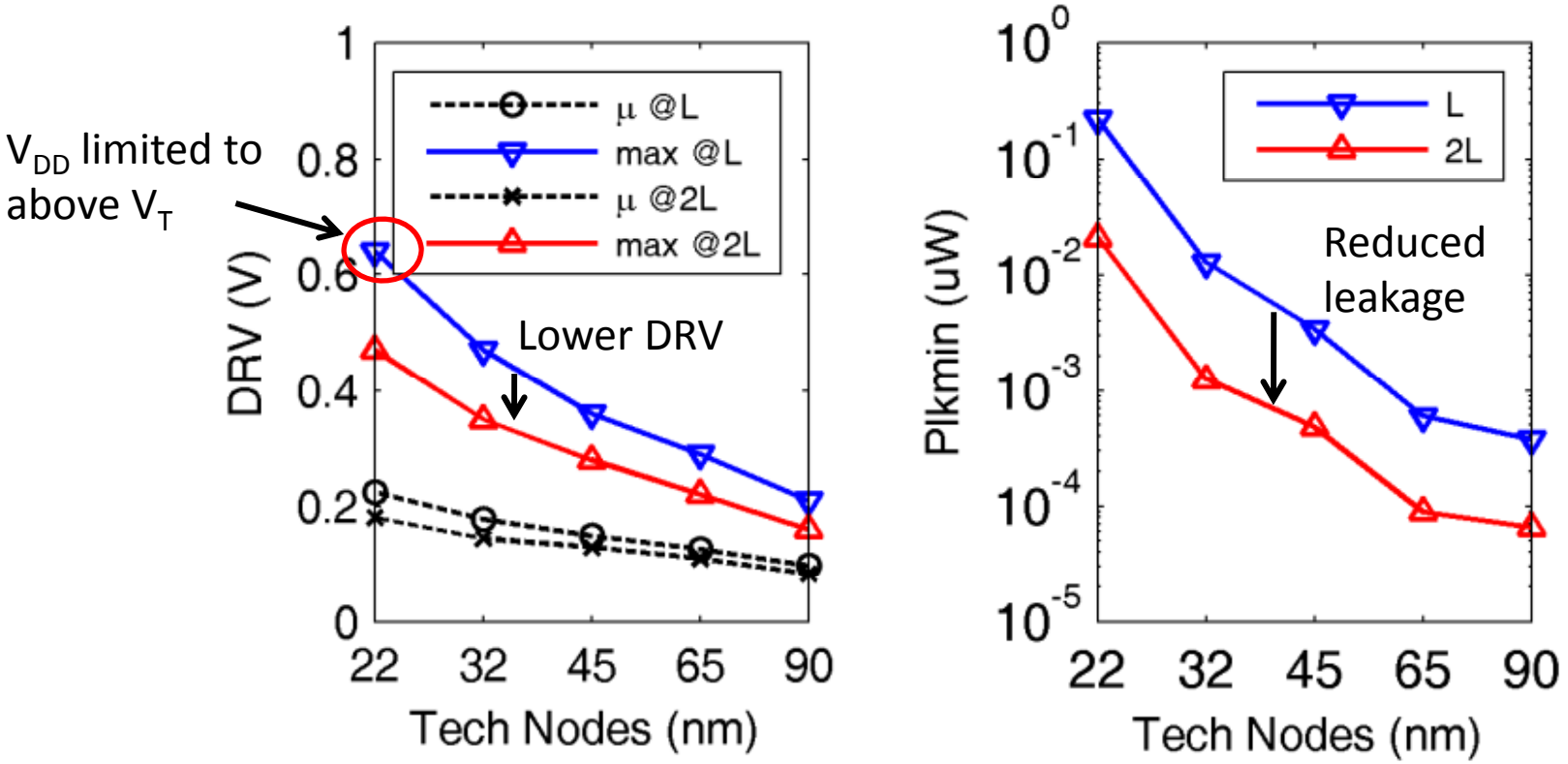
- Noise margin in logic [Kwong '06]
- NAND (poor V_{OL}) to NOR (poor V_{OH}) butterfly



V_{DD} boost and L increase help NM and reduce variability

Variation Impacts Data Retention

- Noise margin in storage elements
  - Aggravated by smaller devices
  - Sub-threshold bitcells – back-to-back inverters to store



Observations about Obstacles

- V_{DD} floor exists – V_{min} for functionality
  - Logic robustness (noise margin)
  - Data Retention Voltage
- V_{min} may be higher than V_{opt} (for min E)
- V_{min} is a function of L
- Within reason, can trade area for V_{DD}, but increases capacitance…
  - Need to look at min E point for tradeoff

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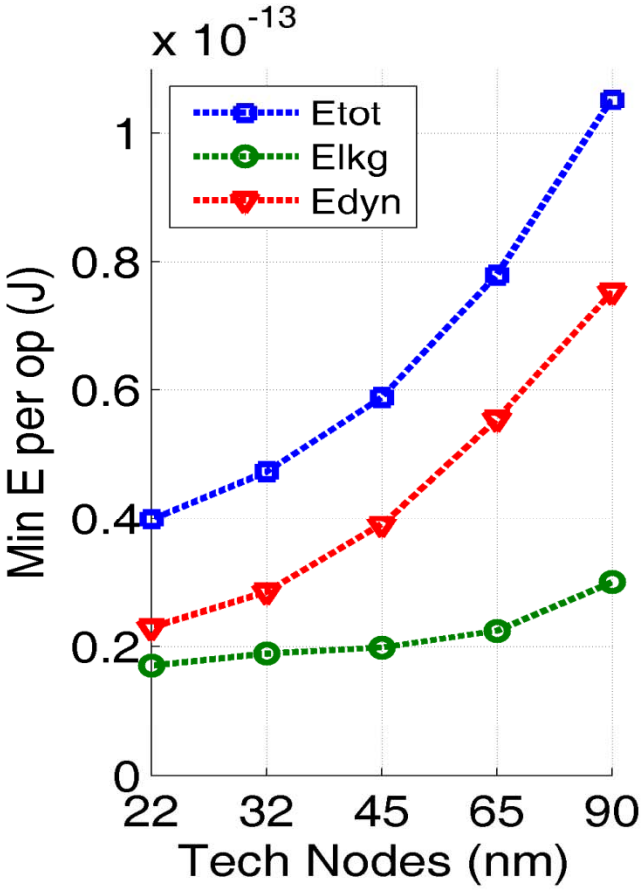
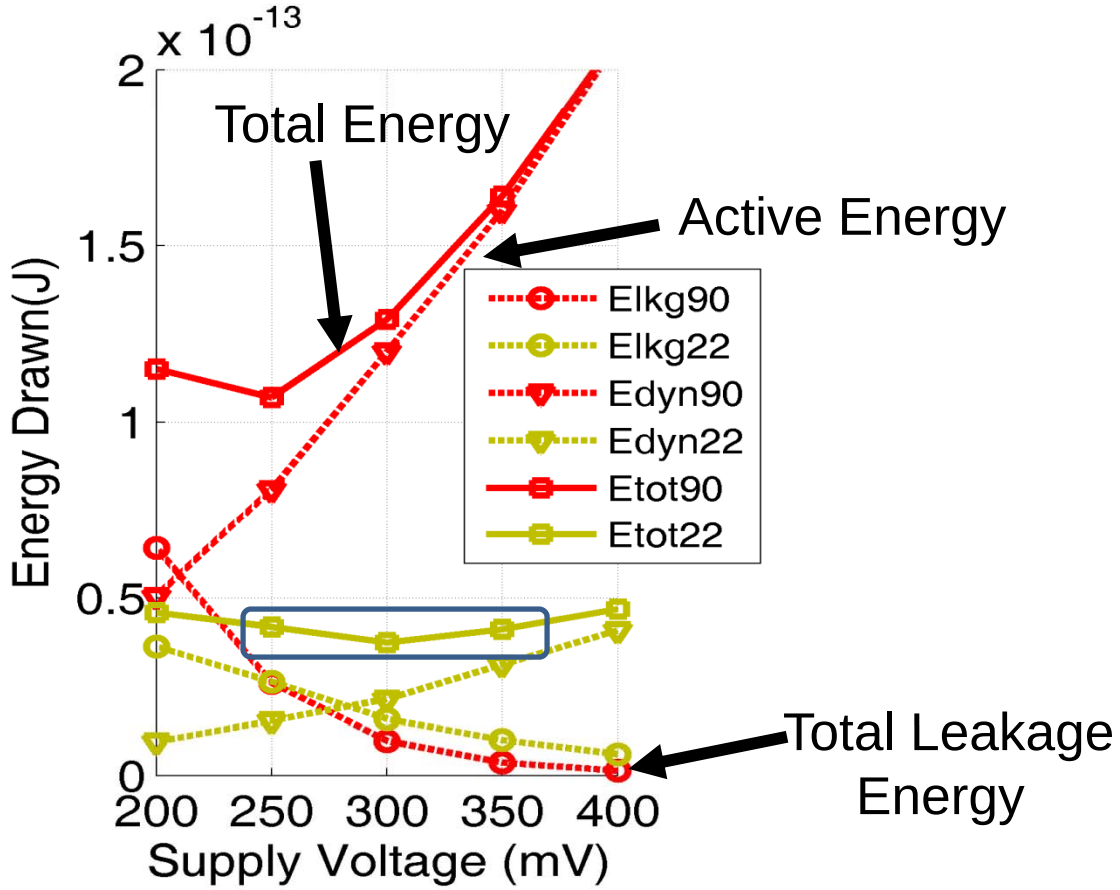
Sub-V_T Minimum Energy Operation



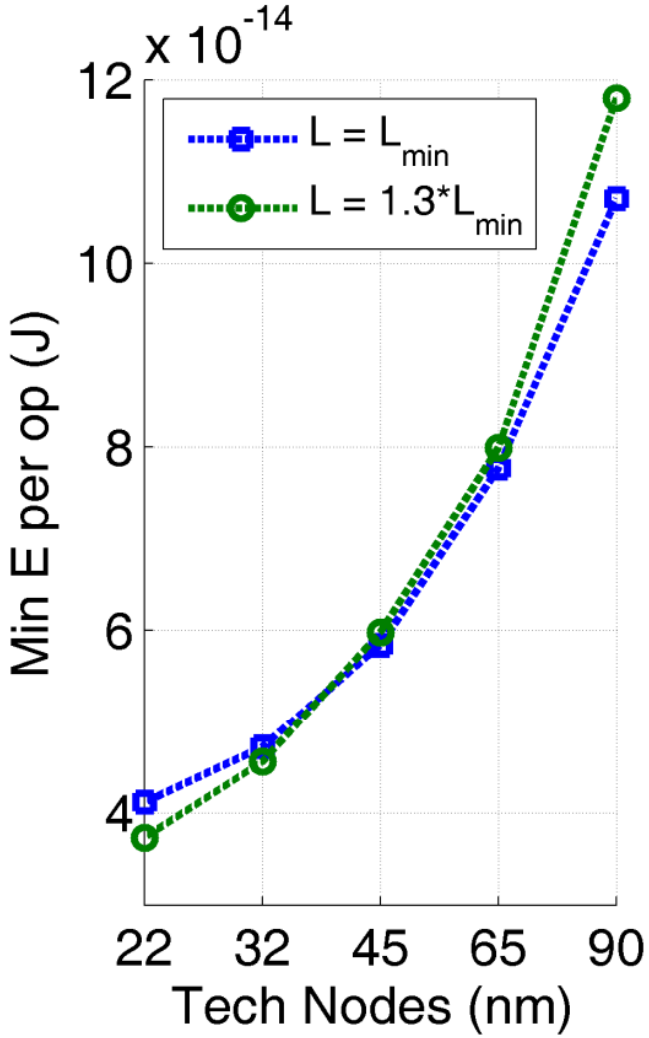


Scaling reduces E_{min}, and raises V_{opt}

E_{min} insensitive to small V_{DD} changes

Energy Tradeoff for L

- From earlier, L increase improves DRV and NM
- Increasing L improves energy at smaller nodes
- L and V_{DD} increase V_{min}, do not cost much energy



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What else to do?

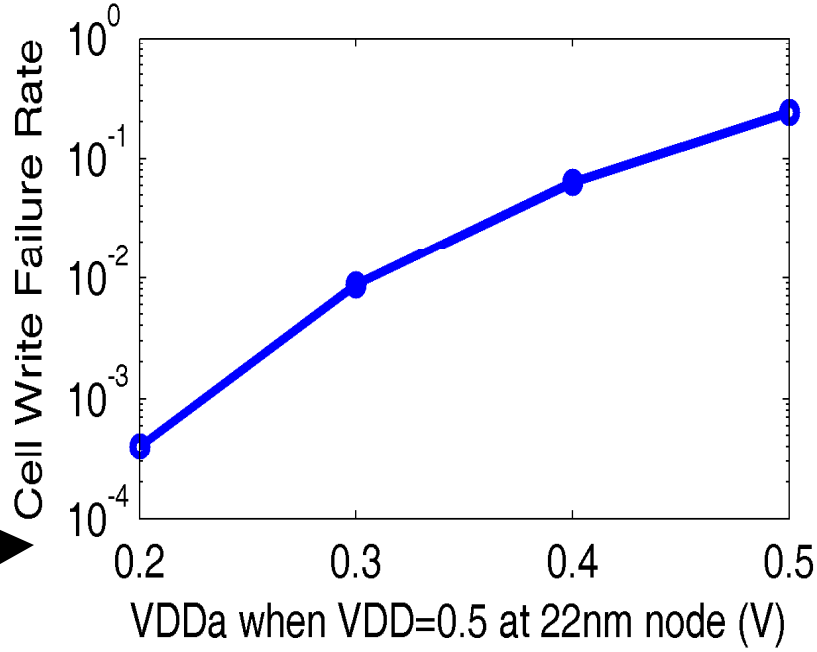
- L and V_{DD} are general knobs, but for sensitive circuits, use context specific response
- Leverage strong knobs (voltages and topology)

- One example: SRAM
  - Alternative bitcells
  - Combine with assist methods

Improve Write Noise Margin

* 8T/10T cell has the same poor write NM as 6T

- Goal
  - Weaken pull-up FET
  - Strengthen pass-gate FET
- Knobs
  - Size pass-gate to pull-up ratio (not efficient)
  - Collapse Bitcell V_{DD}
  - Boost WL V_{DD}
  - Boost VBP



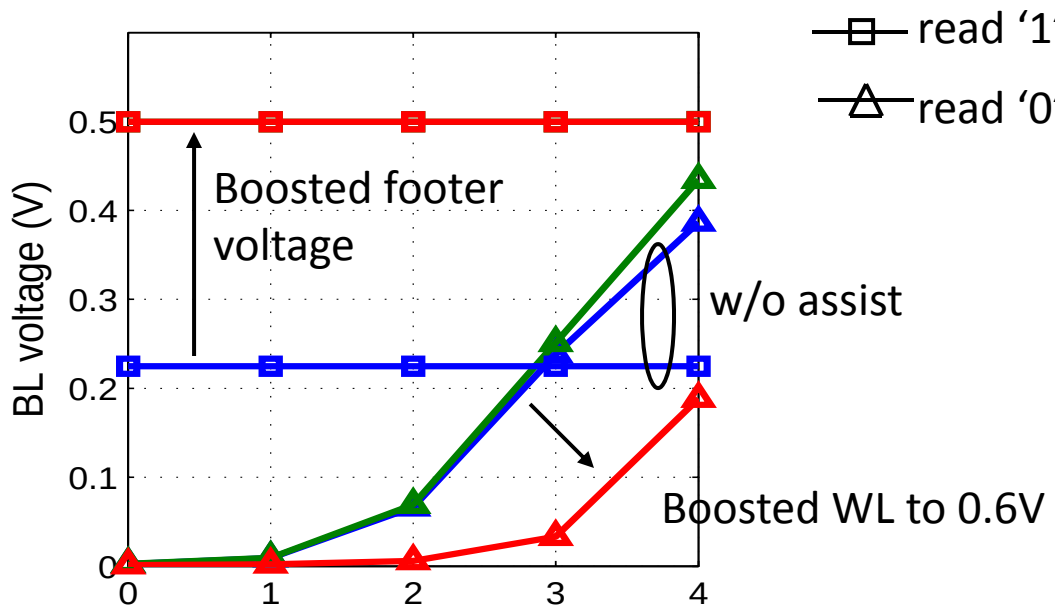
Bitcell V_{DD} collapse gives adequate writability to 22nm

Use V_{DD} collapse (plus others?) to fix WNM

Improve Read Access

8T bitcell @V_{DD}=0.5V

256-cell per BL



Transistor V_T variation (σ) for PTM-LP 22nm node

- To combat large V_T variation, two or more knobs must be used simultaneously
  - boosted footer voltage to improve reading 1
  - boosted WL to improve reading 0

Conclusions

- Scaling sub-threshold makes sense for specific cases, but NOT for ULP only
- Logic NM and DRV (more fundamental) limit voltage scaling in newer technologies
- L and V_{DD} upscaling help
- Customization necessary for sensitive circuits

- Thank you. Any questions?