Sub-threshold Operation and Cross-Hierarchy Design for Ultra Low Power Wearable Sensors

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Thesis Statement for this Talk

- Observation:
  Sub-threshold digital circuits tend to be designed as standalone blocks

- Limitation:
  This approach limits savings to digital portion only

- THESIS STATEMENT:
  To get full benefits from sub-threshold digital circuits, we must CO-DESIGN them with the system in which they are deployed

Outline

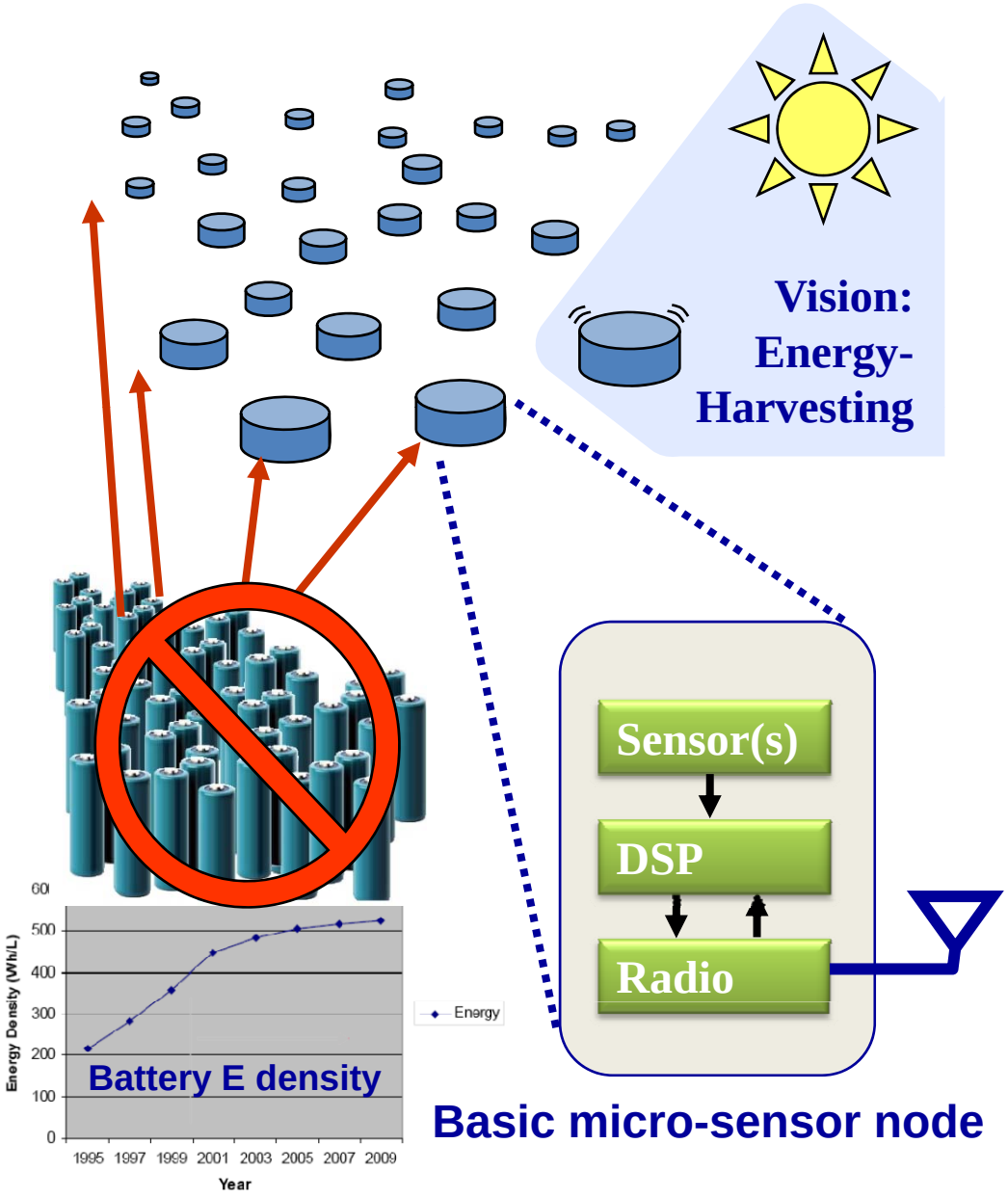
- Body Area Sensor Networks (BASNs)
- Sub-threshold Circuits for BASNs
- Body Area Sensor Design
- Conclusions

Generic Wireless Micro-sensor Nodes

System Specifications

Application Characteristics	Typical Values
Extended Lifetime	5 years+
Number of Nodes	100's – 1000's
Node Size	<1 cm^3
Energy	1000's Joules
Clock Speed	1kHz – 1MHz
Avg. Power Requirement	~100 μW

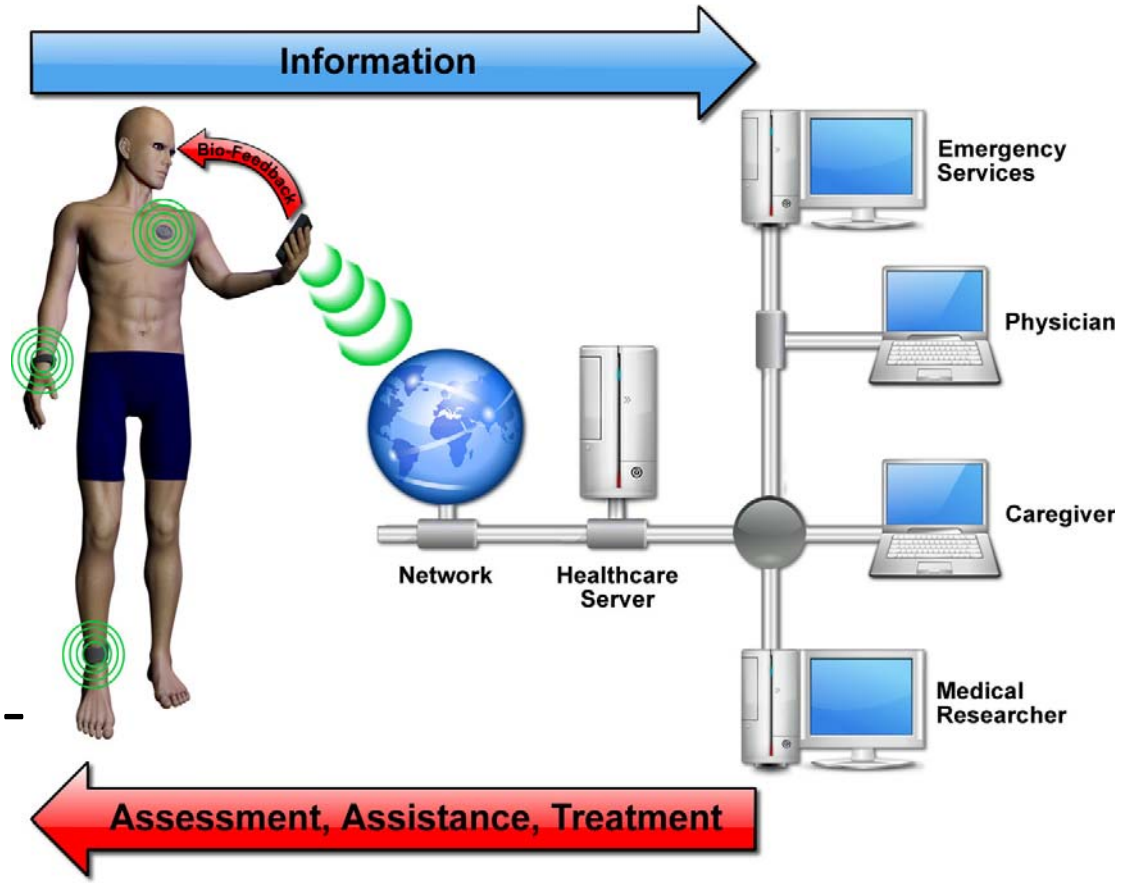
Sub-V_T perfect for long lifetimes on small energy!



Basic micro-sensor node

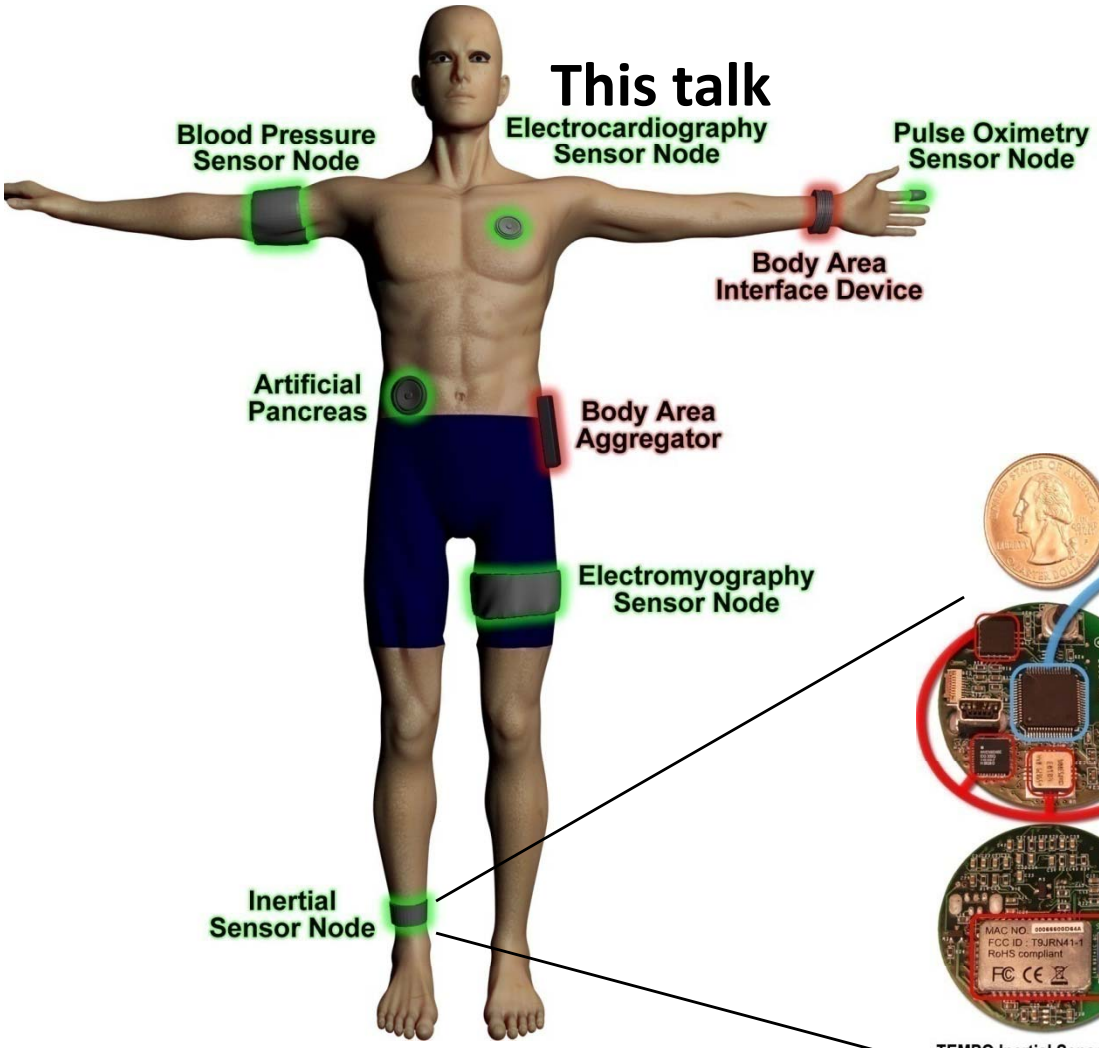
Body Area Sensor Networks (BASNs)

- Sensors worn / implanted: Need long life, small
- Important factors for adoption (on top of technical barriers):
  - Perceived value
  - Safety / Fidelity
  - Ease of use
  - Privacy
  - Security
- Well-suited for Sub-V_T operation

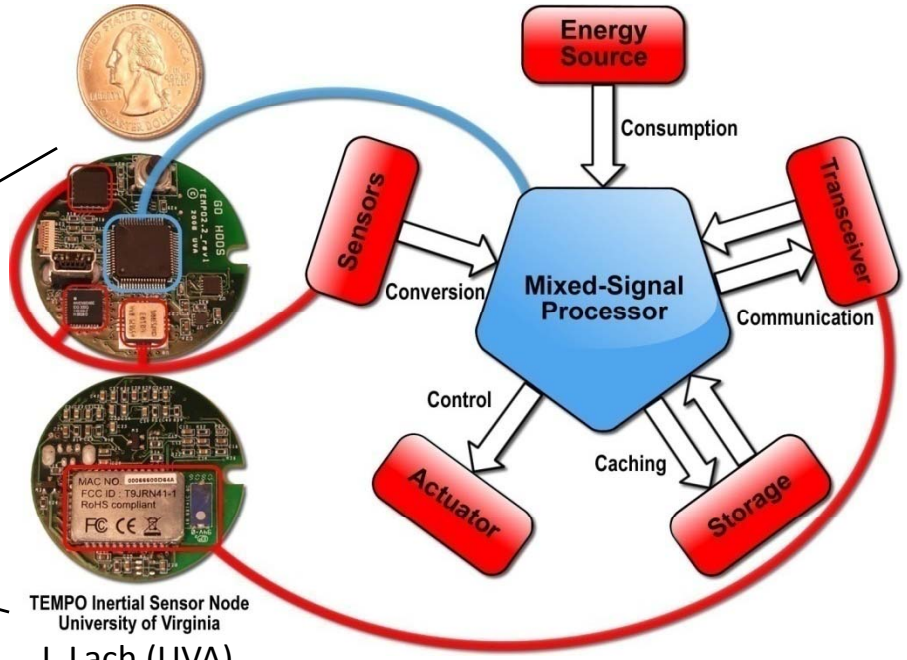


[IEEE Computer, Jan 2009]

BASN Node examples



- Special purpose nodes
- COTS
- Few IC deployments



TEMPO Inertial Sensor Node
University of Virginia
J. Lach (UVA)

BASNs – NOT just another WSN

	Multipurpose Wireless Sensor Networks (WSNs)	Wearable Body Area Sensor Networks (BASNs)
Network Scale	10s to 1000s of nodes over wide area; multi-hop communication; ad hoc placement	<10 nodes; 1 hop communication; fixed placement; each node critical
Lifetime	Very long; rely on many nodes to bypass dead nodes	Mid to long; more conducive to periodic recharging
Form factor	Less crucial constraint	Must be unobtrusive; small, light, “invisible”
Security	Physical access to nodes defeats many security protocols	Nodes carry health info, so secure transmission is critical

[IEEE Computer, Jan 2009]

Gap and Opportunity

- Existing COTS BASNs energy inefficient
  - Lifetimes of <24 hours
- Need custom solutions
- Sub-threshold circuits are ideal technology, but what about other factors?

- How can we best leverage sub-threshold?

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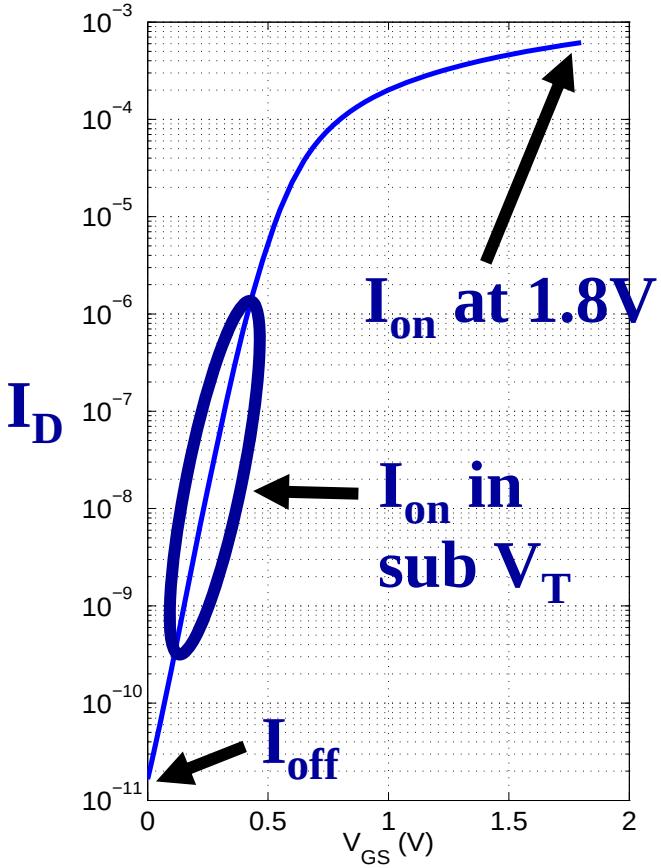
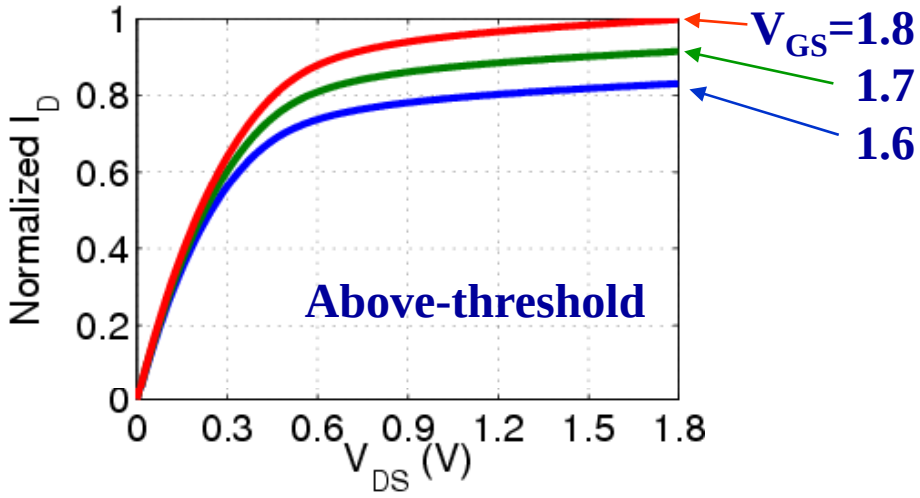
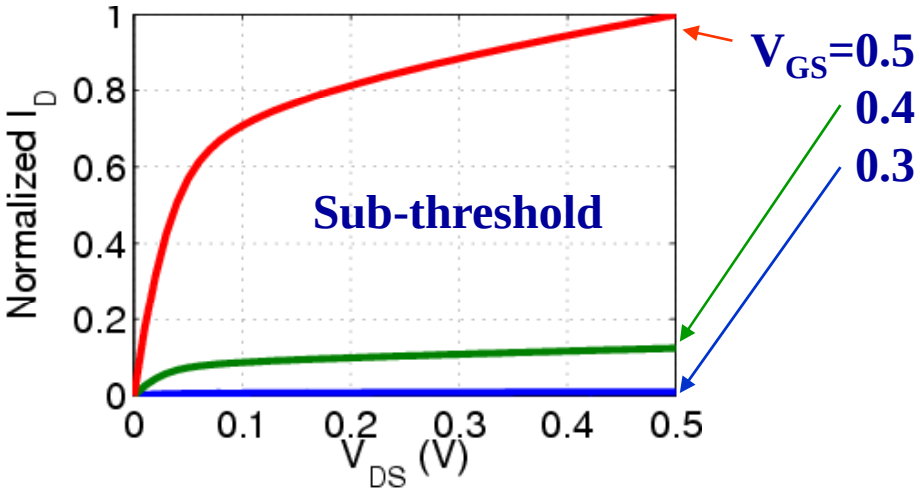
Sub-threshold Operation

- Sub-threshold logic operates with $V_{DD} < V_T$
- Both *on* and *off* current are sub-threshold "leakage"

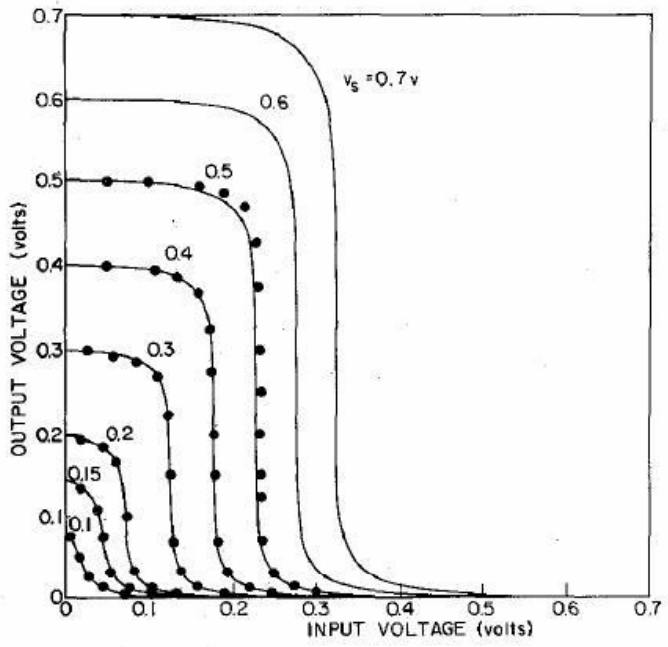






Sub-Threshold Digital Circuits Overview

- 1972: Sub-threshold theorized for minimum V_{DD} operation (*Swanson & Meindl, JSSC*)
- Major challenges:
  - Reduced Ion/Ioff
  - Variation (local V_T variation, especially)
- Last 5 years: sub-threshold demos
  - Logic
  - Memory (SRAM)
  - Micro-processors



Swanson & Meindl, 1972

Benefits of Sub-threshold

- Sub-threshold benefits: V_{DD} from [1.8,1.0]V to [0.4,0.2]V

Leakage Power Decreases: Power = V_{DD} I_{off}

V_{DD} goes down: 2.5X to 9X

DIBL reduces $I_{sub\text{-}threshold}$: 2X to 10X

I_{gate} and I_{GIDL} become negligible

Pleak: 5X to 90X

Energy Consumption Decreases

$E_{active} = CV_{DD}^2$

E_{total}/operation minimized in sub-V_T

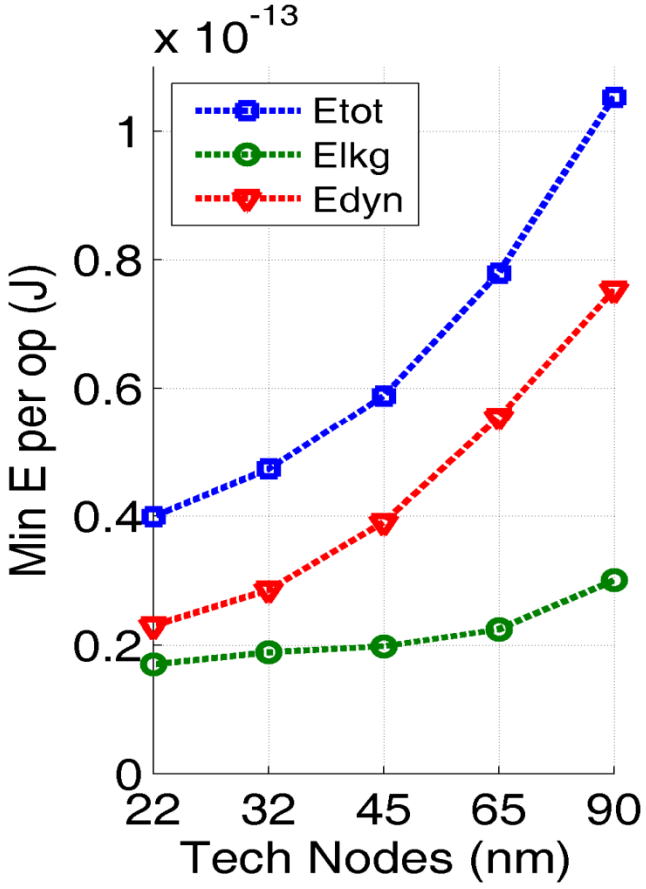
Reliability Effects Improve

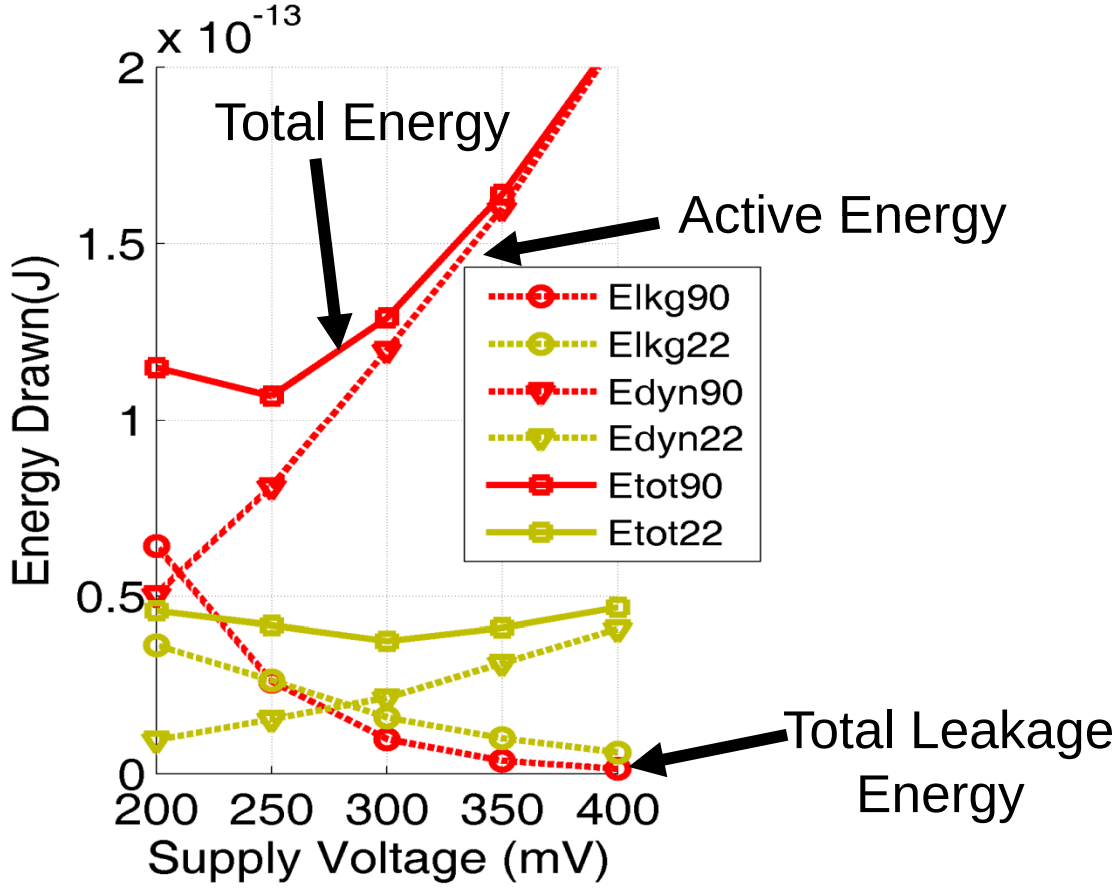
NBTI, EM, TDDB

Main Limitation: Slow Speed, but OK for BASN

Sub-V_T Minimum Energy Operation

$$E_{Total} = \underbrace{C_{eff} V_{DD}^2} + \underbrace{W_{eff} L_{DP} KC_g V_{DD}^2 e^{-\frac{V_{DD}}{nV_{th}}}} = V_{DD}^2 \left(C_{eff} + W_{eff} KC_g L_{DP} e^{-\frac{V_{DD}}{nV_{th}}} \right)$$





Assumes the circuit is always active

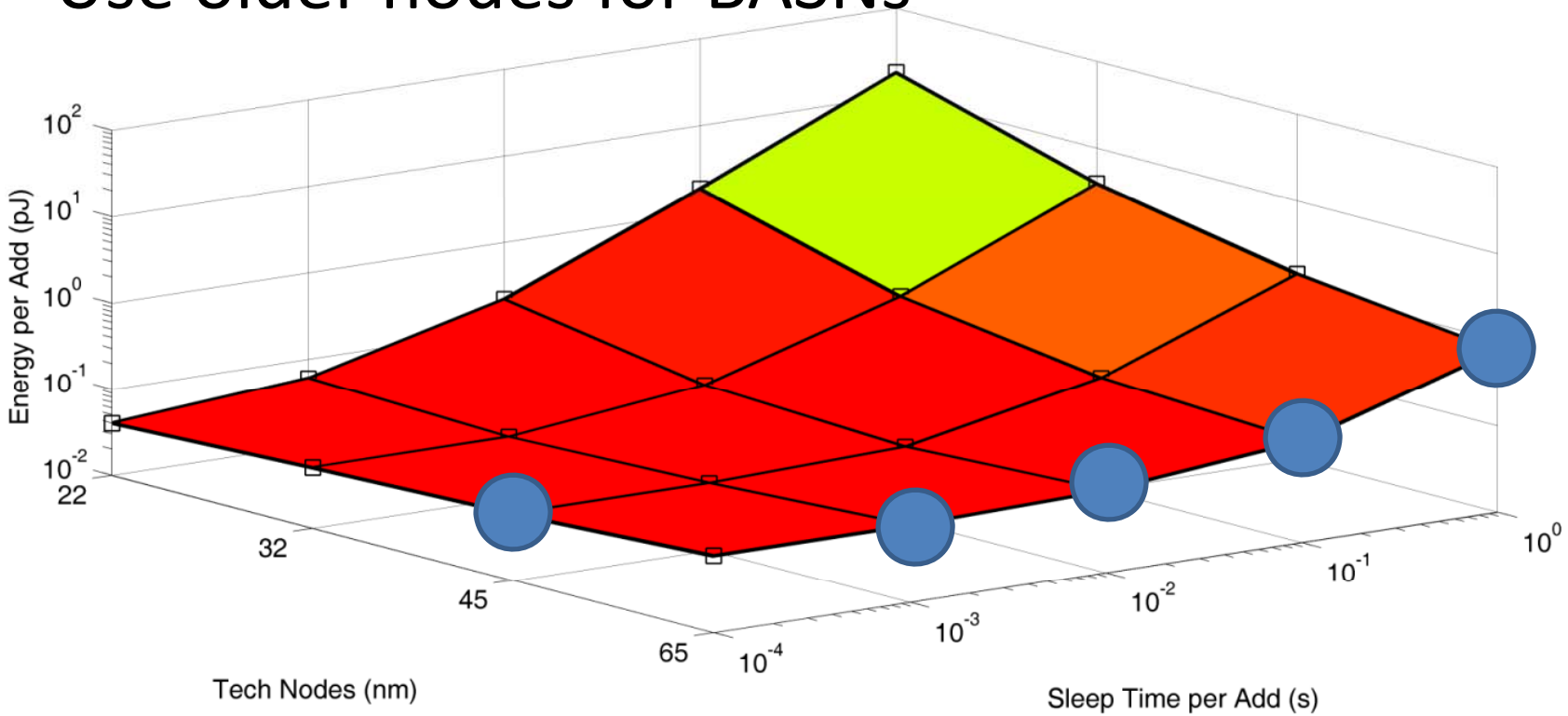
Technology Selection for BASNs

- Sleep periods are likely in BASNs
- Even with power gating (e.g. assume 10X reduction here), sleep energy contributes substantially to overall energy

PTM (nm)	**T_{sleep}=0**	**T_{on} + T_{sleep} = 0.1ms**	**T_{on} + T_{sleep} = 1ms**
90	107	107	129
65	77.7	85.5	147
45	58.4	69.8	193
32	47.2	84.0	428
22	41.2	222	1860

Technology Selection for BASNs

- Assuming 1000X reduction in sleep power, older technologies better for any substantial
- Use older nodes for BASNs



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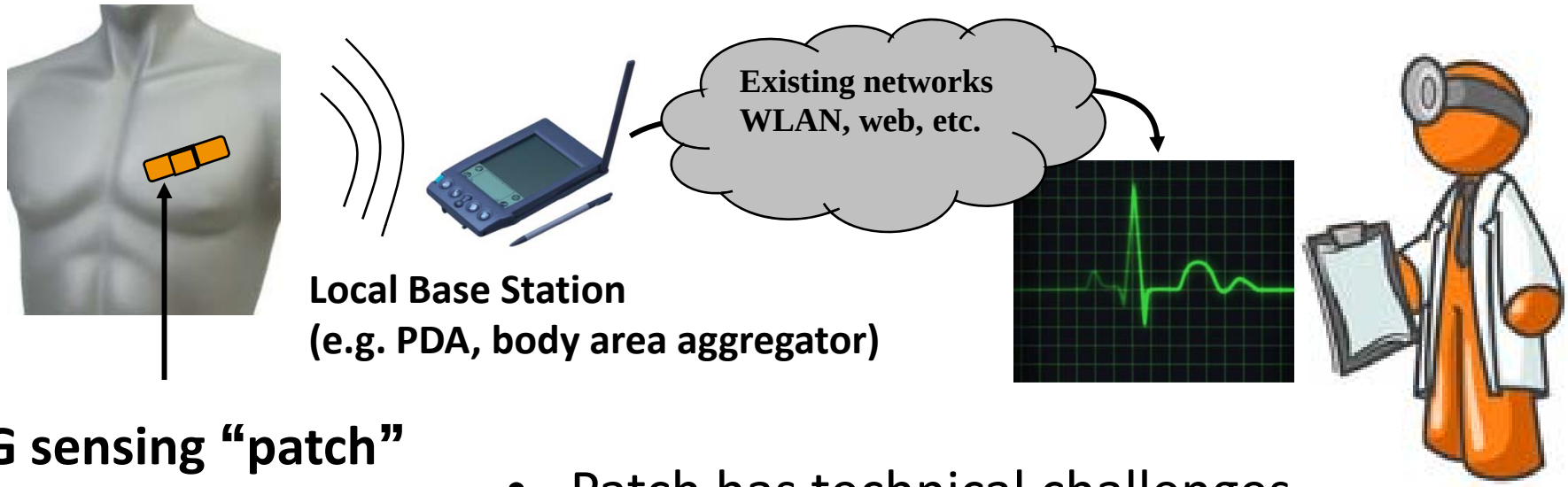
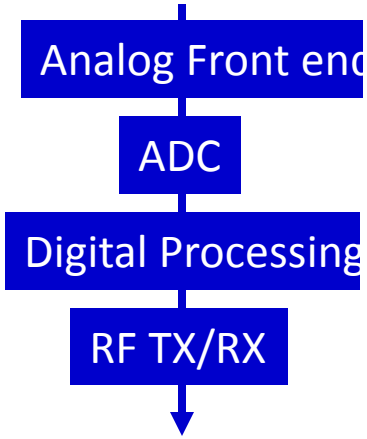
Example Wireless Electrocardiogram (ECG) System

- Medical goals – ambulatory ECG; identify cardiac arrhythmias, etc.
  - Doctor look at ECG waveform
- Technical Goal – build a BASN node to see system level issues; how to leverage sub-threshold circuits most effectively

ECG Monitoring System

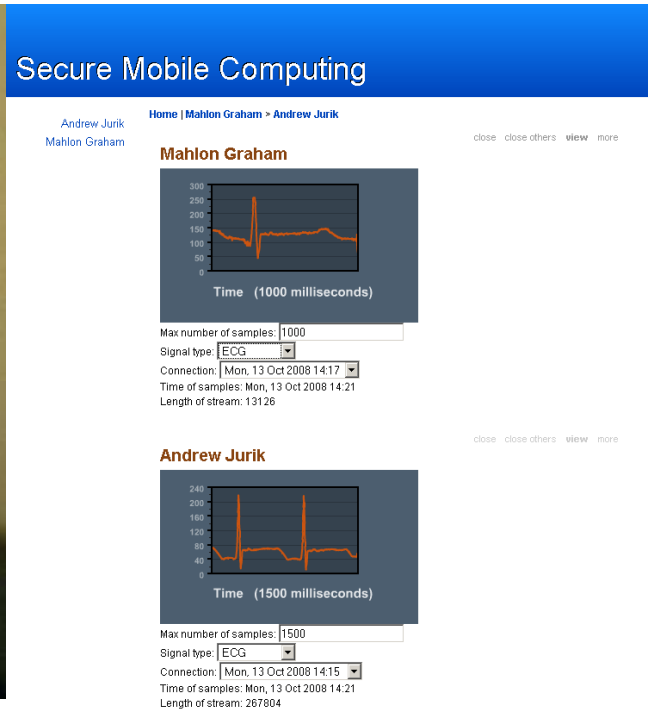


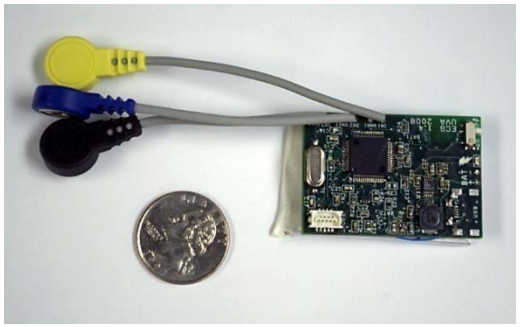
ECG sensing "patch"



- Patch has technical challenges
  - Long lifetime requirement
  - Small form factor, unobtrusive, comfortable
- Sub-threshold design !
  - Use sub-V_T for digital parts, right?

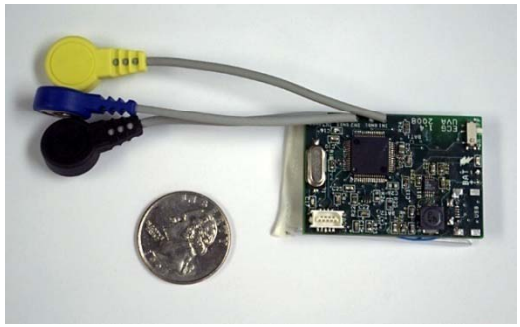
Discrete Prototype: Wireless ECG





- Wireless ECG patch with COTS parts
- Base station client
- Secure web service
- Multiple user support

Discrete Prototype



- **Streaming ECG data:**
  - **~94mW**
  - **93% in RF (Bluetooth)**
  - **6% in analog (Frontend amp & ADC)**
  - **1% in digital computation (MSP430)**

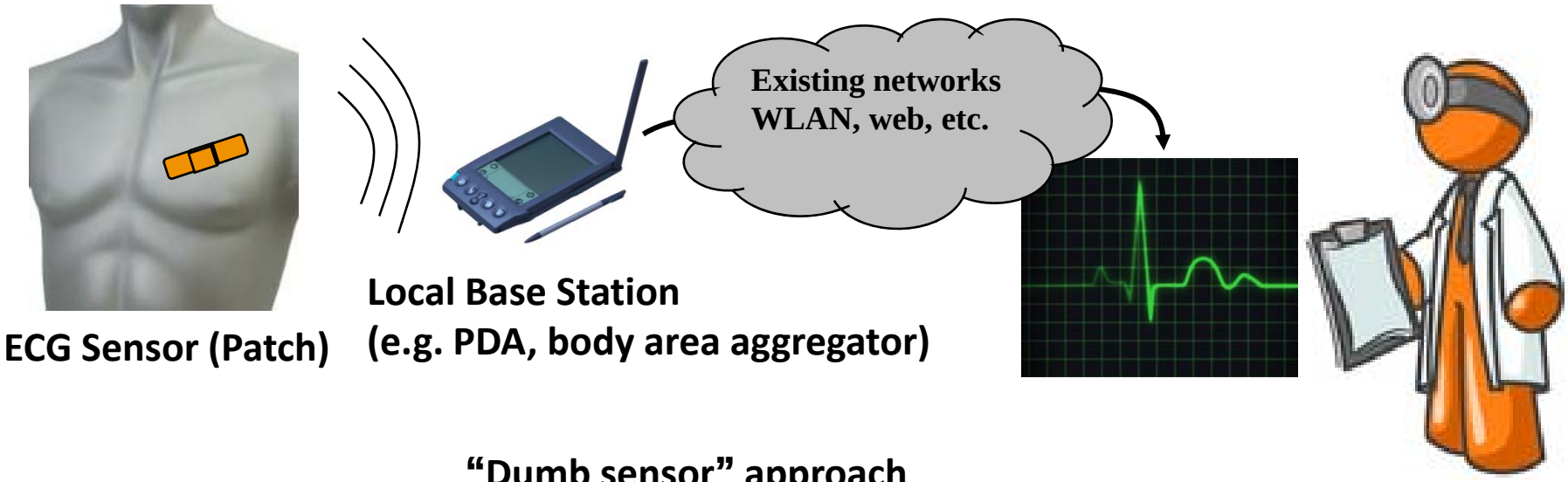
- **Data transmission is the problem**
- **Sub-V_T processor would affect only 1% of system power**
- **We can make the digital consume ~0 of the system power – can "free" digital help?**
  - **Local goals (e.g. Patch lifetime)**
  - **System goals (e.g. Information collection / fidelity)**

Revisit the ECG system: What are the goals?

- Goals of ECG Monitoring for the wearer:
  - Goal 1) Heart rate analysis
- Goals of ECG Monitoring for the wearer's physician(s):
  - Goal 1) Heart rate analysis
  - Goal 2) Identify / Monitor cardio arrhythmias
  - Goal 3) View full ECG of arrhythmia events

- How to achieve Goal 1?
  - Need to extract heart rate from ECG signal
  - Could use digital processing
- How to achieve Goals 2 and 3?
  - Talk to some M.D.s → It turns out that we can detect most arrhythmias of interest by processing heart rate
  - So, meet Goal 1 always and only send ECG when needed

System Partitioning: How to meet the goals?



ECG Sensor (Patch)

Local Base Station
(e.g. PDA, body area aggregator)

“Dumb sensor” approach

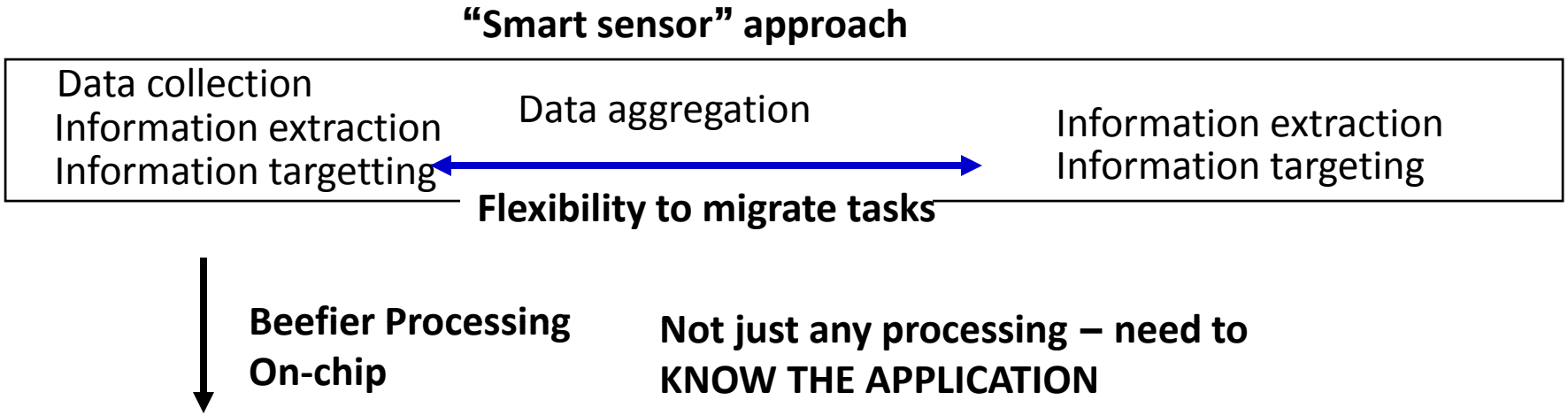
Data collection	Data aggregation	Information extraction Information targeting

“Smart sensor” approach

Data collection Information extraction Information targetting	Data aggregation	Information extraction Information targeting

Flexibility to migrate tasks

System Partitioning: How to meet the goals?



- Heart rate detection on chip (e.g. modified Pan-Tompkins algorithm)
  - **~430X reduction in wireless data rate**
- Compression
  - **Additional 2X to 10X+ reduction**
- On-board arrhythmia detection
  - **Data rate approaches 0; bursts of high activity during events**
- (Need a radio / protocol that scales energy with data rate)

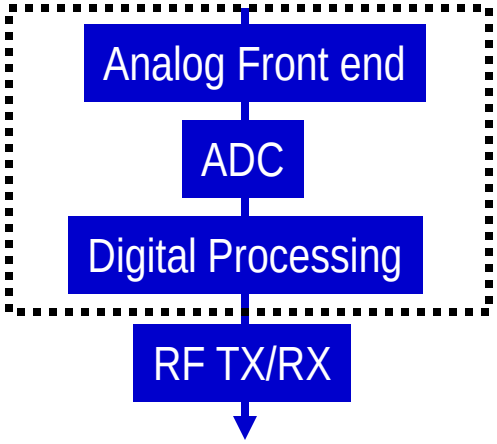
Conclusions

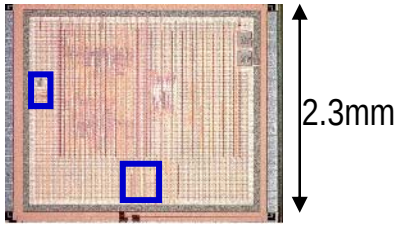
- Wireless transmission is a power hog
- Need energy-scalable radio
- Processing on board can help
  - Smart node, not dumb
- Opportunity for sub-threshold
  - Cross hierarchy / system aware design

- What comes next?

Mixed Signal ECG System on Chip

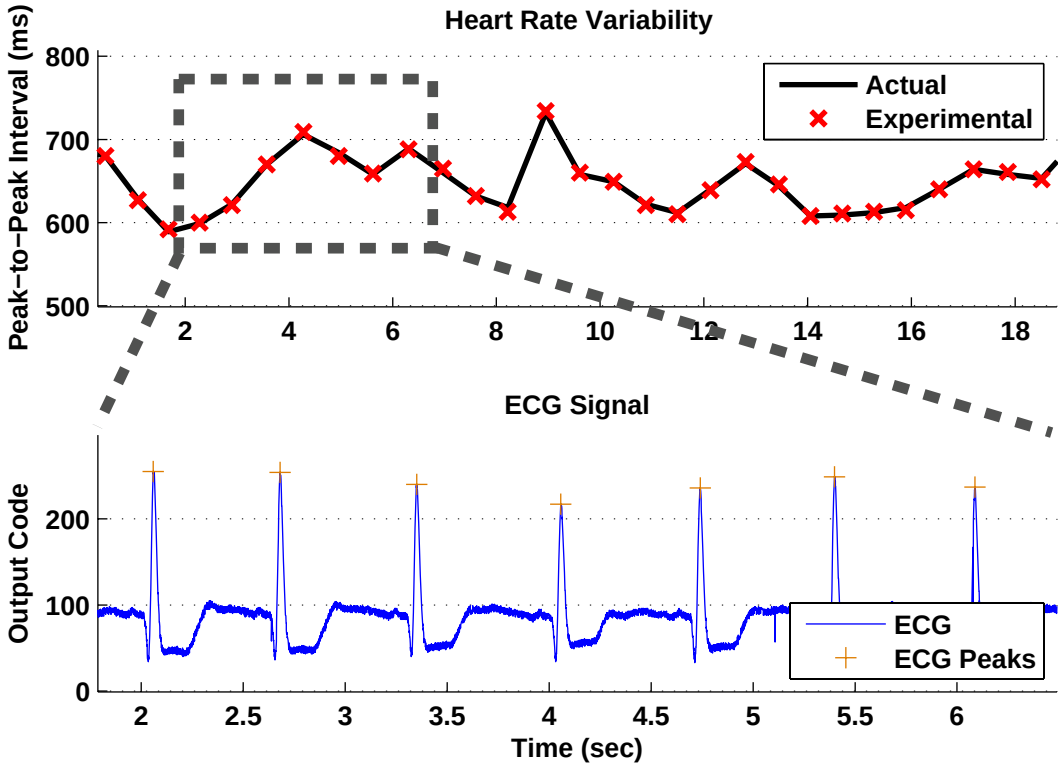
ECG sensing "patch"





Analog frontend

uC
1.5pJ/instr



Leverage Sub-V_T processing by re-partitioning tasks at system level

Heart rate computation cuts wireless data rate by 500X

[to appear at Symp. VLSI Circuits]

Thank you

- Any questions?