# Sub-threshold Sense Amplifier Compensation Using Auto-zeroing Circuitry

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**Voltage offset in SRAM sense amplifiers due to variability causes increased power consumption and degraded performance. The effect is more dominant in the sub-threshold region. In this paper, we propose a circuit that reduces the sense amp offset using an auto-zeroing scheme with automatic temperature, voltage, and aging tracking.**

***Offset Compensation, SRAM, Sense Amplifier, and Auto-zeroing.***

## I. Introduction

Several attempts have been made before to tackle the problem of offset voltage in sense amplifiers (SAs) including redundancy [4], transistor upsizing [3] and digitally controlled compensation [2]. Our approach to eliminating offset is a digital auto-zeroing (DAZ) scheme inspired by analog amplifier offset correction. The main advantages of the approach are the near-zero offset after cancellation and the automatic temperature, voltage, and aging tracking achievable using a repeated offset calibration phase, which makes the design useful in the sub-threshold region due to the high offset voltage sensitivity to supply voltage and temperature variations [1][5].

## II. Mismatch Compensation using Auto-Zeroing Circuitry

Our auto-zeroing scheme uses a split-phase clock and charge pump feedback circuit. Figure 1 shows a conventional latch-based sense amp with PMOS inputs (e.g. to support near-$V_{SS}$ sensing on a low swing bus). Figure 2 shows the auto-zeroing circuit attached to the sense amp. The same scheme can apply to a SA with NMOS inputs in an SRAM. The charge pump circuit is shown in Figure 3. ENI and ENO are the input voltage differential and offset tuning phases respectively. ER1 and ER2 are reset phases. During ER1, a zero differential input is applied to the sense amp. The ENO phase then occurs, and the SA resolves based on its intrinsic offset. The sense amp output is fed to the charge pump circuit that charges the capacitor, Cp, up or down. During ER2, the differential input is applied to the sense amp. ENI then occurs, and the SA resolves based on the differential input. Note that phases ENR1 and ENO can be omitted or included based on how often re-calibration is needed. Transistors MC1 and MC2 control the drive strength of the right side of the sense amp to compensate for the offset. The charge pump controls the drive current in both transistors to equalize the strength of the SA right and left sides to reduce the offset. The offset is compensated with minimal capacitive loading at the output and is independent of input DC bias ($V_{INDC}$).

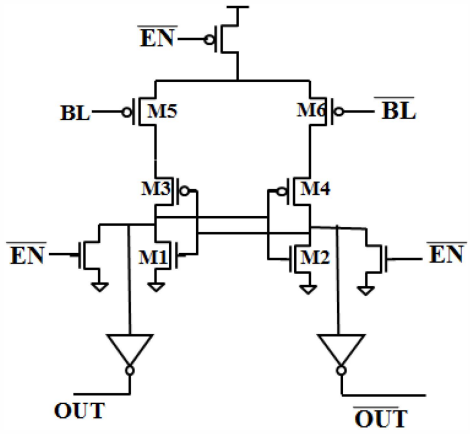


Figure1. Latch-based sense amp for near-$V_{SS}$ inputs.

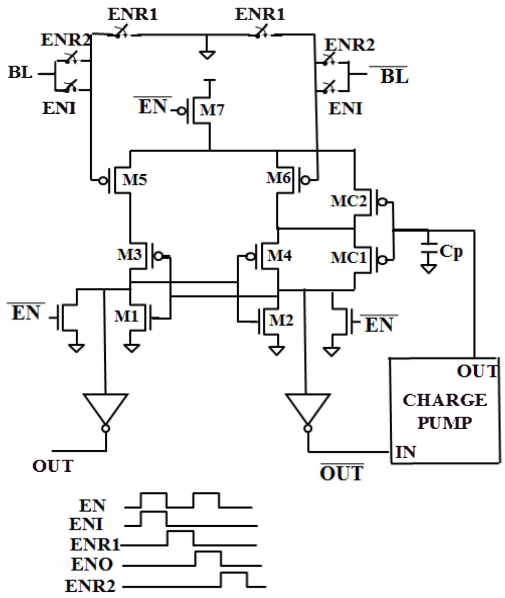


Figure 2. Auto-zeroing circuit attached to the sense amp

## III. Voltage, Temperature, and Aging Tracking

To demonstrate temperature, voltage, and aging tracking, the offset voltage that remains after compensation is calculated for various voltages and temperatures as shown in Figure 4a. Simulations in a commercial 45nm process show that the circuit maintains a constant offset across temperature. The

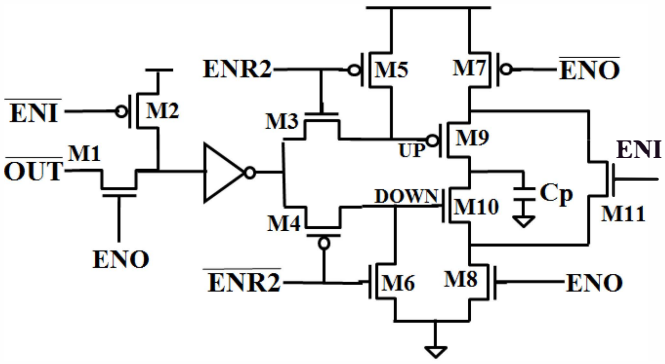


Figure 3. Charge pump circuit for adjusting the voltage on Cp

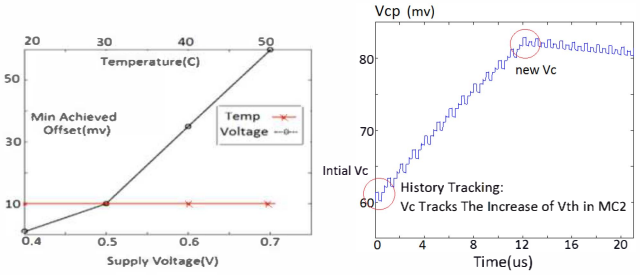


Figure 4 a. Voltage and temperature tracking. b. Aging tracking

accuracy of voltage tracking depends on the supply voltage. Higher supply voltage causes more charge to be pumped to Cp during each offset calibration cycle, and this larger change in charge leads to a coarser resolution, as Figure 4a illustrates.

The auto-zeroing scheme also has the ability to compensate for any changes in device characteristics after circuit deployment. One common cause for such changes is effective threshold voltage shifting due to BTI, hot carrier injection, or other aging effects. To demonstrate how this circuit can compensate for such changes, Figure 4b shows the capacitor voltage after an abrupt increase in the threshold voltage of MC2. The charge pump boosts the voltage on Cp to decrease the drive strength of MC2 in response and rapidly restores the compensated offset voltage.

## IV. Offset Tuning

We define settling time as the difference between the time when the zero differential-input is first applied and the time when the voltage of the output capacitor settles as shown in Figure 5. Changing the size of the output capacitor (Cp) affects the amount of charge added during the offset compensation phase (ENO) and so controls both the offset and the settling time. Figure 6 demonstrates the trade-off between accuracy (min achieved offset) and settling time using different values of output capacitors.

## V. Power Consumption

The main contribution to the power consumption comes from the continuous calibration. Minimizing the period of the

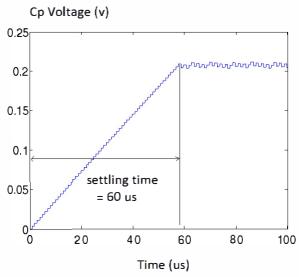


Figure 5. Settling time simulation

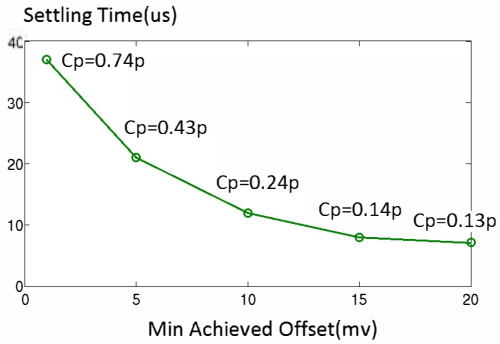


Figure 6. Min achieved offset vs. settling time for different values of output capacitor (Cp, value in F)

calibration phase relative to the input phase decreases the power consumed but is limited by the leakage at the output capacitor (Cp). The leakage of Cp also degrades the settling time. Shorting the output virtual nodes of the charge pump through M11 can decrease the leakage by reducing $V_{DS}$ of the switches and improve settling time as shown in Figure 7.

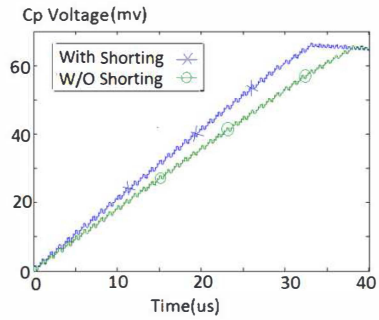


Figure 7. Voltage on Cp with and without shorting the virtual supply nodes of the charge pump

The switching power can also be decreased by strengthening M9 in the charge pump circuit relative to M10 to avoid the continuous toggling of the sense amp output during offset compensation phase (ENO) after settling as shown in Figure 8. Strengthening M9 has the downside effect of increasing the settling time when Cp is moving to lower voltages; the time Cp takes to discharge will increase. However the compensation usually starts with zero-initial voltage on the capacitor Cp, that makes the settling time mostly dependent on the charging rate.

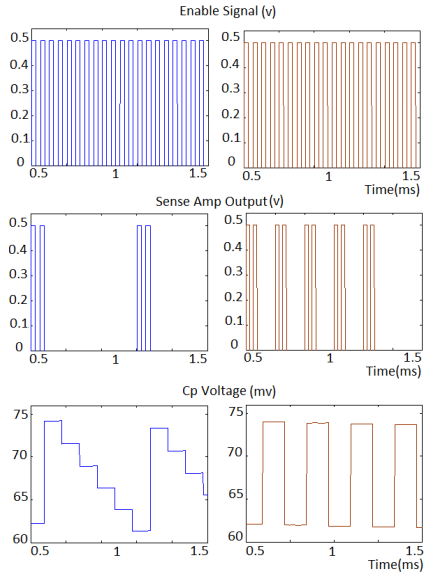


Figure 8. Strengthening the pull up transistor of the charge pump (left column of sims) reduces the rate at which the SA output switches high relative to equal strength devices (right column). This reduces power consumption.

## VI. Offset Sensitivity

The sensitivity of the offset compensation depends on the split phases, charge pump circuit, and the output capacitance. The accuracy of the split phases has the dominant influence on the resolution. A small overlap between ENO and ENR2 phases can dramatically degrade the accuracy by connecting M1 and M2 to the supply rails during charging. That leads to a significant increase in the charge pump rate degrading the accuracy as shown in Figure 9b, where the min achieved offset is plotted against the error in split phase timing, measured as the percentage of time overlap between ENO and ENR2. The scheme is also sensitive to variations in the M9 and M10 transistors in the charge pump circuit. They are responsible for charging/discharging Cp, and so the one with more drive strength determines the final offset value. Figure 9a shows the sensitivity of the offset voltage to the output capacitance Cp.

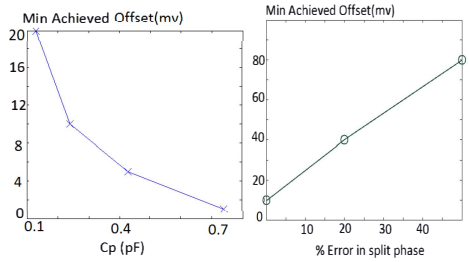


Figure 9 a. offset voltage sensitivity to output capacitance b. sensitivity to split phases

The offset voltage is also sensitive to the frequency of the split phase. The increase in the split phase frequency increases the enable signal switching and degrades the compensated offset voltage.

## VII. 45nm Test Chip Measurements

A test chip fabricated in 45nm technology is used to verify the scheme. The chip contains one regular SA array for benchmarking and another array that uses the auto-zeroing circuit, with Cp=0.74pF. Split phase of 1MHz frequency is supplied to the auto-zeroing circuit. Fig 10 shows the measured offset distribution of both banks. The auto-zeroing circuit limited the absolute average value of the offset to 1mV, which coincides with the simulation prediction from Figure 6.

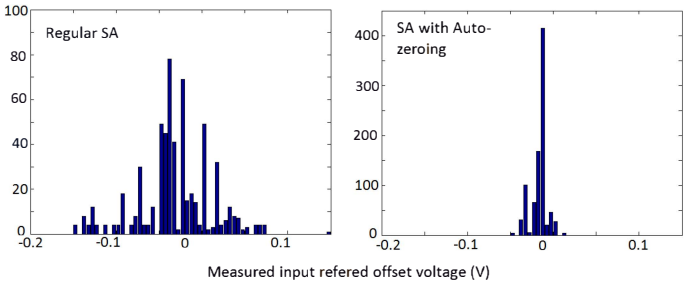


Figure 10 Measured offset voltage distribution a. regular SA b. SA with auto-zeroing circuitry

To verify the offset sensitivity to split phases, the offset is measured for different split phase frequencies. Figure 11 shows the offset voltage values for different split phase frequency.

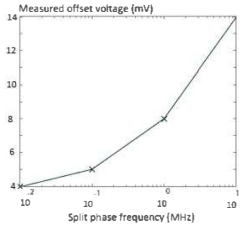


Figure 11 Measured offset voltage vs. split phase frequency

## VIII. Conclusion

We proposed a circuit that is capable of improving sense-amp offset to near zero, which is valuable for sub-threshold operation due to the heightened effect of mismatch. Simulations of the design (0.5V, 1 MHz) show a compensated offset voltage of 1mV, settling time of 37us, and total power consumption of 12nW. Measurements from a test chip fabricated in 45nm technology showed the circuit ability to improve the offset to 1mV using 1MHz split phase frequency and 0.74pF Cp capacitance.

## IX. References

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