SRAM Sense Amplifier Offset Cancellation Using BTI Stress

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Introduction

Device variability in modern processes has become a major concern in SRAM design leading to degradation of both performance and yield. Variation induced offset in the sense amplifiers (SA) requires a larger bit-line differential, which slows down SRAM access times.

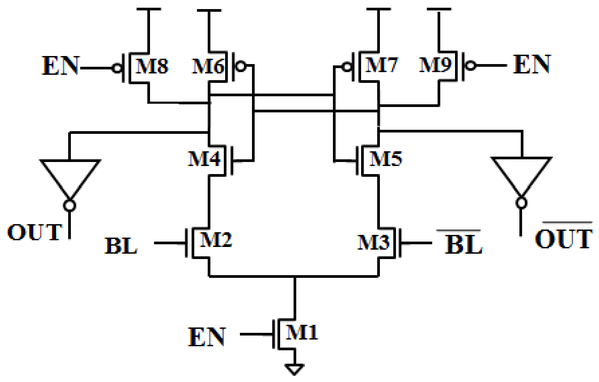
Several attempts have been made before to tackle the problem of offset voltage in sense amps including

- Redundancy
- Transistor upsizing
- Digital compensation

- We propose a post fabrication technique that takes advantage of the typically detrimental bias temperature instability (BTI) aging effect to improve SRAM sense amplifier offset.
- Unlike the previously mentioned methods, our approach is not a design time method. Instead, it can be applied after fabrication (e.g. during burn-in, power up, or built-in-self-test) and used in addition to other compensation techniques as an initial step to reduce the offset variations.

BTI Compensation

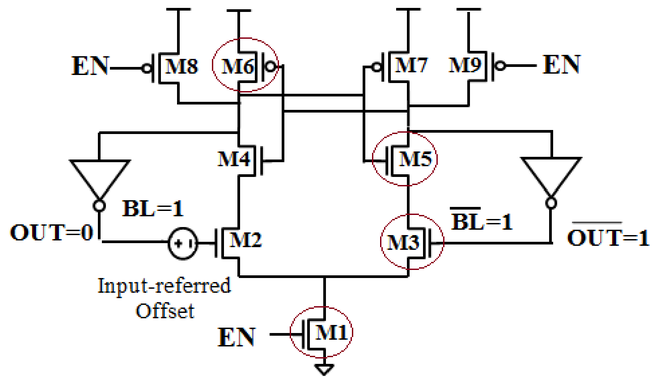
- We can exploit BTI to combat random variation (i.e. mismatch) by applying different stress conditions for different transistors.
- For a sense amp with mismatch, when we only stress transistors with higher variation induced strength, the BTI induced change can compensate for mismatch and thus contribute to balancing the sense amp.
- We illustrate the scheme on a latch based sense amp shown below



Latch-based Sense Amp

Example

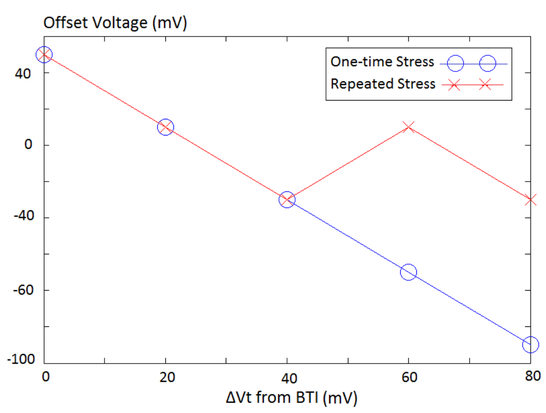
- Consider a case where M2 has higher threshold voltage than M3. If a zero-differential input is applied to the SA, the output node “OUT” will be driven to 0. M1, M2, M3, M5 and M6 will be in strong inversion indicated by the red circles and will be affected by the BTI stress during compensation, that improves the offset voltage.
- To avoid stressing both the access transistors, the output is fed back to the input to turn off M2 during stressing.



Compensation scheme

Overstress Avoidance

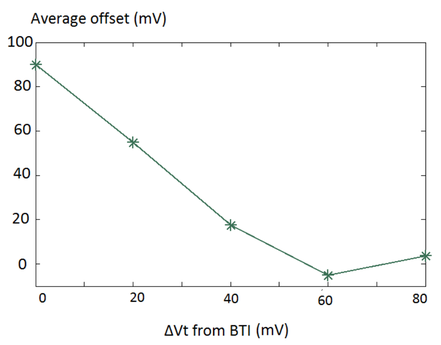
- Applying the stress only one time might cause an extra increase in the threshold voltage that might move sense amplifier offset to the other polarity rather than canceling it.
- One solution to avoid this is to repeatedly reset the SAs during stress. Each reset event will set each SA into a new state based on its new offset value, the stress will act on the correct devices to reduce the offset toward 0.

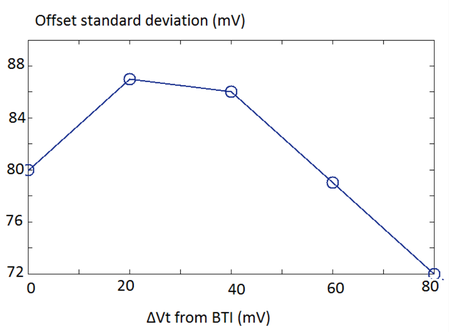


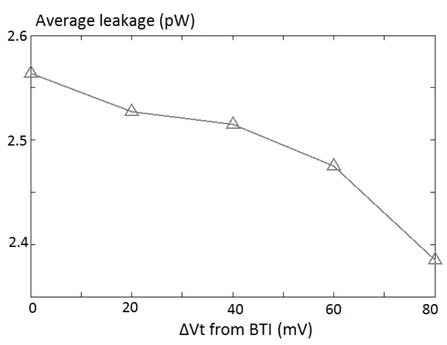
Monte-Carlo Simulation Results

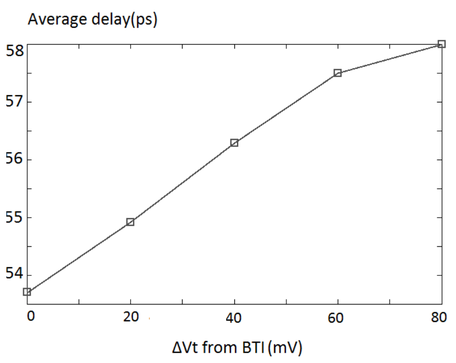
➢ **We performed 80 Monte Carlo simulations in 45nm commercial process of a SA undergoing a stress event with resets after each effective 20mV change in VT. Variations within ±40 mV range are included in the threshold voltage of M2, M3, M4 and M5.**

- Both the average and the standard deviation of the offset voltage decreases but non-linearly with the induced threshold shift and might not be monotonic
- The reason for that is while the BTI stress decreases the offset for some sense amps, it increases it for those with offset voltage close to zero.





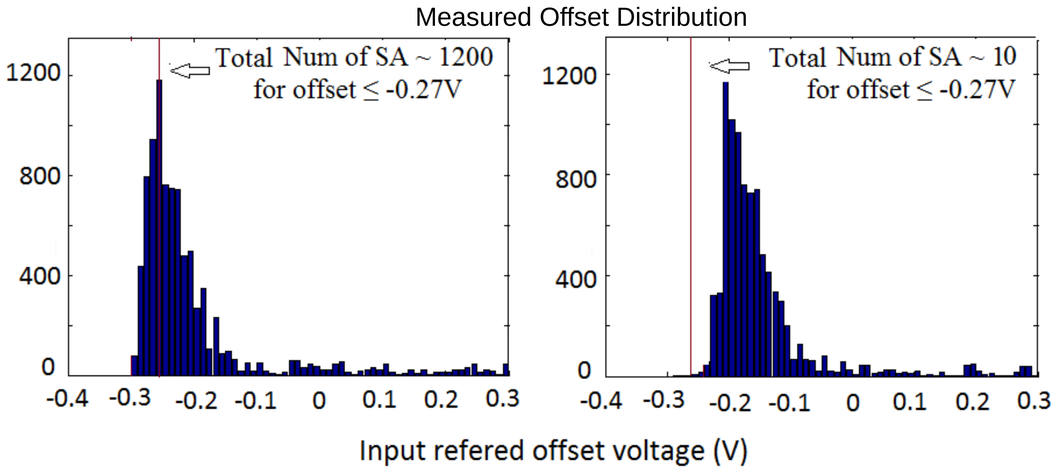


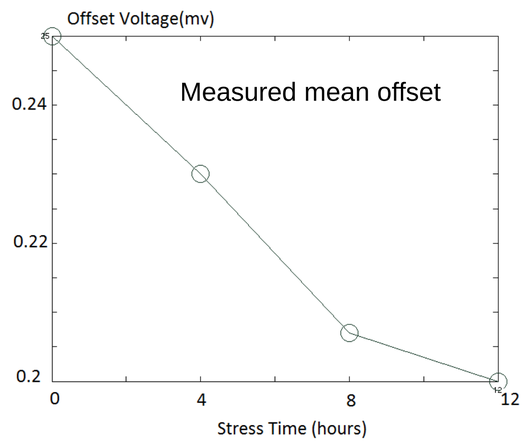


- Increasing the threshold voltage of the stressed devices has the effect of decreasing the leakage power but has the downside of degrading the sense amp speed
- Although the degradation in the speed may be easily compensated by the speedup that is enabled by a reduction in offset of the worst cells.

120nm Chip Measurements

- We applied the proposed scheme to a test chip that contains an array of SAs to demonstrate how BTI can improve offset. The chip is fabricated in 120nm technology and contains 15,360 sense amplifiers arranged in an array to simplify testing.
- To verify the scheme, the chip was stressed at 1.7× of the nominal VDD and 45°C for 12 hours, and measurement of the offset voltage was performed every 4 hours. Due to the structure of the test chip, all SAs had to receive stress in the same direction. This means that the offset should improve for roughly half of the SAs and degrade for the other half.





- The stress has the expected effect of reducing offset in the anticipated direction. By applying the feedback and reset scheme proposed above, we can reduce the offset of all of the SAs.

Conclusion

- We presented a scheme that uses the typically detrimental aging effect to improve the SRAM sense amplifier offset.
- Offset compensation of 50mv was achieved using stress of 1.7× of the nominal VDD and 45°C for 12 hours.
- It can be periodically used through the life time of the chip to offset variation from real-time aging and could be easily integrated with other compensation techniques as an initial step to reduce the offset variations.

Future Work

- Integrate the BTI compensation technique as an initial step to other design-time compensation techniques.