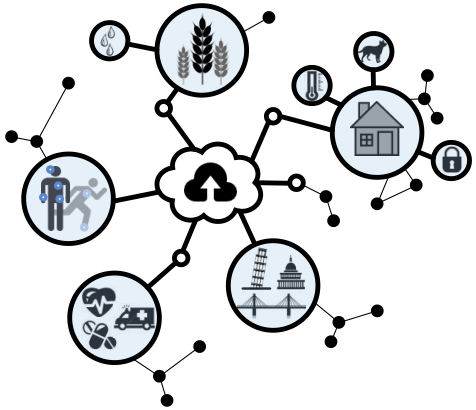
A 256kb 6T Self-Tuning SRAM with Extended 0.38V-1.2V Operating Range using Multiple Read/Write Assists and V_{MIN} Tracking Canary Sensors

*Arijit Banerjee, *Ningxi Liu, *Harsh N. Patel, *Benton H. Calhoun
*Electrical and Computer Engineering
University of Virginia, Charlottesville

** John Poulton, **C. Thomas Gray
** Nvidia, Durham, North Carolina

Motivation

- IoE market rapidly growing



IoE= Internet of Everything

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- IoE market rapidly growing
- Battery recharge and replacement problems

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- Soln: ULP wide-range DVS

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IoE= Internet of Everything, ULP= Ultra-low Power, DVS=Dynamic Voltage Scaling

Bottleneck in ULP wide-V_{DD} Range

- V_{MIN} guard-banding in 6Ts

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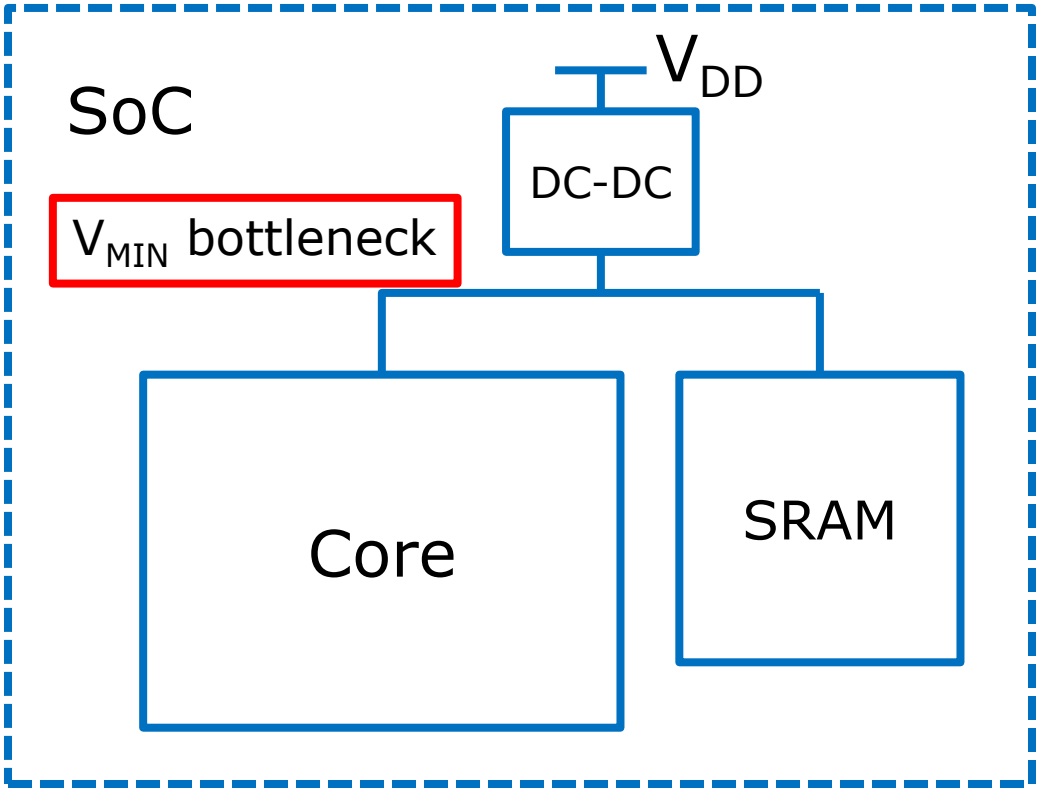
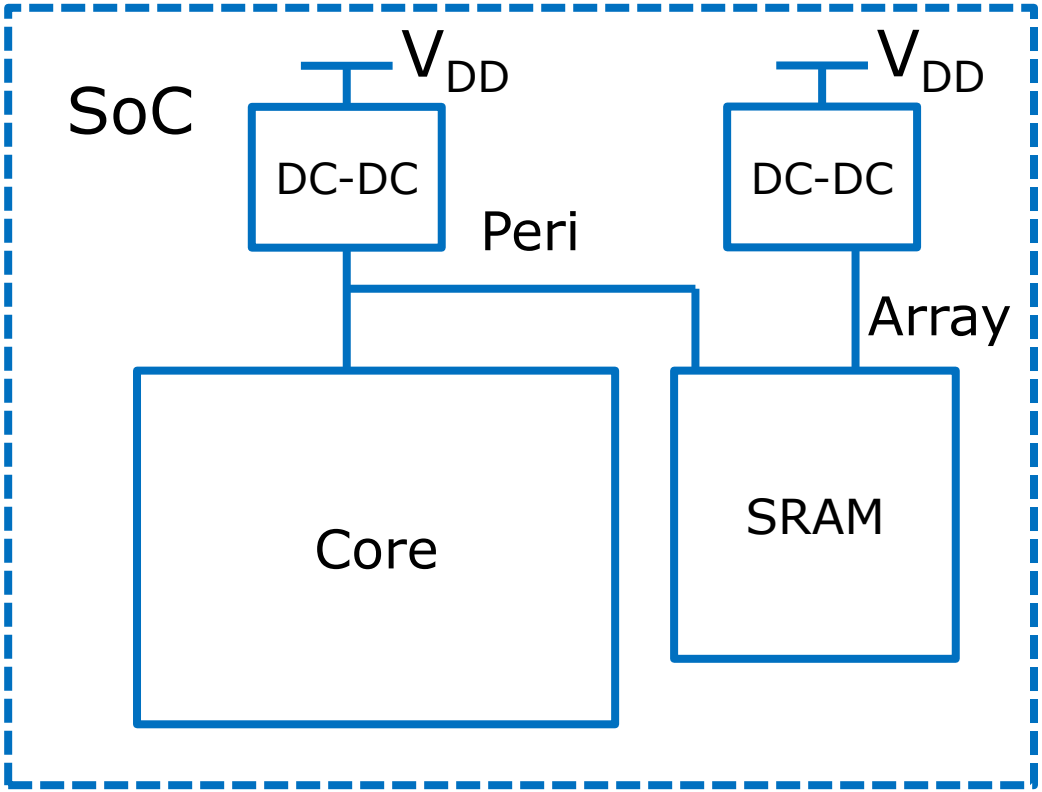
- SRAM V_{MIN} DVS bottleneck



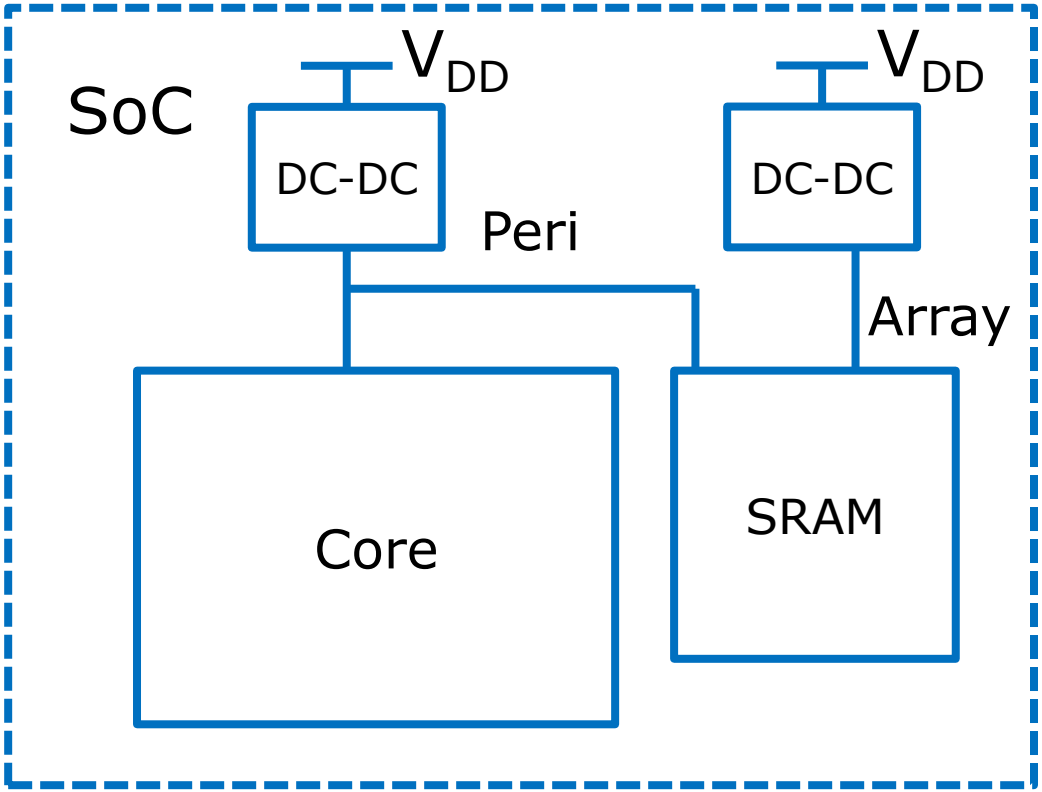
Bottleneck in ULP wide-V_{DD} Range

- V_{MIN} guard-banding in 6Ts
- SRAM V_{MIN} DVS bottleneck
- Dual rail SRAMs SoC level tradeoffs

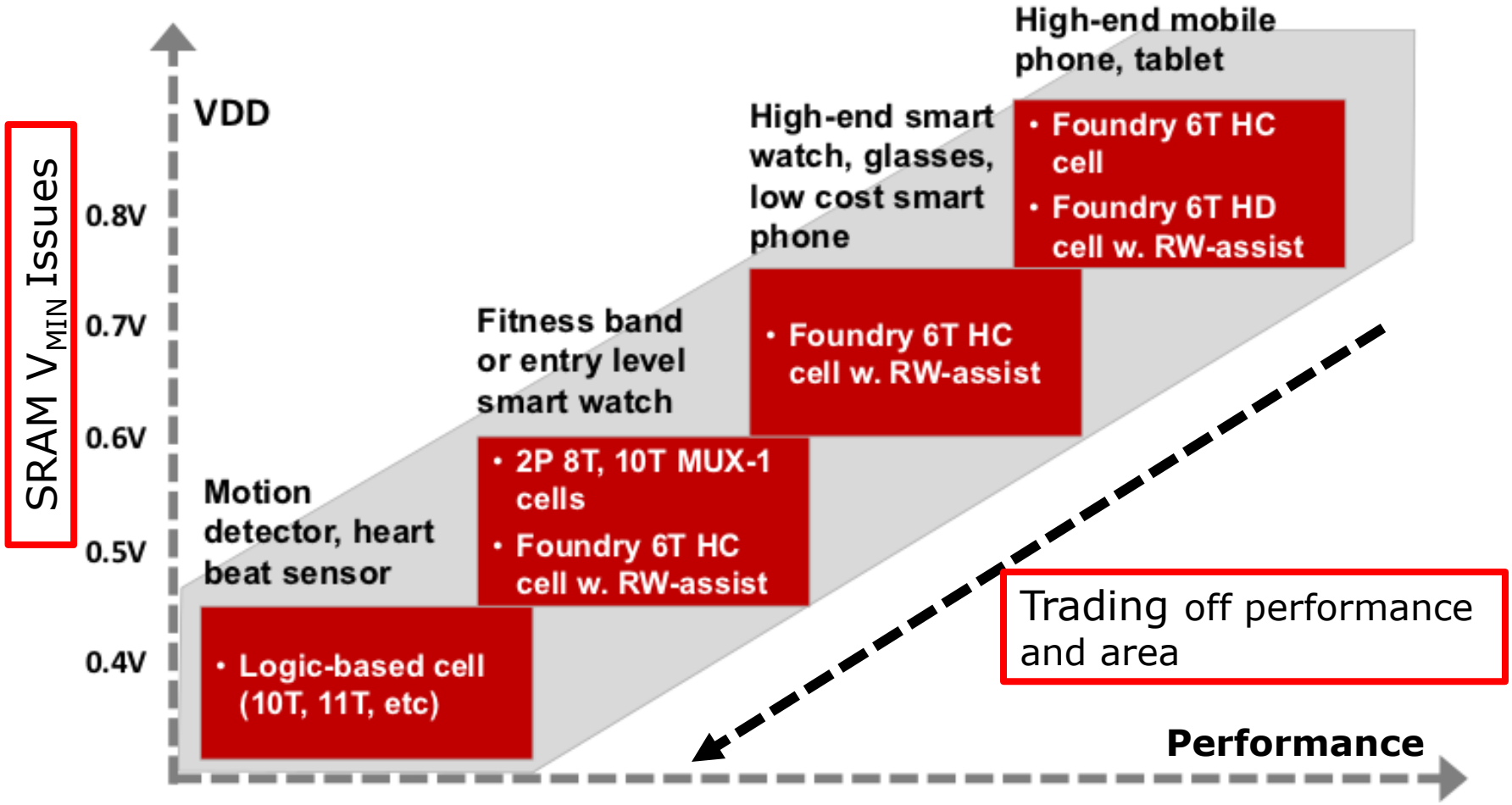


Bottleneck in ULP wide-V_{DD} Range

- V_{MIN} guard-banding in 6Ts
- SRAM V_{MIN} DVS bottleneck
- Dual rail SRAMs SoC level tradeoffs
- Different solutions across applications



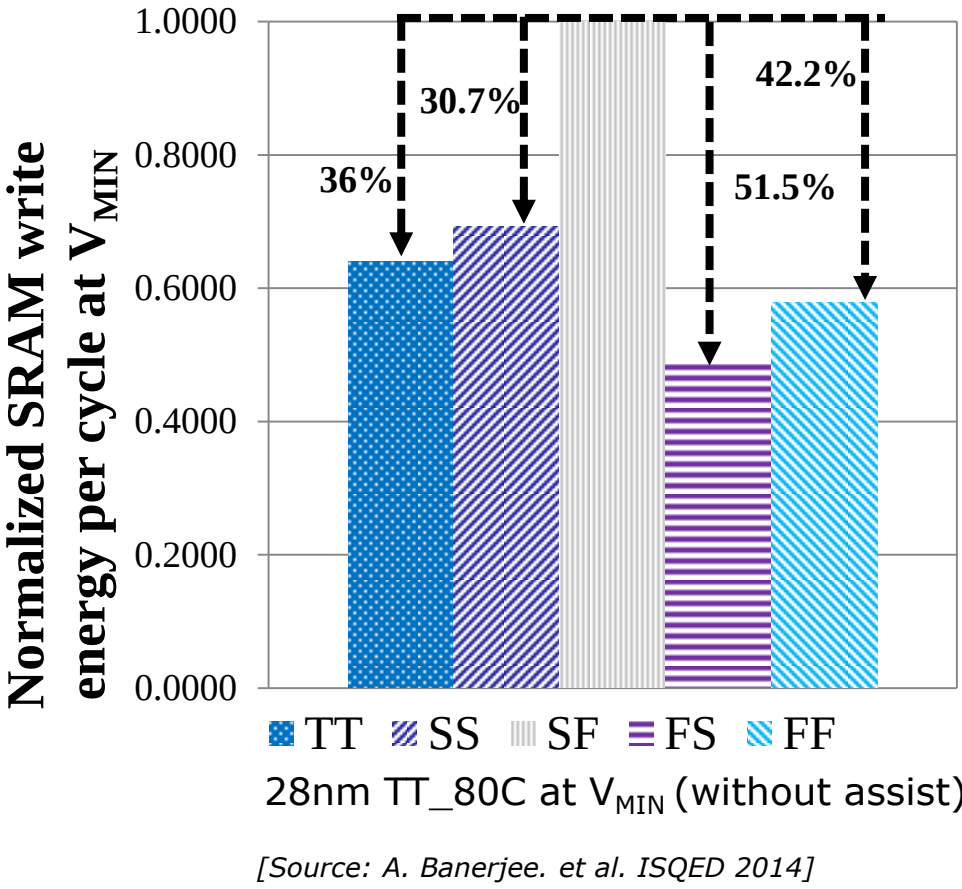
SRAM Solutions for ULP Applications



[Source : Cliff Hou, TSMC, ISSCC 2017]

Scope of 6T SRAM Improvements

- Peripheral assist for V_{MIN} improvement

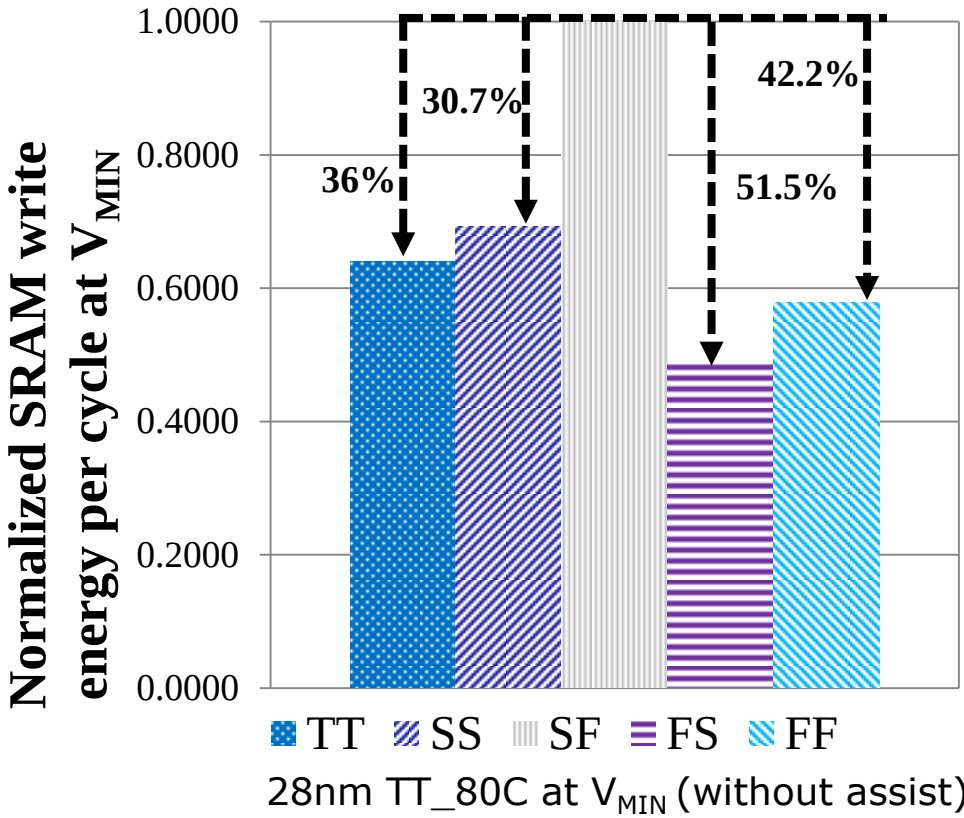


[Source: A. Banerjee. et al. ISQED 2014]

Scope of 6T SRAM Improvements

- Peripheral assist for V_{MIN} improvement
- Lower V_{MIN} guard-band

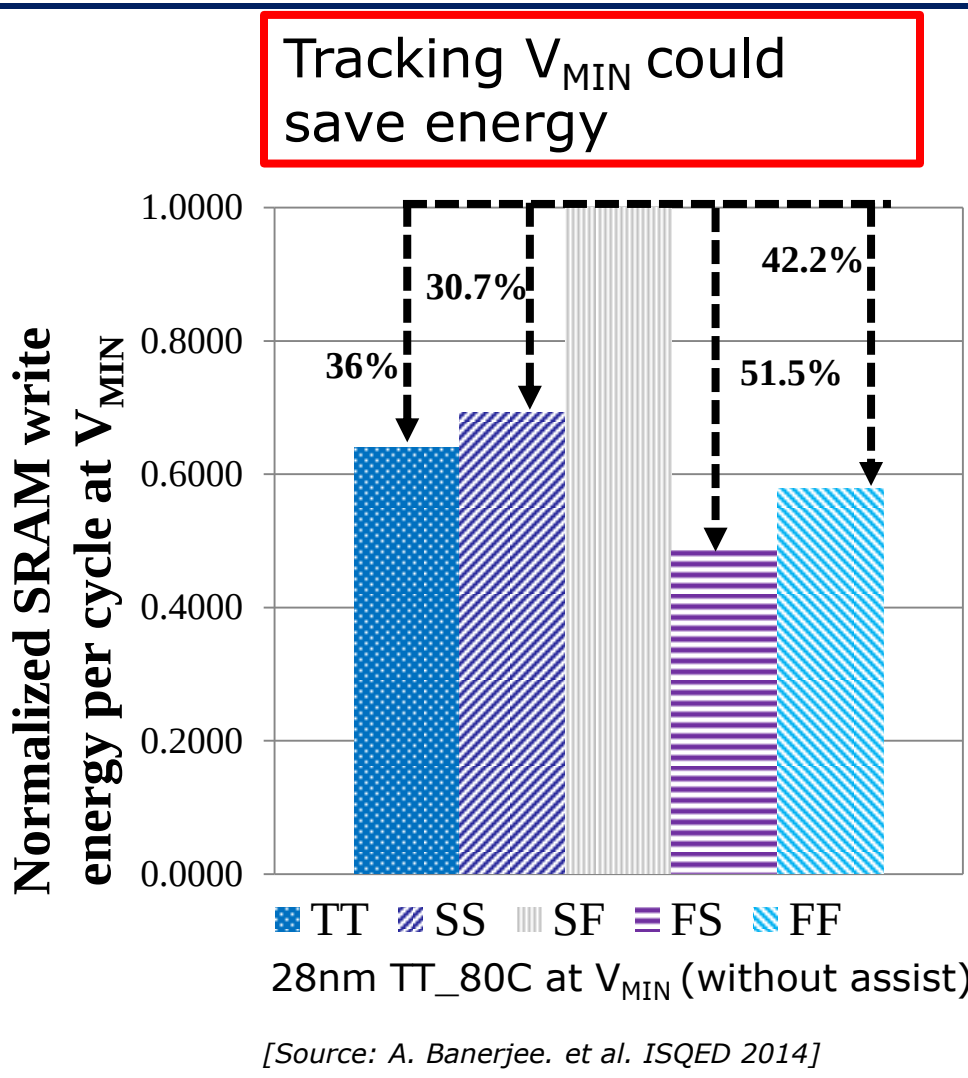
Tracking V_{MIN} could save energy



[Source: A. Banerjee. et al. ISQED 2014]

Scope of 6T SRAM Improvements

- Peripheral assist for V_{MIN} improvement
- Lower V_{MIN} guard-band
- Proposed Solution
  - Combined assist[1] and Canary based V_{MIN} tracking[2] reducing guardbanding



[Source: A. Banerjee. et al. ISQED 2014]

[1E. Karl et al., 2012; 2A. Banerjee et al. 2015]

Agenda

- Canary SRAM Sensors
- Peripheral Assists and Reverse Assists
- 256kb Self-tuning SRAM Architecture
- Experiments & Results
- Comparison
- Conclusion

Canary SRAM Sensors

[Source: http://animalphotos.info/a/topics/animals/birds/canaries/]

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Canary SRAM Sensors

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- Canary SRAM a sensor or detector
- Fails earlier than the population of SRAM bits
- Prior work was in SRAM DRV* tracking[1]

[1] *[J. Wang, and B. H. Calhoun, CICC, 2007], *DRV=Data retention voltage;*

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Peripheral Assists and Reverse Assist

- What is a peripheral assist (PA) in SRAM context?
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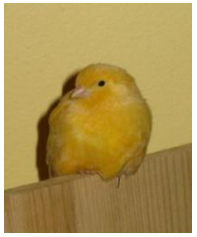
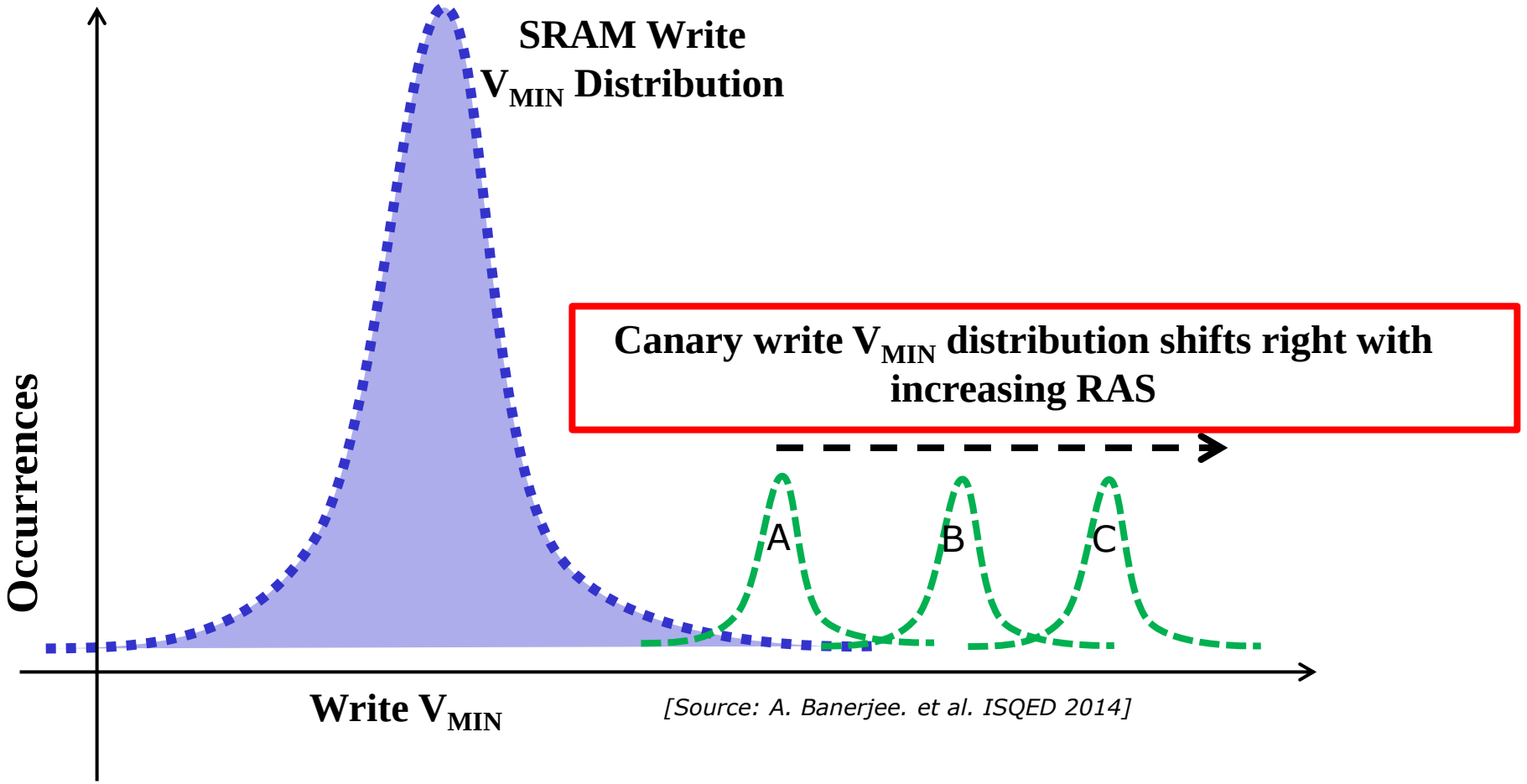
Peripheral Assists and Reverse Assist

- What is a peripheral assist (PA) in SRAM context?
  - An auxiliary circuit that improve read/write-ability
- What is reverse assist?
  - An auxiliary circuit that degrades read/write-ability
  - SRAM bitcell + Reverse Assist =  SRAM bitcell

Example: SRAM write V_{MIN} Distribution with Reverse Assist Settings (RAS)



[Source: A. Banerjee. et al. ISQED 2014]

Input and Output Design Metrics

Input Metrics	
N	Number of SRAM bits on a chip
Y_{SRAM}	Core SRAM target yield
C	Number of canary SRAM bits
F_{th}	Canary failure threshold condition
V_{RA} (RAS[1])	Canary BL type reverse assist voltage
Output Metrics	
P_{fc}	Canary SRAM chip failure probability

[Source: A. Banerjee. et al. ISQED 2014]

[1]RAS=Reverse assist settings; F_{th}= Failure threshold condition

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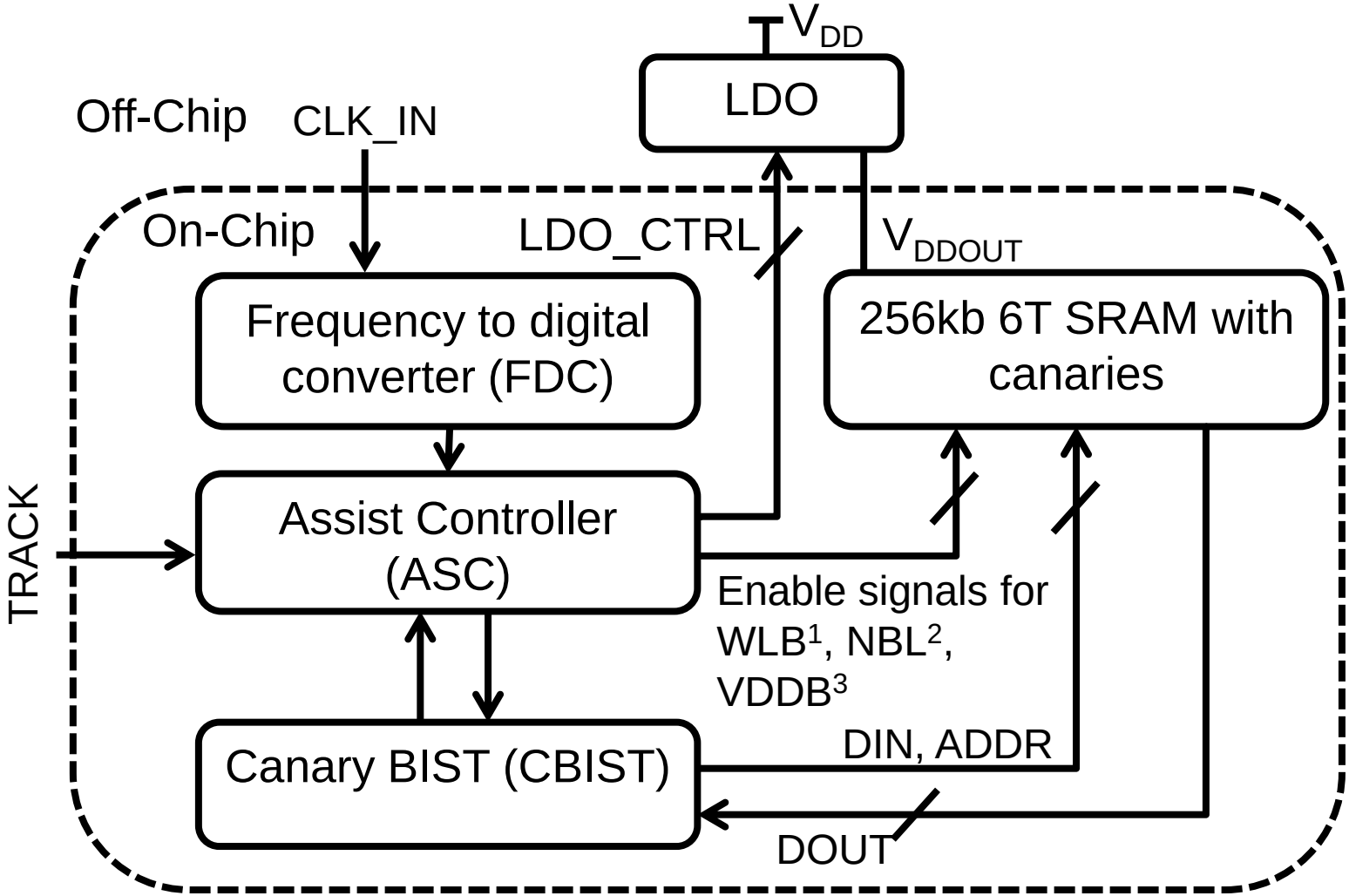
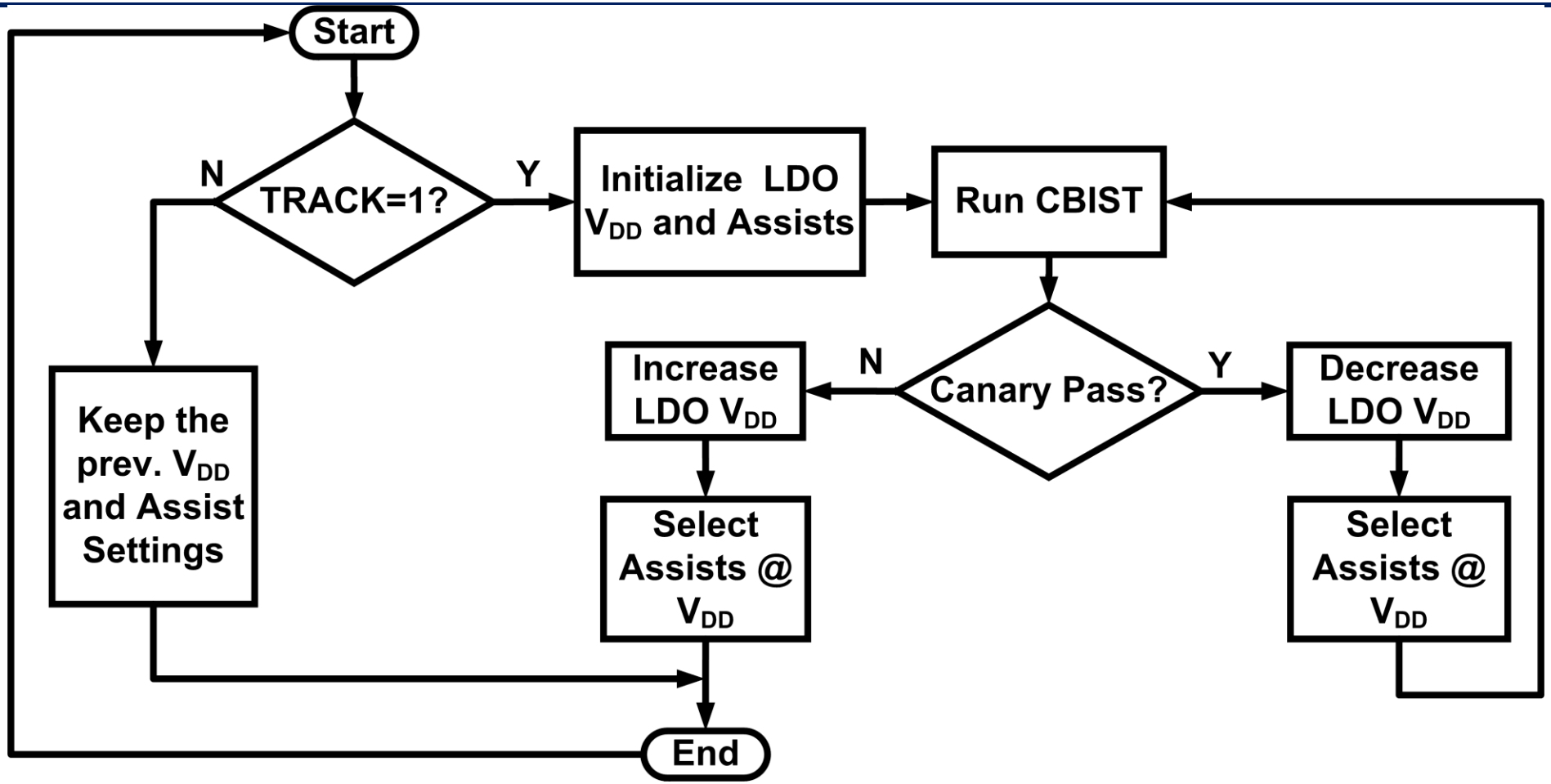
256kb Self-tuning SRAM Architecture



[1]*WLB=Wordline Boost,* [2]*NBL=Negative Bitline,* [3]*VDDB=Vdd Boost.*

V_{MIN} Self-tuning Operation



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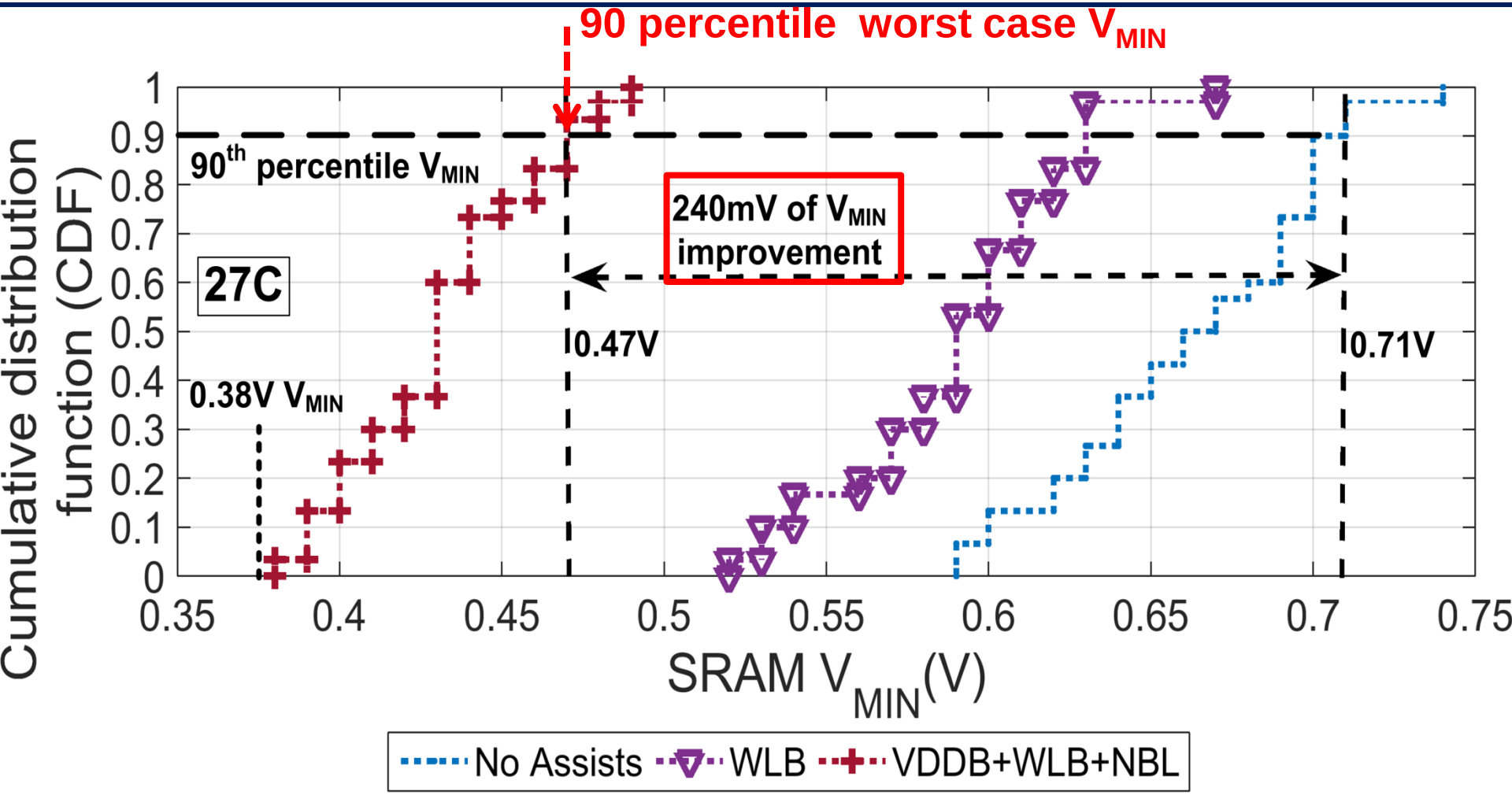
Experiments and Results

- SRAM + PAs = Max 240mV V_{MIN} improvements
- Does not eliminate V_{MIN} guard-bands

PA=Peripheral assists

V_{MIN} Lowering using Combined Read/Write Assists



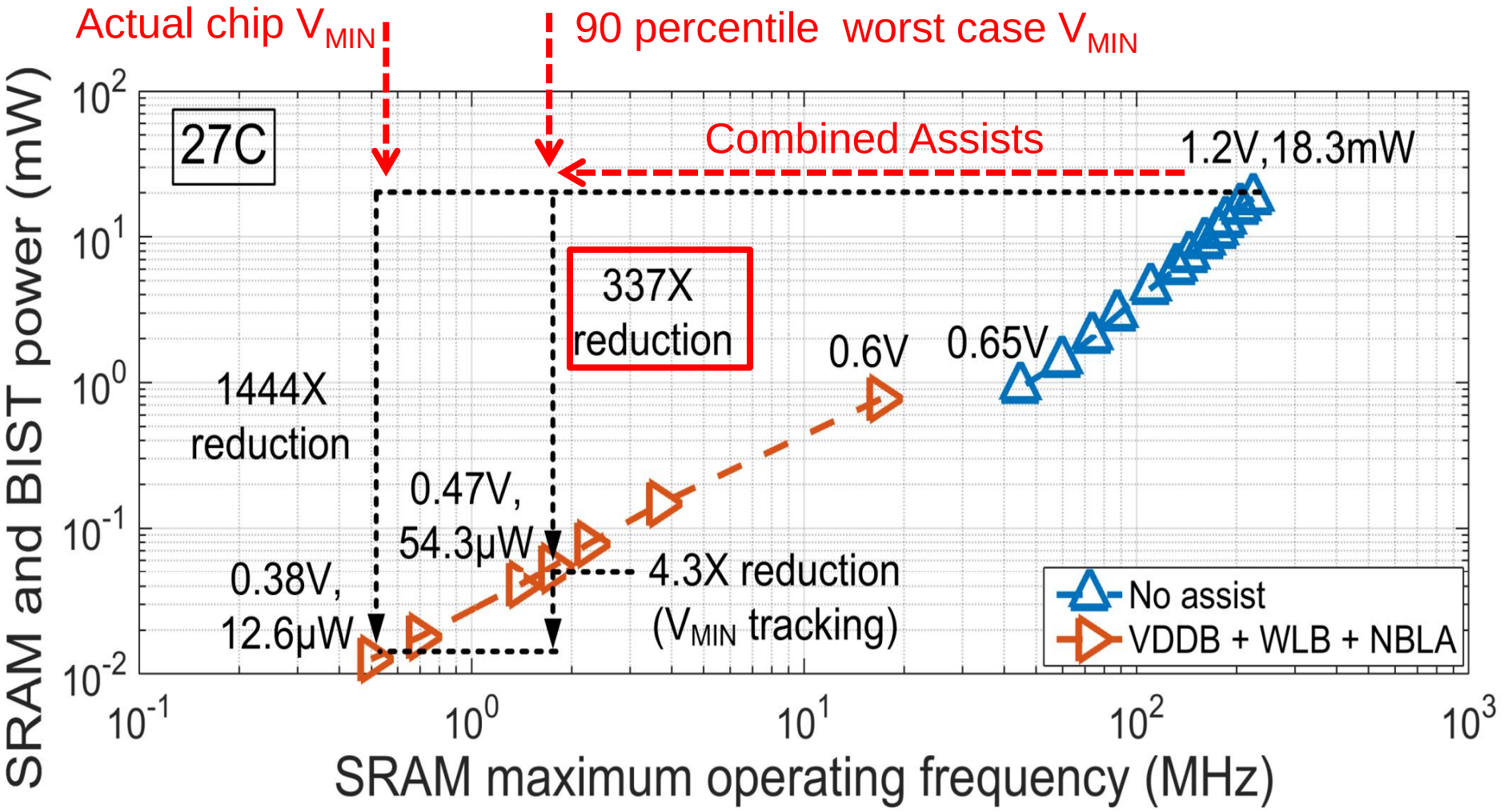
Measured CDF showing V_{MIN} improvement w/ combined assist

Experiments and Results

- SRAM + PAs + Canaries = Arbitrary guard-band lowering can save 1444X active power
- SRAM + PAs + Canaries = 12.4X leakage savings

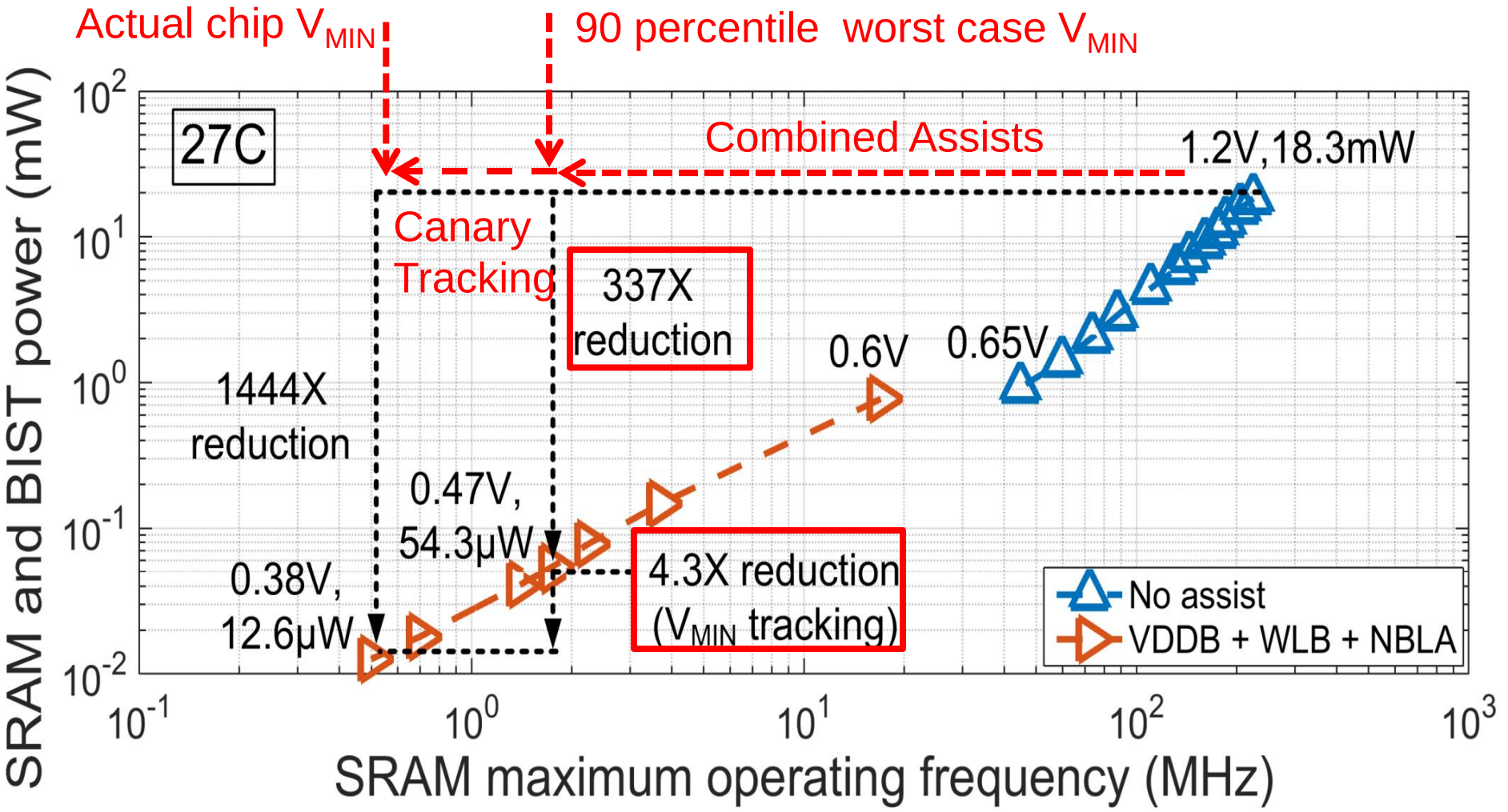
PA=Peripheral assists

Active Power Reduction using Combined Assist and Guard-band Lowering Canary Tracking



Measured active power improvements

Active Power Reduction using Combined Assist and Guard-band Lowering Canary Tracking



Measured active power improvements

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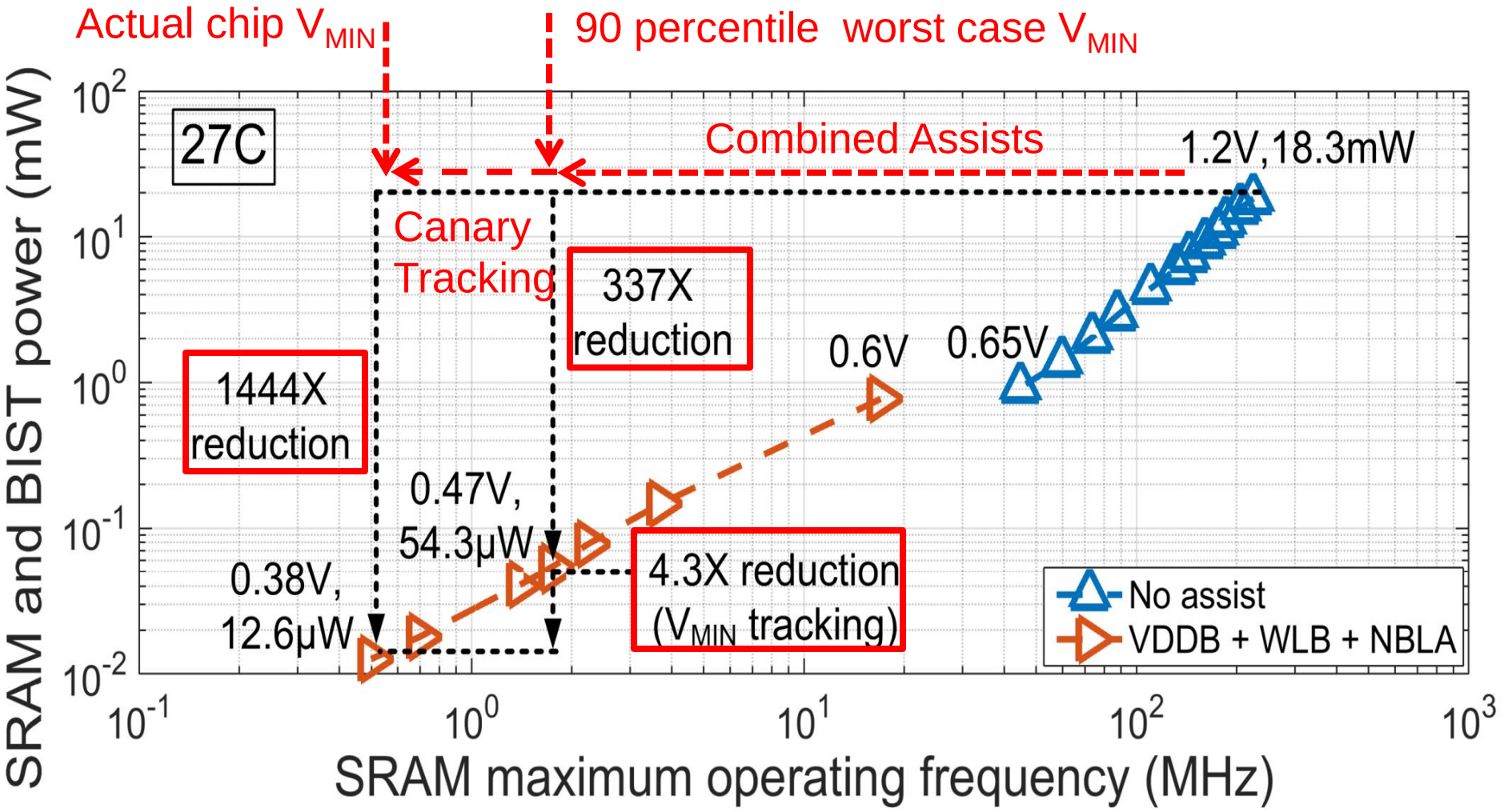
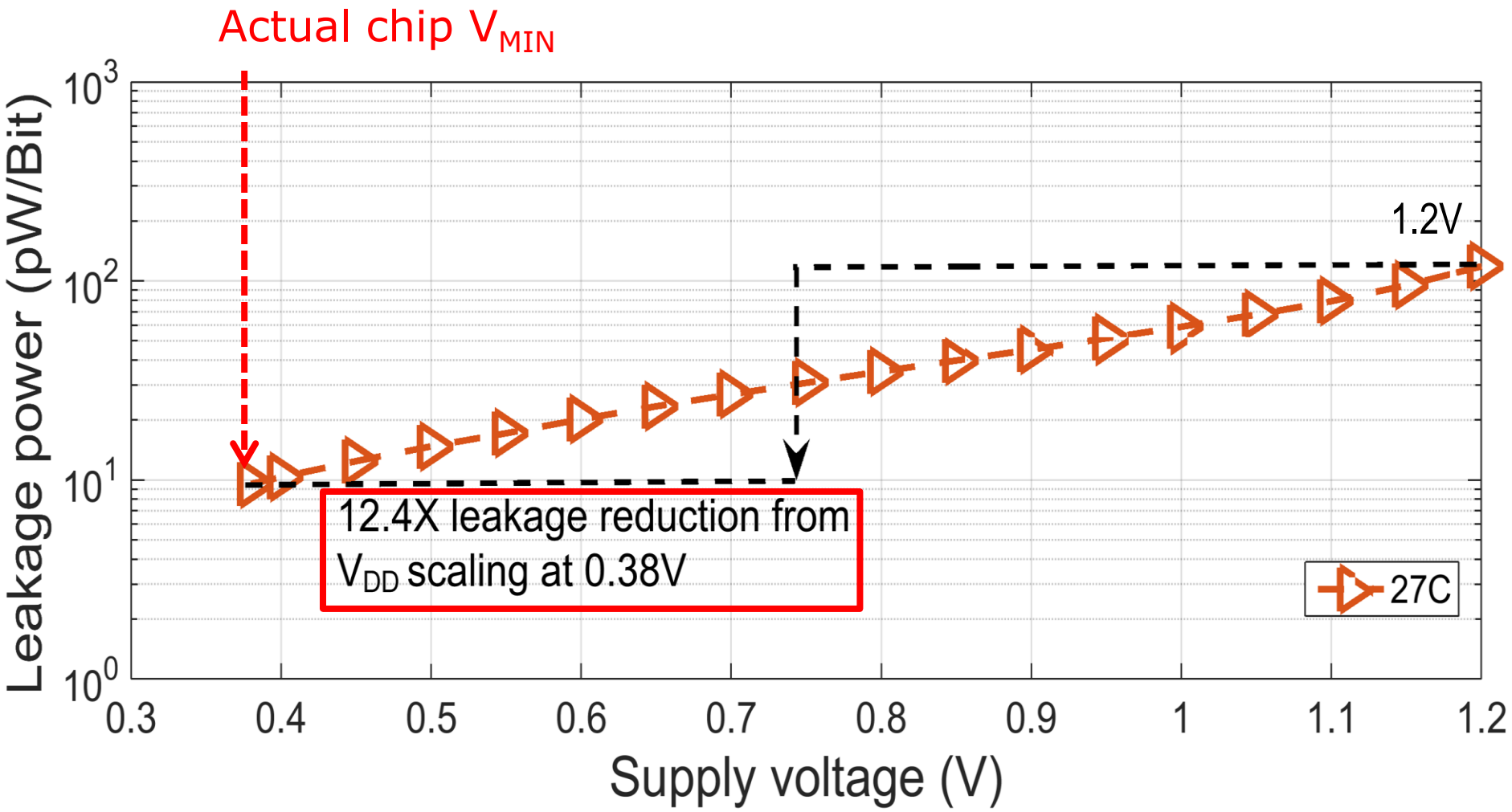


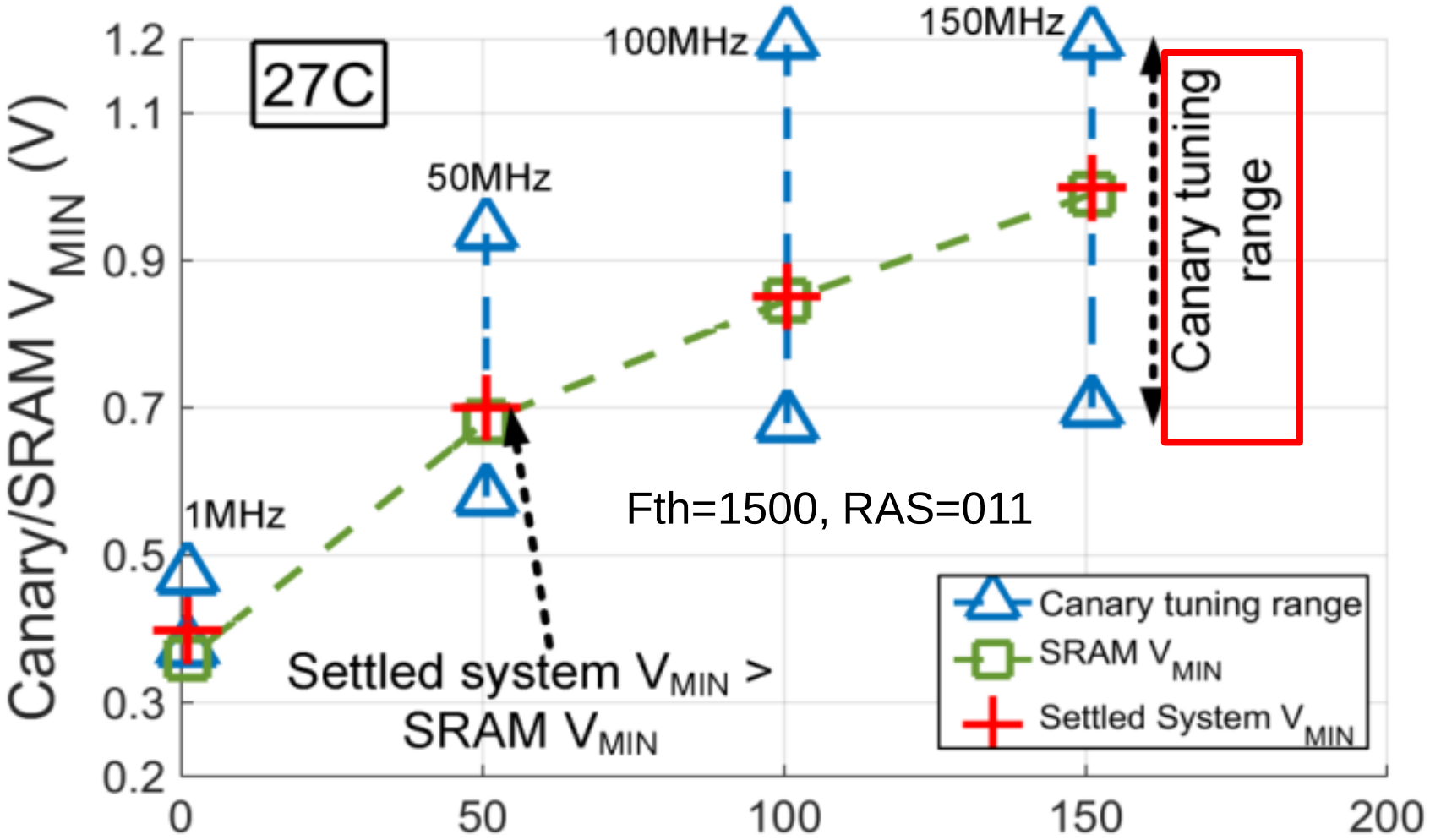
Measured active power improvements

Leakage Power Reduction using Combined Assist and Canary Tracking



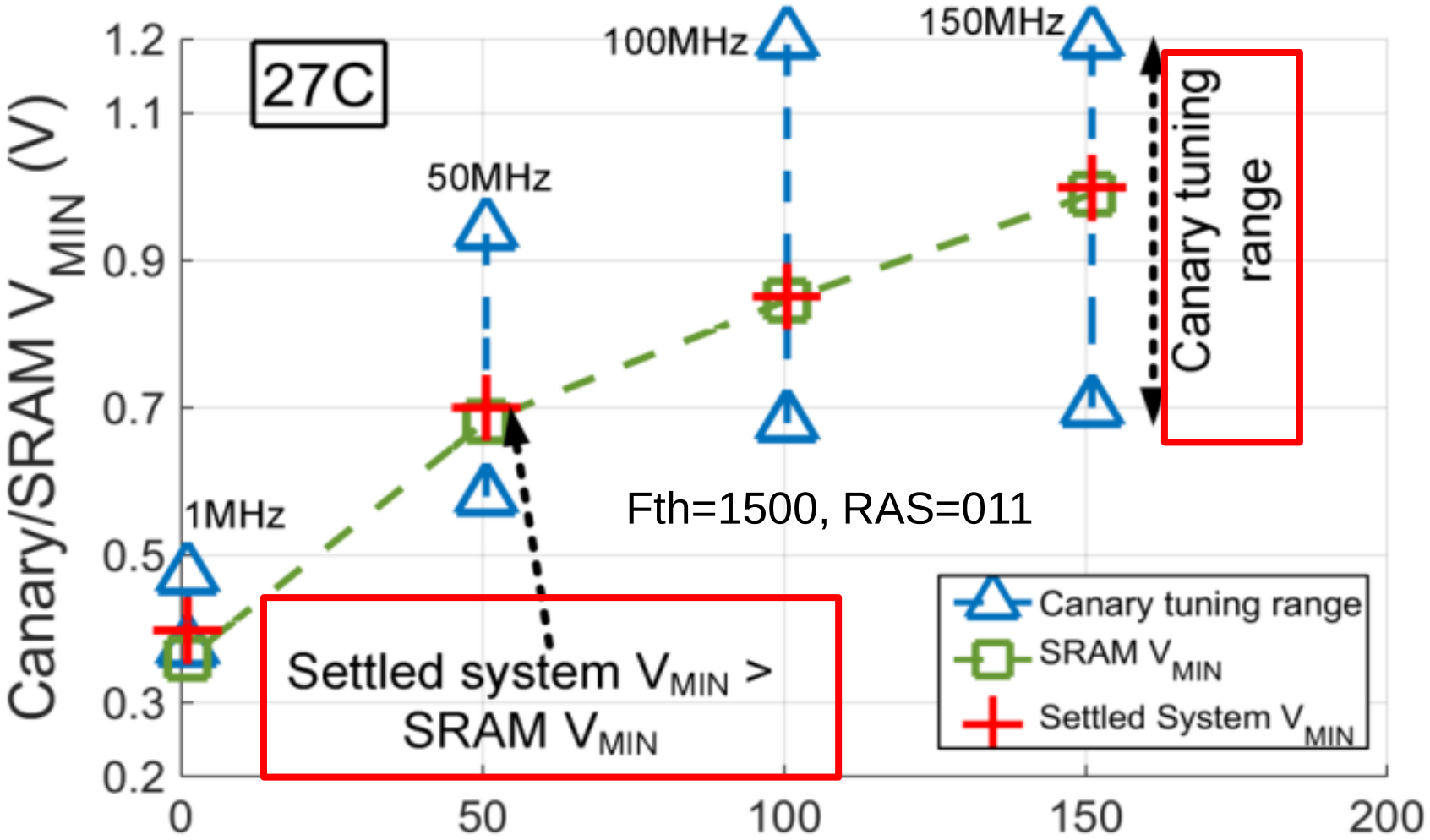
Measured leakage power improvements

Canary V_{MIN} Tracking @ 130nm Bulk



Measured canary V_{MIN} tracking across frequencies

Canary V_{MIN} Tracking @ 130nm Bulk



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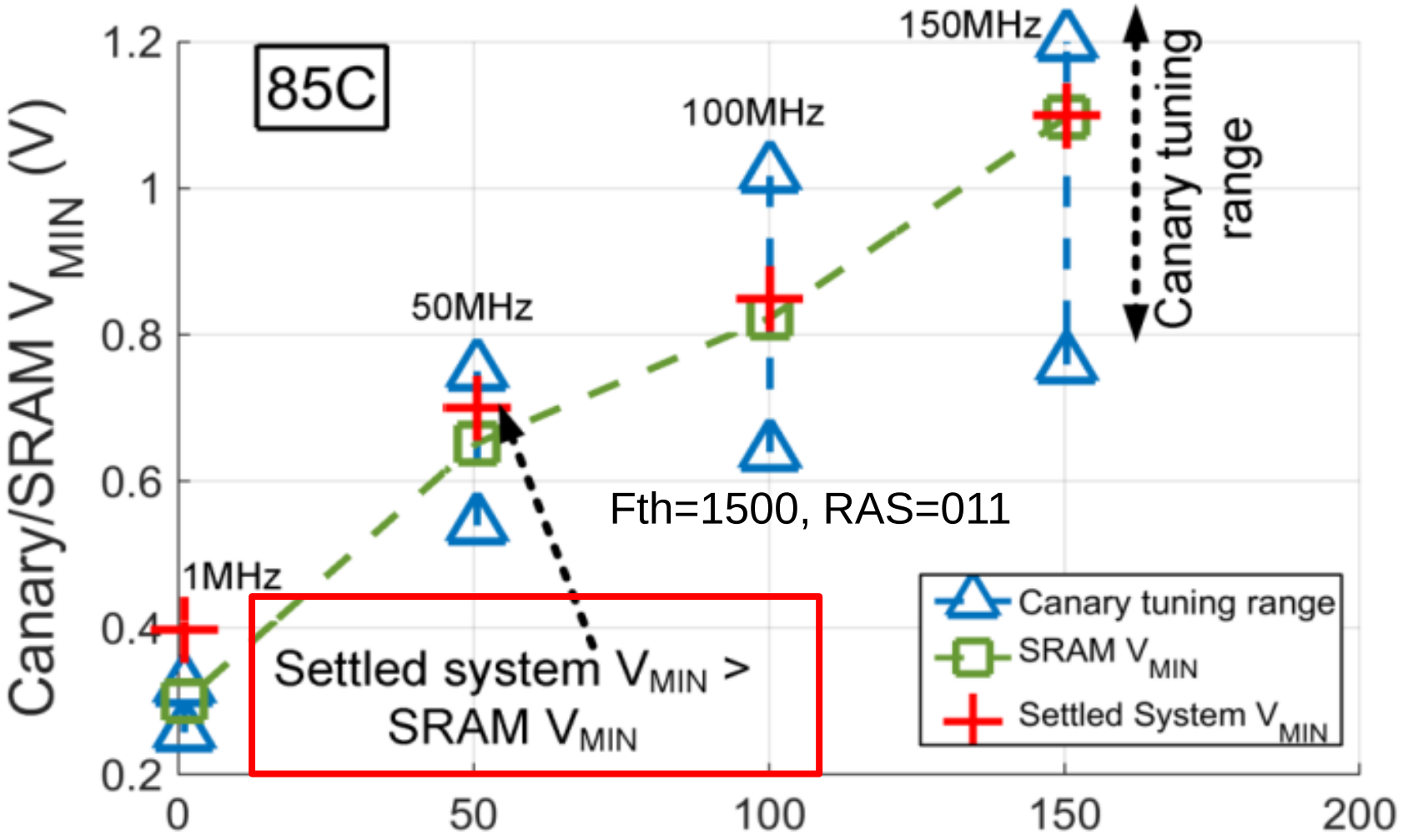
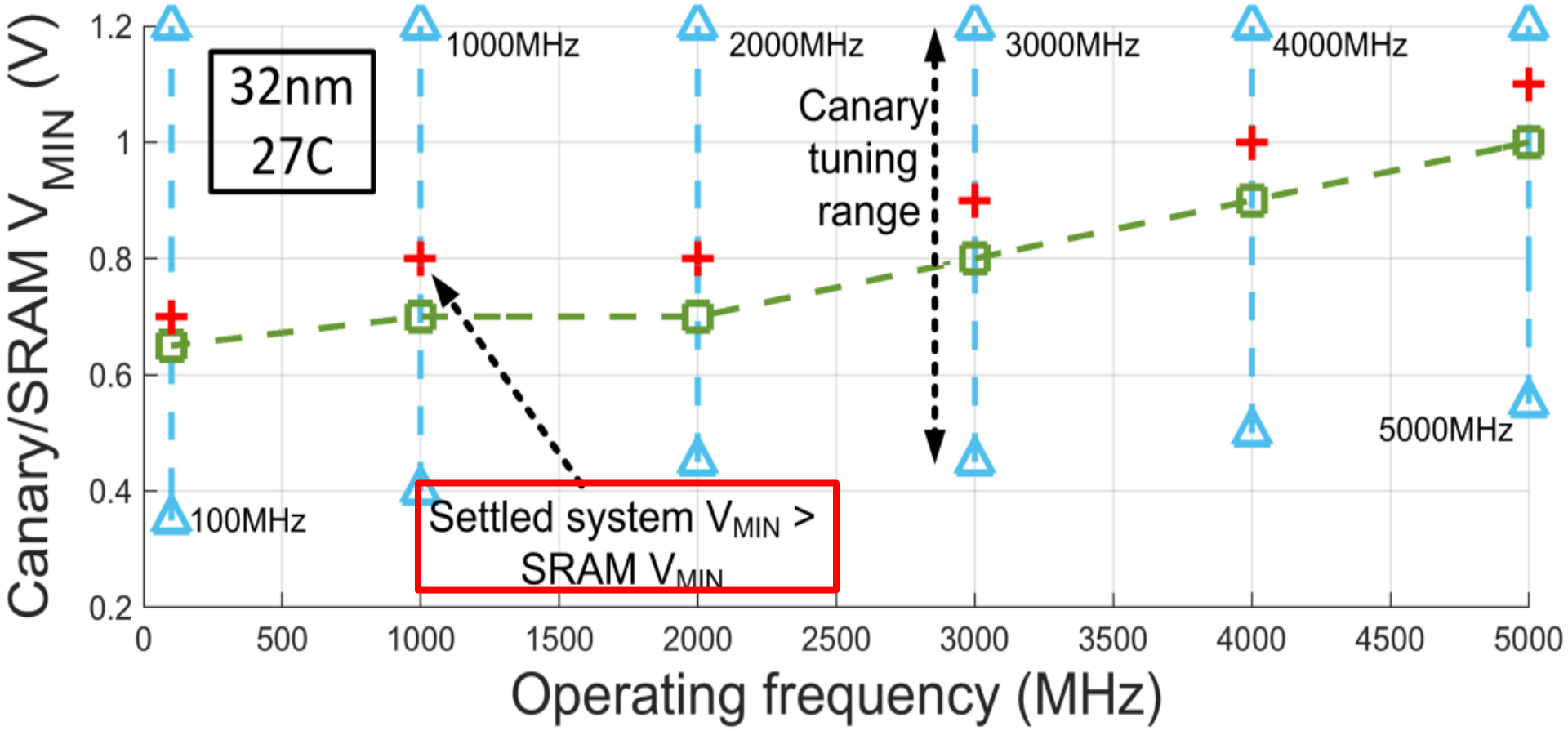


Measured canary V_{MIN} tracking across frequencies

Scalability of Canary Tracking @ 32nm FDSOI



Simulation results of canary based V_{MIN} Tracking at TT corner

Overhead

- Canary area overhead only 0.77% (array)
- Combined assist area overhead 2.8% in SRAM
- Total system components without BISTs 1.8%
- Onetime canary tuning (matching the worst case SRAM bitcell) overhead
- Running ~ 90/282 cycles/V_{DD} granularity per frequency/temp change for full 512b/2kb canaries

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Comparison

		VLSI' 15	This work	ISSCC'15	VLSI'14	ISSCC'12
Memory Features	Technology	14nm	130nm	28nm	180nm	22nm
	Cell type	8T	6T	6T	8T	6T
	Capacity	288kb	256kb	256kb	16KB	576KB
DVS/VMIN Features	DVS range	1-0.3V (700mV)	1.2-0.38V (850mV)	0.9-0.58V (320mV)	1.8-0.6V (1200mV)	1-0.625V (375mV)
	V_{MIN} Tracking	N	Y	N	N	N
	V_{MIN}	0.3V	0.38V	0.58V	0.6V	0.7V
Supply / Power	Sub-VT Operation	N	Y	N	N	N
	Max power Reduction	-	1444X	-	16.4X	-

Conclusion

- A wide DVS range (1.2V-0.38V) with lower SRAM V_{MIN} (0.38V) achieved using multiple assists (write/read) across supplies
- Canary sensors track SRAM V_{MIN} for margin guard-band minimization
- Demonstrated a reliable and an adaptive SRAM system selecting optimal V_{DD} and assist techniques for ULP IoE enablement

Acknowledgements

- Advisor: Professor Ben Calhoun
- UVa Colleagues: Harsh Patel , Ningxi Liu, Farah Yahya, Divya A. K., Kevin Leach, Dilip Vasudevan, Terry Tigner
- Nvidia Colleagues: Tom Gray and John Poulton
- These projects was supported in part by NVIDIA through the DARPA PERFECT program

Thank You