A Sub-nW 93% Peak Efficiency Buck Converter With Wide Dynamic Range, Fast DVFS, and Asynchronous Load-Transient Control

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Abstract—This article presents a highly efficient buck converter with sub-nW quiescent power and wide dynamic range for ultra-low-power (ULP) Internet-of-Things (IoT) systems-on-chip (SoCs). To optimize the SoC power consumption and performance, this buck converter supports fast dynamic voltage and frequency scaling (DVFS) and fast load-transient response (FLTR) using an asynchronous control scheme. To achieve robust and high-efficiency power delivery over process, voltage, and temperature variations, an adaptive deadtime controller (ADTC) is proposed with minimized area and power overhead. The power stage and gate drivers are optimized by a length split technique and a strong-up weak-down (SuWd) scheme to achieve low quiescent power. In addition, the buck converter is fully self-contained with a bias generator (BG), clock, and power-on-reset (PoR) integrated on-chip. Fabricated in 65-nm CMOS, measurement results show that the buck converter achieves 802-pW quiescent power and 93% peak efficiency at 1.5-V input voltage. The measured dynamic range is from 0.5 to 2.75 mW, which is over six orders of magnitude. The measured voltage droop is 56 mV for a 45-nA-to-1-mA load current step and DVFS up- and down-tracking takes 10.57 and 19.81 μs for an 88- and 92-mV reference step, respectively. This sub-nW buck converter integrates fast DVFS and FLTR features with a wide dynamic range making it suitable for ULP IoT applications.

Index Terms—Asynchronous control, buck converter, fast dynamic voltage and frequency scaling (DVFS), fast load-transient response (FLTR), high efficiency, sub-nW quiescent power, wide dynamic range.

I. INTRODUCTION

WITH growing research interests and rapid development in wireless sensor nodes, healthcare devices, green and efficient industry, smart home, and cities, systems-on-chip (SoCs) need to work autonomously with energy harvesters to use energy directly from environment or keep active by using batteries with minimized form factor and a lifetime of tens of years with minimum maintenance. Therefore, aggressive power scaling techniques for the Internet-of-Things (IoT) SoCs are needed and projected to continue for a longer system lifetime, especially when those devices are powered by a shrinking size of energy harvesters. A commercial CR1025 lithium coin battery [1] only provides a 30-mAh capacity, which provides <15 months lifetime at 3-μA load power. An on-chip photovoltaic (PV) cell can only provide 10 nW–1 μW under 10–1000 lx for indoor applications [2]. With the limited form factor and diverse environmental conditions, the power dissipation of the SoCs needs to decrease down to a few nanowatts or even picowatt level [3], [4] to meet the ultra-low-power (ULP) budget for next-generation IoT devices. To optimize the SoC power and performance, several power management techniques have been used, including dynamic voltage and frequency scaling (DVFS) [3]–[5] and multimodal control [4], [6]–[8]. However, these trends and new techniques bring tremendous challenges to the dc–dc converter design. For DVFS technique, the supply voltage and clock frequency of the SoC adaptively scale according to the workloads and energy conditions to achieve energy saving while maintaining the performance requirements. Therefore, the dc–dc converter should support fast reference tracking to enable DVFS and adapt to the load current change with fast response. Furthermore, to optimize system energy and performance, components usually operate at different modes, with a wide range of dynamic power consumption. For example, the SoC in [4] covers a power range from 10 nW to 4 mW (4×10^5) with three operation modes and Lin *et al.* [6] reported an SoC that has a power range from 1.85 nW to 343 μW (1.8×10^5) with six different operation modes. Besides, the dc–dc converter potentially also powers different types of components, such as power scalable ADC [9] and clock [10]. All those applications motivate the necessity of designing a ULP, high efficiency, and wide dynamic range dc–dc converter with fast DVFS tracking and fast load-transient response (FLTR) to avoid large voltage droop and long settling time during load operation mode switching.

Thus far, a wide variety of ULP voltage regulators have been reported to achieve those goals [11]–[19]. The sub-nA digital low dropout (DLDO) regulator in [11] utilizes a hybrid synchronous binary-searching and asynchronous linear-searching

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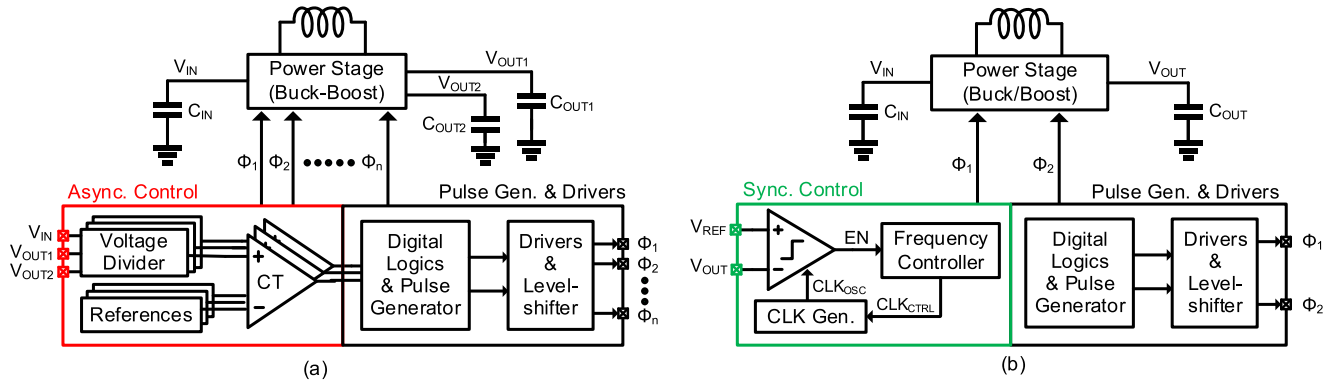
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Fig. 1.   Conventional architectures of ULP dc–dc converters. (a) Using an event-driven asynchronous control loop [16]. (b) Using a PFM-based synchronous control loop [15], [17], [23].

control to achieve a wide dynamic range and FLTR. However, the power efficiency degrades for a large input and output voltage ratio intrinsically. A switched-capacitor (SC) voltage regulator [12] utilizes power-gating and event-driven asynchronous control to achieve picowatt leakage power with limitations of 50% peak efficiency and a 1.3×10^4 dynamic range. Another sub-nW SC regulator [13] proposes a recursive current injection scheme where the input current is injected to each stage of the voltage booster but only achieving 58% peak efficiency and a 10^2 dynamic range. The inductor-based switching voltage regulator (SVR) has the advantages of high conversion efficiency, which is suitable for energy-efficient systems. Bandyopadhyay *et al.* [14] proposed a 1.1-nW boost converter with 544-pW quiescent power and 4-nW maximum output power. Paidimarri and Chandrakasan [15] proposed a 92% peak efficiency and wide dynamic range buck converter with 240-pW quiescent power. The optimization of power FET length and pulsewidth is explored to achieve low quiescent current and minimized energy loss. In [16], a 3.2-nW buck–boost converter is presented for solar energy harvesting and battery power management. To achieve low switching loss, the system operates in an asynchronous fashion with a continuous-time (CT) comparator. Sadagopan *et al.* [17] presented a Wi-Fi energy harvesting boost converter with ~1-nW quiescent power. Although the prior inductor-based SVR has achieved sub-nW or near sub-nW quiescent power, they either suffer from small output power range [14], [16], [17] due to the limited clock frequency range and slow speed or require manual control for clock and deadtime [15]. Furthermore, none of the prior arts support both fast DVFS and FLTR. Conventional work [18]–[21] utilizes a multilevel structure or current-mode scheme to achieve FLTR and DVFS with a small value of inductor and capacitor. However, those techniques usually require a high-frequency clock (~MHz) and target on milliwatt power range, which are not suitable for ULP applications.

To address the existing challenges, we presented a sub-nW buck converter with high peak efficiency, wide dynamic range, fast DVFS, and FLTR [22]. By using a hybrid synchronous and asynchronous feedback control loop, reusing existing signals and circuits, and multiplexing the control paths, the buck converter achieves those features with minimum power and area

overhead. The synchronous loop is able to achieve frequency modulation and output regulation with high efficiency and the asynchronous loop automatically tracks the maximal frequency the circuit can operate at to achieve fast reference tracking. The control paths of the DVFS up-tracking and FLTR are multiplexed to achieve low area and power cost. Using thick oxide devices, a wide frequency range clock, and leakage-optimized power stage and drivers, this buck converter achieves sub-nW quiescent power and 93% peak efficiency with wide dynamic power range (5.5×10^6). In this article, we expand the work [22] to further illustrate the design details, tradeoffs, and circuit implementations in the context of energy-constrained ULP IoT SoC applications. The rest of this article is organized as follows. Section II describes the system architecture, design considerations, and control loops. Section III explains the circuit implementations followed by the measurement results and comparison with the state-of-the-art buck converters in Section IV. Finally, Section V concludes this article.

II. SYSTEM ARCHITECTURE AND CONTROL LOOPS

A. Conventional Versus Proposed Architectures

The conventional dc–dc converters [15]–[17], [23] achieve low quiescent and high conversion efficiency by using two types of architectures shown in Fig. 1. Fig. 1(a) shows the event-driven asynchronous control scheme [16]. The input/output voltages are regulated by the amplifier-based CT comparators. Based on the voltage value, the comparator generates the enable signal and the pulse control block triggers the power delivery operation where the inductor gets charged and then discharged to deliver power to the load side. The second architecture uses a synchronous pulse frequency modulation (PFM)-based buck/boost scheme, as shown in Fig. 1(b), where the clock frequency is adjusted based on the input/output power. When the output power is high, the clock frequency increases to allow more frequent comparisons between V_{REF} and V_{OUT} and power delivery operations for output regulation. When the output power is low, the clock frequency decreases to save dynamic power loss. Therefore, the PFM can scale the frequency to balance between power loss and speed. To achieve FLTR and fast DVFS for the two prior architectures, the asynchronous control scheme needs to
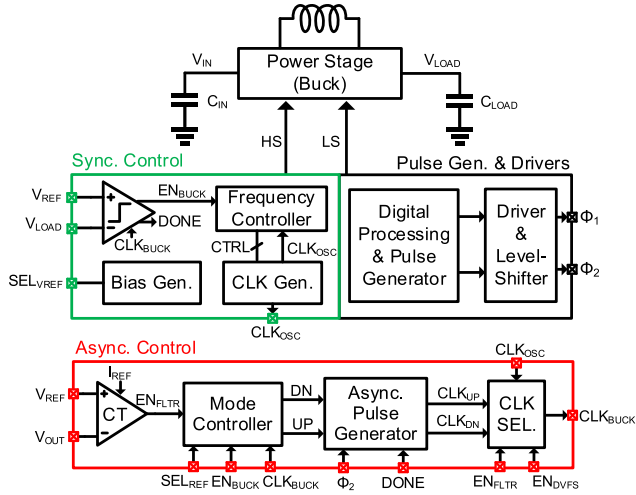
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Fig. 2. Proposed buck converter with hybrid synchronous/asynchronous control loops.

Fig. 3. Flowchart for mode control algorithm.

increase the bias current of the comparators to achieve higher speed, and the synchronous scheme must always run at a high frequency to improve the bandwidth and response speed. Due to those intrinsic drawbacks, conventional scenarios are not suitable for ULP DVFS applications.

The proposed architecture utilized a hybrid synchronous and asynchronous control loops to achieve fast DVFS and FLTR, as shown in Fig. 2. The system consists of four parts: a power stage with off-chip inductors and capacitors, a synchronous PFM-based loop, an asynchronous control loop, and a pulse generator with drivers that controls the power stage to deliver power from V_{IN} to V_{OUT}. The synchronous PFM loop is implemented to regulate the output of the buck converter. At the rising edge of the CLK_{BUCK}, the strong-arm-based comparator compares V_{REF} and V_{OUT}. When V_{OUT} is smaller than V_{REF}, the output of the comparator, EN_{BUCK}, goes up to 1 and enables power delivery for only once. Otherwise, EN_{BUCK} stays at 0 and no power delivery operation is executed. When CLK_{BUCK} is zero, EN_{BUCK} gets reset to 0, ready for next comparison. The frequency controller with PFM control algorithm adaptively tunes the frequency of CLK_{OSC} by maintaining the frequency ratio of CLK_{BUCK}/EN_{BUCK} to be 3–4 times. The mode controller (MC) controls the circuit to operate among three modes: synchronous mode, DVFS mode, and FLTR mode. In default, the MC disables the asynchronous loop and the system clock is controlled by the PFM and equal to CLK_{OSC}. When SEL_{VREF}, which controls the voltage references, has changed or EN_{FLTR} is high, the MC enables asynchronous loop to achieve fast DVFS and FLTR, as shown in Fig. 3.

When the asynchronous loop is enabled, unlike the traditional way where the CT comparator in the asynchronous loop regulates the output [16], the proposed asynchronous loop generates a fast asynchronous pulse frequency to clock the strong-arm comparator in the synchronous loop to regulate the output. The asynchronous loop has four functions: 1) the CT comparator detects the voltage drop at the output; 2) the asynchronous pulse generator (APG) reuses the existing
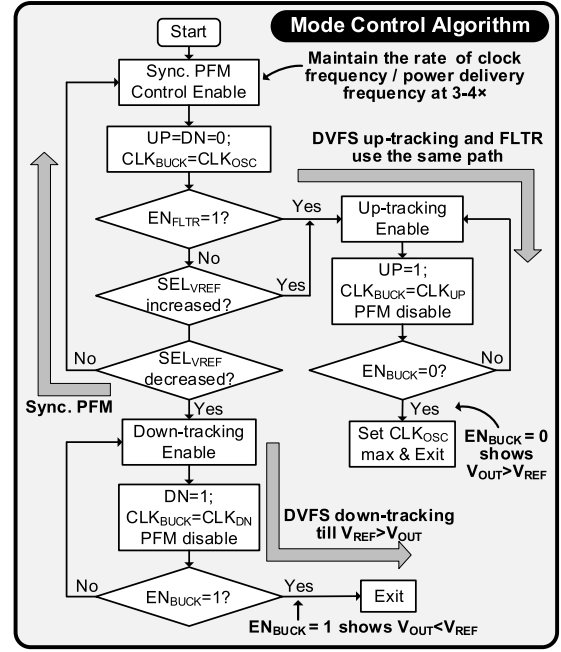
DONE and low side (LS) signals to generate the maximal frequency that the circuit can operate at for fast DVFS and FLTR; 3) based on the circuit mode, the clock selector chooses asynchronous pulse, CLK_{UP} or CLK_{DN}, as the system clock, CLK_{BUCK}, which is used by the strong-arm comparator and MC; and 4) the feedforward signal, EN_{DVFS}, generates a pulse at CLK_{BUCK}, to quickly let the MC response. Therefore, the FLTR and DVFS tracking speed is no longer dependent on the bias current of the CT comparator and is maximized by the APG. In this design, a 50-pA bias current is used for the CT comparator to achieve low static power. The APG is digitally implemented and is only enabled when DVFS and FLTR are detected.

Furthermore, since the FLTR and DVFS up-tracking both track a higher voltage reference, their control paths can be merged to achieve lower area and power cost, as shown in Fig. 3. The DVFS is enabled when SEL_{VREF} changes, which is controlled externally by the processor or users based on performance requirements and power-saving demand, while the FLTR is enabled internally by the CT comparator based on the voltage difference between V_{REF} and V_{OUT}. With all those features, the asynchronous loop adds negligible power and area overhead to the whole system while enabling fast reference tracking.

B. Power Loss Analysis and Component Parameter Selection

Adding an extra control loop inevitably increases area and power, to achieve high efficiency at near nanowatt range, the power loss of the circuits should be carefully considered and optimized especially at light load. For discontinuous conduction mode (DCM) operation, as shown in Fig. 4, where the inductor current keeps at zero during the OFF state (T_{OFF}), the efficiency of the dc–dc converter can be calculated by the

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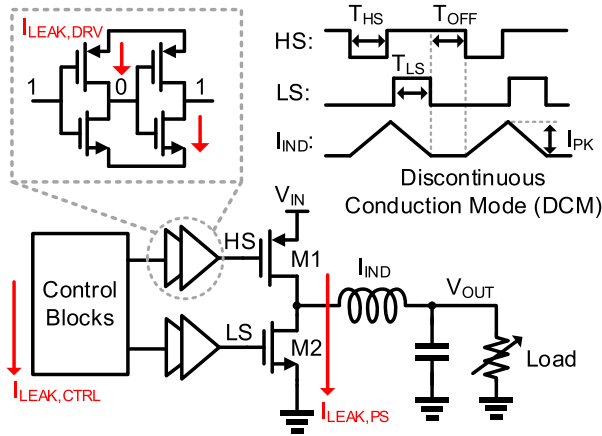

Fig. 4.   Leakage loss paths and key waveforms for DCM operation.

following equation:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_{OUT} + P_{DYN} + P_Q + P_{SW} + P_{COND}} \quad (1)$$

where P_{IN} and P_{OUT} stand for input and output power, respectively, and P_Q, P_{DYN}, P_{SW}, and P_{COND} stand for quiescent power, dynamic power, switching loss, and conduction loss, respectively. Notably, P_{DYN} is proportional to the output current and P_Q is the power consumption when the output current is zero. It consists of the dynamic loss of control logics, leakage power, and bias current. As load power keeps shrinking down to nanowatt–picowatt, P_{SW}, P_{COND}, and P_{DYN} are negligible, while P_Q dominants. Therefore, to improve the efficiency, the dynamic loss, leakage, and bias current should be minimized.

In terms of the leakage power and bias current, or called static power, as shown in Fig. 4, it mainly comes from three parts, which are buffer stage leakage, power stage leakage, and static power from control circuits. Several techniques are proposed to suppress the static power including transistor length modulation [15] and power stage over-driving [14], [17]–[23]. In this work, the three parts are effectively optimized by utilizing a strong-up weak-down (SuWd) driver, length split technique, digital implementation, signal reuse, and path multiplexing, which will be discussed in detail in Section III.

In terms of the dynamic loss minimization, a clock source with a wide frequency range and PFM control scheme is desired to be able to scale the clock frequency down to a few hertz. To allow low-frequency operation, an inductor with large inductance value ($>\mu$H) is needed since a large inductor can deliver more power per operation, which allows the circuit to operate at a lower frequency at light load. The following equations show the methods to calculate the desired components parameters for the purpose of decreasing power delivery frequency and dynamic power loss. The inductor peak current can be calculated by the following equation:

$$I_{PEAK} = \frac{V_{IN} - V_{OUT}}{L} T_{HS} \quad (2)$$

where L represents the inductance of the off-chip inductor and T_{HS} represents the width of the high side (HS) signal.

The energy delivered to the load per power delivery operation, E_{PULSE}, can be calculated by (3), if the inductor peak current is given

$$E_{PULSE} = \frac{V_{IN} L I_{PEAK}^2}{2(V_{IN} - V_{OUT})}. \quad (3)$$

The energy delivered per pulse increases with the inductance. Therefore, with a larger inductance, the power delivery frequency can be decreased according to the following equation:

$$P_{LOAD} = P_{PULSE} = FREQ_{PULSE} \times E_{PULSE}. \quad (4)$$

However, the ripple voltage V_{RIPPLE} increases with E_{PULSE} according to the following equation:

$$C_{LOAD}((V_{OUT} + V_{RIPPLE})^2 - V_{OUT}^2) = 2E_{PULSE}. \quad (5)$$

For example, assume that $V_{IN} = 2$ V, $V_{OUT} = 0.5$ V, and $I_{PEAK} = 20$ mA, if we want the frequency of the power delivery operation to be 10 Hz for a 100-nW output power, according to (4) and (5), we can resolve L, which needs to be 37.5 μH. If a $<$10-mV ripple voltage is required, by utilizing (5), C_{LOAD} requires to be 1.98 μF.

C. Fast Reference Tracking for DVFS

Fast DVFS up-tracking allows the circuit to quickly switch to a high-power and high-performance mode, which is critical for performance regulation. For DVFS down-tracking, although the slow free-discharging method [24] can fully utilize the energy stored on the cap, yet slowly moving into low power mode could lead to more power consumption for the components that are communicating with the free-discharged blocks. Because the frequent communications are likely to generate more power at interfaces and other components, especially in SoCs applications. Therefore, fast DVFS down-tracking is desired as well. However, the constrained current budget significantly limits the bandwidth and frequency of the circuits, which leads to slow reference tracking and large settling time. When reference tracking is demanded, the dc–dc converter should maximize the power delivery to the load or the discharging current at the load. When T_{OFF} is negligibly small, the buck converter can continuously delivery energy to the load, and the energy delivery speed can be calculated by being divided by the period. Therefore, when the load current is much smaller than the up-tracking current, the up-tracking speed, S_{PULSE}, can be expressed as follows:

$$S_{PULSE} = \frac{E_{PULSE}}{T_{PULSE}} = \frac{V_{OUT} I_{PEAK}}{2} \quad (6)$$

where T_{PULSE} represents the time period of one power delivery, which equals $T_{HS} + T_{LS}$ when T_{OFF} is zero.

According to (6), faster energy delivery can be achieved with a larger peak inductor current. However, it causes a larger conduction loss and degrades efficiency [15]. Therefore, with the analysis in Section II-B, the choice of the off-chip component parameters is a tradeoff between speed, efficiency, and ripple voltage. For a given peak inductor current which is decided by the efficiency requirements, larger inductance and
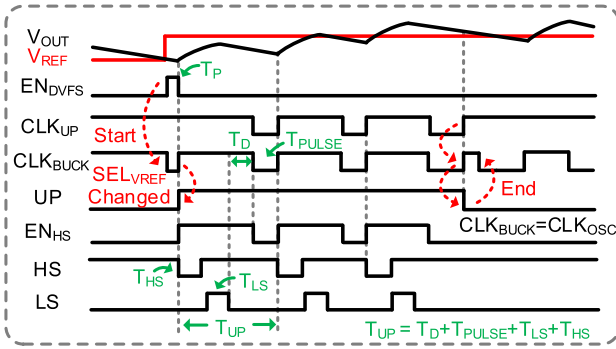
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Fig. 5.   Operation timing diagram of the reference up-tracking.

Fig. 6.   Operation timing diagram of the reference down-tracking.

Fig. 7.   Operation timing diagram of the FLTR.

capacitance decrease the quiescent power and ripple voltage yet at a cost of slower DVFS tracking speed.

Fig. 5 shows the waveform of the DVFS reference up-tracking. To achieve fast up-tracking, the asynchronous loop generates the maximal clock frequency the circuit can run to deliver energy quickly. As analyzed above, T_{OFF} needs to be near zero to enable continuous power delivery. Therefore, the LS falling edge, which represents the completion of one power delivery, is used to generate the asynchronous pulse, $\mathrm{CLK_{UP}}$. The signal $\mathrm{EN_{DVFS}}$ is used to generate a pulse, T_P, at $\mathrm{CLK_{BUCK}}$ to let the circuit quickly move into the DVFS mode since the MC makes decision at the rising edge of $\mathrm{CLK_{BUCK}}$. When $\mathrm{SEL_{VREF}}$ changes, the MC enables the DVFS mode. Then, the UP signal equals 1 and $\mathrm{CLK_{UP}}$ is selected as the system clock. At the end of each power delivery operation, the LS falling edge triggers a pulse, T_{PULSE}, after a time delay, T_D, to generate $\mathrm{CLK_{UP}}$. Then, the asynchronous pulse enables power delivery to the output to increase the voltage value until the comparator output, $\mathrm{EN_{BUCK}}$, is 0 at the rising edge of the $\mathrm{CLK_{BUCK}}$, indicating that $V_{\mathrm{OUT}} > V_{\mathrm{REF}}$. Then, the MC stops the up-tracking, and $\mathrm{CLK_{BUCK}}$ switches from $\mathrm{CLK_{UP}}$ back to $\mathrm{CLK_{OSC}}$. To regulate the output at higher V_{REF}, the $\mathrm{CLK_{OSC}}$ frequency is set to be maximum initially after the up-tracking completes. Then, the frequency is controlled by the PFM. The period generated by the APG is decided by the HS pulsewidth (T_{HS}), LS pulsewidth (T_{LS}), T_D, and T_{PULSE}. Notably, in the real design, T_D and T_{PULSE} could be negligible compared with T_{HS} and T_{LS}.

Fig. 6 shows the waveform of the DVFS down-tracking. Once triggered by the pulse created by $\mathrm{EN_{DVFS}}$, the MC detects the decrease of $\mathrm{SEL_{VREF}}$, and then, the DN goes to 1 and turns on a switch between V_{OUT} and GND, to generate a large current sink at output to quickly decrease the output voltage. Therefore, the comparator is required to work at the fastest speed to avoid potential undershoot. When the clock of the comparator is zero, the DONE signal gets reset. When the comparator finishes one comparison, the DONE signal goes up to 1, indicating the completion of comparison. The DONE signal is used to create the asynchronous pulse, $\mathrm{CLK_{DN}}$. The rising edge of the DONE signal followed by a short delay (T_D) enables the next comparison until $\mathrm{EN_{BUCK}} = 1$, representing $V_{\mathrm{OUT}} < V_{\mathrm{REF}}$. Then, the down-tracking stops, and the buck clock switches to the $\mathrm{CLK_{OSC}}$ again. During down-tracking, the clock period in DVFS down-tracking is equal to $2 \times T_D$.
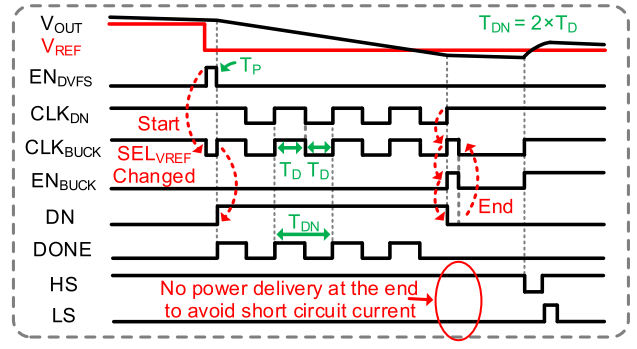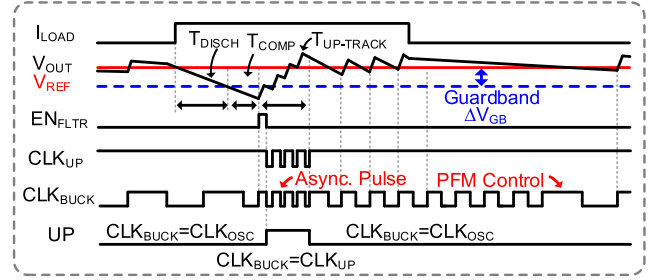
D. Fast Load-Transient Response

Fig. 7 shows the waveform of the asynchronous FLTR, which reuses the DVFS up-tracking path to achieve low power and area cost. When the output current changes with a step up, the voltage drops below the guard band, and $\mathrm{EN_{FLTR}}$ goes up to 1 to generate a pulse, T_P on $\mathrm{CLK_{BUCK}}$ to push the circuit into the FLTR mode. Once $\mathrm{EN_{FLTR}}$ is equal to 1, the MC enables FLTR and the circuits start to track the reference. The total settling time $T_{\mathrm{SETTLE}} = T_{\mathrm{DISCH}} + T_{\mathrm{COMP}} + T_{\mathrm{UP-TRACK}}$. The first parameter is the discharging time of the guard band voltage, ΔV_{GB}, which is dependent on the output capacitance, load current, and ΔV_{GB}. T_{COMP} is the delay mostly from the CT comparator. $T_{\mathrm{UP-TRACK}}$ is the time needed for charging the output to the voltage reference and is decided by the tracking speed, load current, and output capacitance. In this design, due to the low bias current and large ($\sim \mu \mathrm{F}$) off-chip decoupling capacitor, the discharging time of the guard band voltage and the delay of the CT comparator dominate the total settling time. Also, the voltage droop at the output is decided by the guard band and T_{COMP} since the FLTR is enabled after the CT comparator output changes to 1. Thus, as shown in Fig. 7, the voltage keeps dropping after it reaches the guard band due to T_{COMP}. After the FLTR is enabled, similarly, once the output voltage reaches the reference voltage, $\mathrm{EN_{BUCK}}$ stays at 0 after comparison, the circuits exit FLTR mode, and the system clock, $\mathrm{CLK_{BUCK}}$, switches back to equal to $\mathrm{CLK_{OSC}}$. When there is a current step down, the FLTR is not enabled and there is no overshoot theoretically even if the clock frequency is high since the power delivery operation is enabled only once if the comparator output is 1. After the load current steps down, there is no power delivery operation if $V_{\mathrm{OUT}} > V_{\mathrm{REF}}$.
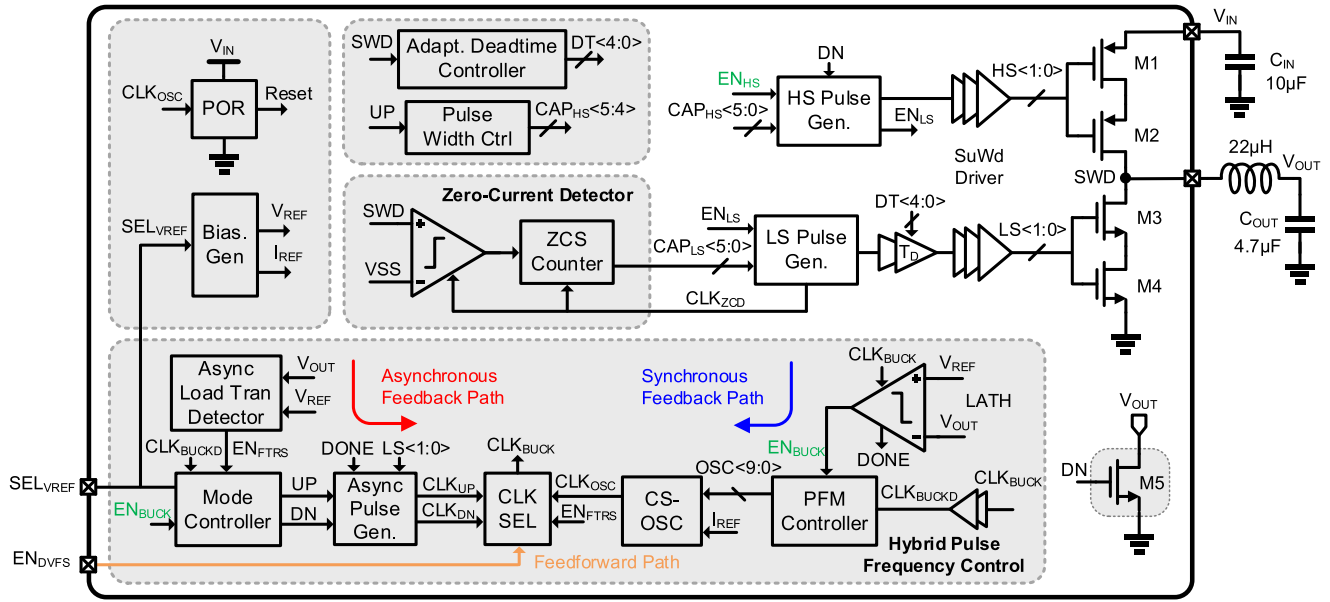
Fig. 8. System block diagram of the proposed buck converter [22].

Also, the PFM is enabled to decrease the clock frequency for power saving.

III. CIRCUIT IMPLEMENTATION

A. System Implementation

The detailed block diagram of the proposed buck converter is shown in Fig. 8. During general operation, the strong-arm latch, LATH, compares V_{OUT} with V_{REF} to generate the control signal, EN_{BUCK}, and enable power delivery under DCM. Triggered by the rising edge of EN_{BUCK}, the pulse generator generates the HS and LS pulses to enable power delivery. At the end of each power delivery operation, the ZCD comparator compares the switching node, SWD, with VSS and adjusts the LS pulsewidth through a counter to achieve zero-current switching (ZCS). The hybrid pulse-frequency control block switches the circuit between synchronous and asynchronous loops to achieve output regulation, clock frequency modulation, and fast DVFS and FLTR. For the PoR, once V_{IN} is powered up, a voltage detector block generates an enable signal to turn on a 7-bit counter and the current-starving oscillator (CS-OSC). After counting for a certain number of clock cycles, an output pulse is generated to reset the buck converter. To minimize the quiescent power, all the digital blocks are implemented with 500-nm length 2.5-V-thick oxide devices at the cost of a larger area.

B. Driver and Power Stage Optimization

The power stage design is critical to achieve low power and high efficiency for buck converter. To optimize the tradeoffs among conduction loss, switching loss, and quiescent power, the width and length of the FET need to be carefully picked. Traditionally, the method of directly increasing the length of the transistor is utilized and analyzed in [15] for low quiescent power, as shown in Fig. 9(a). However, the large length of the
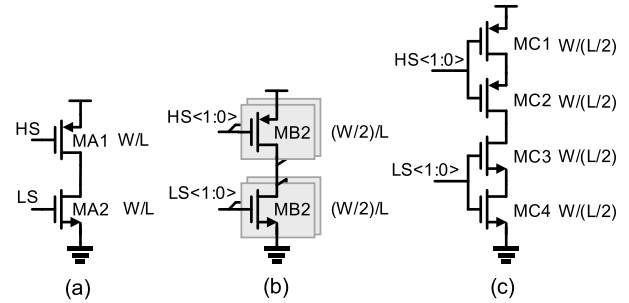

Fig. 9. Power stage optimization methods. (a) Traditional length modulation [15]. (b) Width split technique [25]. (c) Length split technique [29].

CMOS inevitably increases the gate capacitance, which incurs extra switching loss and degrades the efficiency at heavy load with PFM control. The gate width split technique is introduced in [25] to balance between conduction loss and switching loss targeting on an output power range from 500 μA to 20 mA, as shown in Fig. 9(b). At heavy load, more power stage FETs are turned on to decrease the conduction loss, while in PFM, they are turned off to decrease switching loss. However, in the nanowatt power range, when leakage power is dominant, the width split method has no ability to suppress the leakage. Hence, by leveraging the stack effects [26], [29], we implement a length split technique to balance the switching loss and leakage power, as shown in Fig. 9(c). Since the leakage current from PMOS of the power stage partly flows into the load side, which can be regarded as the load charging current, here, we only consider the SWD to GND leakage loss.

Fig. 10 shows the simulated power stage leakage power and estimated area when we use a traditional structure with a size of W/L versus the length split technique with a $W/(L/2)$ for each split FET. When the length is small, the length split technique may suffer from short channel effects leading to
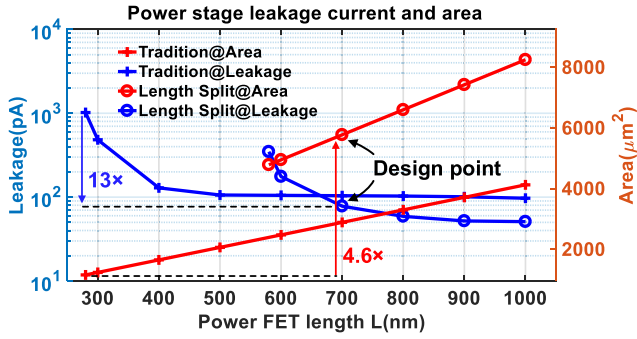
Fig. 10.   Simulated power stage leakage loss and estimated area cost for traditional length modulation versus length split techniques at $V_{\mathrm{IN}} = 1.5$ V and $V_{\mathrm{OUT}} = 0.5$ V.

large leakage current from SWD to GND. However, as the channel length increases, the length split scheme achieves better leakage suppression ability compared to the traditional length modulation. When V_{OUT} is 0.5 V and V_{IN} is 1.5 V, at 700-nm length, the stacked FETs have a 350-nm length and leakage is 78 pA, while the traditional length modulation has a 104-pA leakage at the same transistor length. Furthermore, by always turning on one of the two stacked FETs at heavy load, the proposed structure can achieve 40.4% less switching loss in simulation when $V_{\mathrm{IN}} = 1.5$ V and output power is 250 nW. In addition, compared with the minimal length transistors, the length split technique with 700-nm length can achieve 13× smaller leakage current with a 4.6× area cost.

For the length split technique, each power FET requires a dedicated driver for equal transition time [25] to avoid potential timing glitches such as deadtime mismatch caused by the HS/LS feedthrough, which increases the number of drivers. Therefore, the driver stage takes a large portion of leakage, which needs to be optimized. Drivers with smaller size have less leakage and gate capacitance but lack driving ability, which leads to large transition time when turning on/off the power FET and increases conduction loss, especially when the inductor current is at the peak. To balance the tradeoff, as shown in Fig. 11(a) and (b), the proposed SuWd driver minimizes the pulling down transistors for low quiescent power while maintaining the pulling up ability to achieve negligible penalty in conduction loss since the long transition time only happens when inductor current is still small. Therefore, for the HS driver, the design is straightforward where a smaller NMOS (8 μm/500 nm) can be selected, while the PMOS stays constant (80 μm/300 nm) at the last stage. For LS driver, the PMOS desires small leakage and large driving ability at the same time. Therefore, we increase both the width and length (100 μm/500 nm) for the PMOS of the driver. To avoid large reverse current at the ZCS point, a medium size (16 μm/300 nm) is selected for the NMOS. Compared to a traditional 300-nm length fan-out-four (FO4) driver, as shown in Fig. 11(c), the simulated result shows that it can improve the efficiency by 3%–4% at light load due to the transistors with larger length on the leakage path. At heavy load, the efficiency is also improved by 1%–2% since smaller size NMOS of the driver decreases the switching loss.
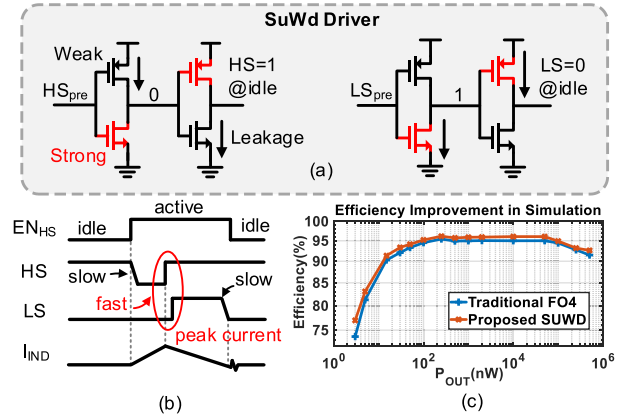

Fig. 11.   (a) Schematic of the proposed SuWd driver circuit and leakage path. (b) Related timing waveform and principles. (c) Efficiency improvement compared with traditional 300-nm length FO4 drivers.

C. Load-Transient Detector and Asynchronous Timing Generator

Fig. 12(a) shows the schematic of the asynchronous load-transient detector (LTD). The LTD consists of a CT comparator and a D flip-flop (DFF) to store the $\mathrm{EN_{FLTR}}$ signal. The CT comparator uses an amplifier-based structure with 50-pA bias current, including 4-bit offset tuning bits to generate a guard band, ΔV_{GB}, as shown in Fig. 7. To generate the maximal clock frequency for DVFS tracking, the APG has two separate loops to for up-tracking and down-tracking, as shown in Fig. 12(b). In the FLTR and DVFS mode, $\mathrm{CLK_{UP}}$ and $\mathrm{CLK_{DN}}$ are all set at 1 to make sure that the clock does not change during mode transition since mode transition happens at the rising edge of the $\mathrm{CLK_{BUCK}}$. For up-tracking, the falling edge of LS, which represents the completion of power delivery, generates a negative pulse at $\mathrm{CLK_{UP}}$ to enable the next power delivery. Similar schemes could be used for $\mathrm{CLK_{DN}}$ generation. However, in our design, a simpler oscillating scheme is used. When $\mathrm{CLK_{BUCK}}$ is 0, the LATH resets the $\mathrm{EN_{BUCK}}$ and DONE signals. During comparison, either DONE or $\mathrm{EN_{BUCK}}$ goes up to 1 according to the input voltages. Therefore, during the down-tracking when $V_{\mathrm{REF}} < V_{\mathrm{OUT}}$, the DONE always toggles between 0 and 1. Also, this feature is used to create an oscillating loop for $\mathrm{CLK_{DN}}$ generation.

Fig. 12(c) shows the simulated delay of the CT comparator under different input voltage differences and bias current. The two knobs significantly affect the speed of the comparator. To tradeoff between the speed and power, a 50-pA current and 20–50-mV programmable guard band is used for our design.

D. Pulse Generators

Fig. 13 shows the pulse generator schematic and design optimization for parasitics, which can deteriorate the power efficiency of the dc–dc converter. The HS pulsewidth is generated at the rising edge of $\mathrm{EN_{BUCK}}$ controlled by the time that the pulse generator needs to charge X_{CHG} from 0 to the threshold, which is around $V_{\mathrm{IN-REAL}}/2$. The charging time is dependent on the RC constant, which is fine-grained tuned by a

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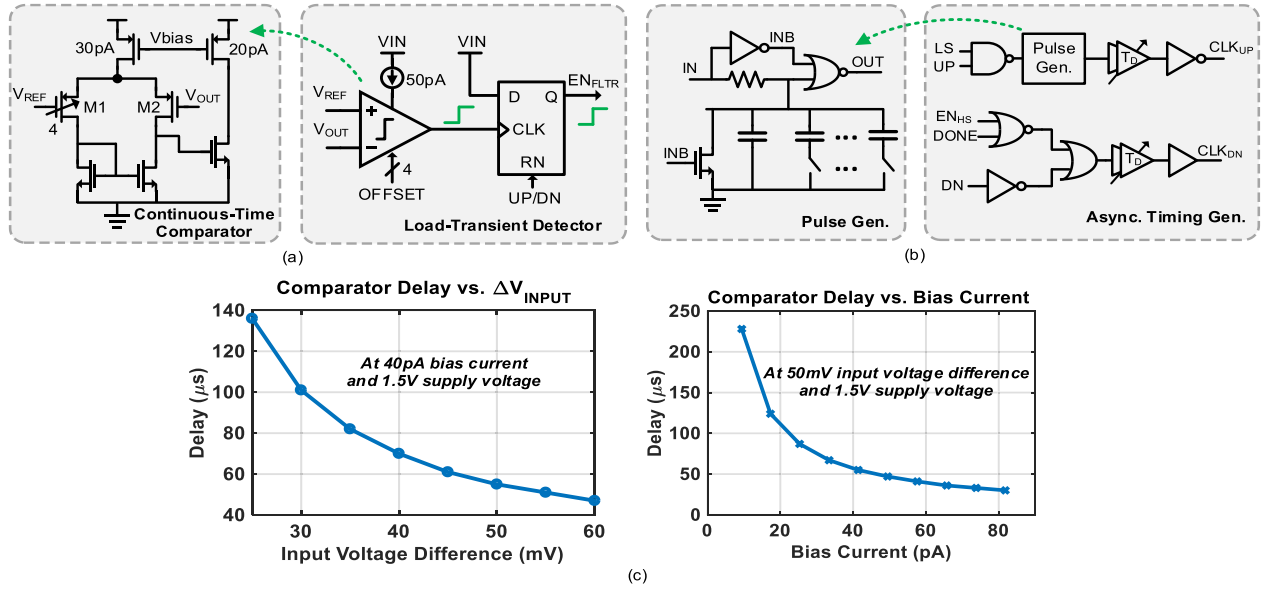

Fig. 12. (a) Schematic of the LTD with a CT amplifier-based comparator. (b) Schematic of the asynchronous timing generator with a pulse generator. (c) CT comparator delay versus input voltage differences and bias current.
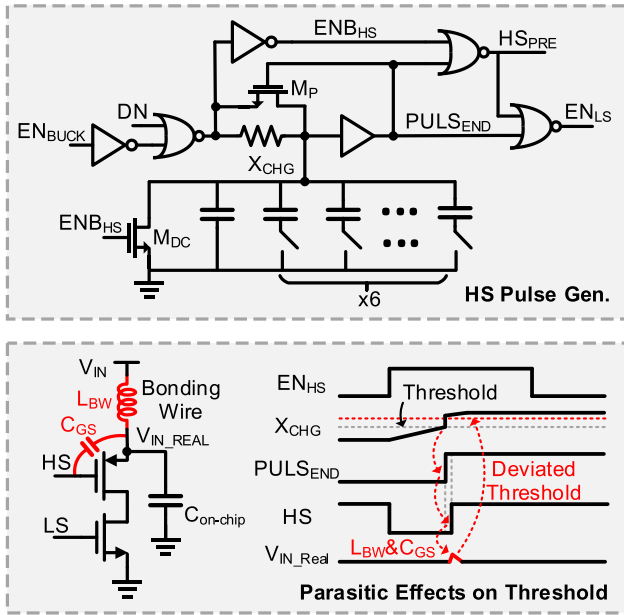

Fig. 13. Schematic of the pulse generator with an extra MP to solve the pulse generator threshold deviation caused by the parasitic CGS and bonding wire inductance at the rising edge of HS signal.

6-bit capacitance tuning bit [15]. The DN signal is also added as an input signal of HS pulse generator. Referring to Fig. 8, EN_{BUCK} goes to 1 first, and then, the MC detects it at the rising edge of the delayed clock signal, CLK_{BUCKD}. To avoid the down-tracking mode and power delivery happening at the same time and causing short-circuit current, the pulse generator will not be enabled until DN goes back to 0. Therefore, there is no power delivery operation at the end of the down-tracking mode if CLK_{OSC} is 0, as shown in Fig. 6.

Due to the large parasitic C_{GS} from the large power FET, bonding wire parasitic inductance, and picofarad-level on-chip decoupling capacitance, when X_{CHG} charges up to the threshold and HS goes from 0 to 1, the large C_{GS} and inductor remaining current causes the supply voltage, V_{IN_REAL}, bumping up to a higher voltage value, which causes the threshold to go up as well. This leads to ringing and generates a large short-circuit current at the power stage degrading the efficiency. Therefore, an extra transistor M_P (shown in the top of Fig. 13) is added to expedite the charging speed of X_{CHG} once it reaches the threshold. Considering the delay time introduced by the drivers, M_P has enough time to charge X_{CHG} to a safer voltage value before HS flips if M_P is large enough. After EN_{BUCK} goes down to zero, the pulse generator gets reset by the transistor M_{DC}. This is important, because for FLTR and DVFS up-tracking, when the clock goes to 0, the LATH and the pulse generator need to be reset and ready for next power delivery. The LS pulse generator uses a similar structure to generate the pulse but without the feedback M_P transistor.

E. Clock and Bias Generator

The clock generator is implemented by a CS-OSC with optimized driver stage, shown in the top of Fig. 14. The CS-OSC has benefits of ultra-low quiescent current but suffers from weak driving abilities and large short-circuit currents at the output driver stages. To improve the driving ability with low power cost, capacitances are added at last CS stages to expedite the transition and the normal buffer stage utilizes the stacked drivers to suppress short-circuit current. The bottom of Fig. 14 shows the simulated power consumption of the CS-OSC when C_2 increases at different values of V_{IN}. The tradeoff exists between the short-circuit current at the driver stage and the extra power needed to charge/discharge the
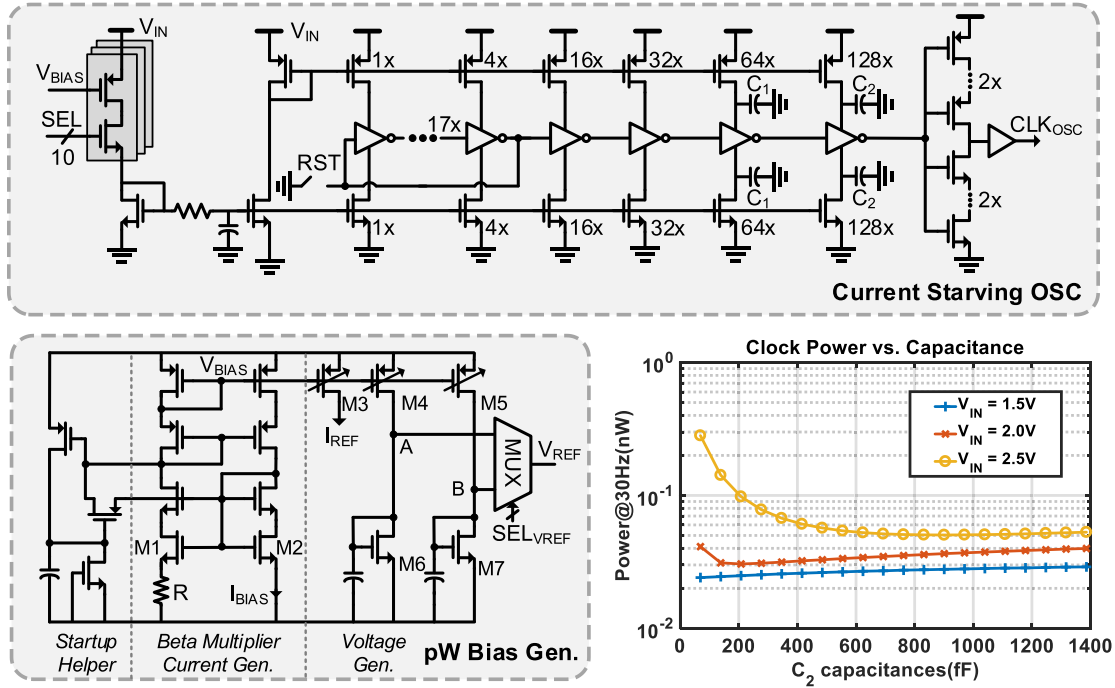
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Fig. 14. Schematic of the CS-OSC and BG, and simulation results of the impact from C_2 capacitance across V_{IN}.

added extra capacitors. In our design, 600-fF C_2 value is selected to balance the tradeoffs, which achieves 25.2-pW power at 20 Hz and 1.5-V V_{IN}. The 10-bit bias current tunability is added to cover a range of 20 Hz–78.8 kHz according to the simulation. The bias generator (BG) utilized a beta multiplier current reference to generate supply-independent current and voltage references. The voltage reference value can be calculated using the following equations. The current flowing through M1 and M2 is equal due to the PMOS-based current mirror. The bias current can be resolved by using the following equation:

$$\sqrt{\frac{2I_{BIAS}}{\mu_n C_{ox}(W_2/L_2)}} + V_{TH2}$$
$$= \sqrt{\frac{2I_{BIAS}}{\mu_n C_{ox}(W_1/L_1)}} + V_{TH1} + I_{BIAS}R \quad (7)$$

where I_{BIAS} represents the bias current of M1 and M2, μ_n represents the carrier mobility, C_{ox} represents the gate oxide of the transistor per unit area, and W/L represents the ratio of transistor width and length. Then, M4 copies the current reference to generate a voltage reference through M6. The reference voltage can be solved by using the following equation:

$$V_A = V_{GS,M6} = \sqrt{\frac{2I_{BIAS}}{\mu_n C_{ox}(W_6/L_6)}}$$
$$= \sqrt{\frac{4*(\sqrt{\frac{L2}{W2}} - \sqrt{\frac{L1}{W1}})^2}{(\mu_n C_{ox})^2(W_6/L_6)R^2}}. \quad (8)$$

With a 30-MΩ resistor, the BG works across 1.4–2.5 V and achieves 397 pW at 1.5-V supply in simulation. For DVFS

reference, two voltage references with 6.4-pF on-chip decoupling capacitors are connected to a MUX for reference selection. When SEL_{VREF} changes, the BG changes the voltage through the MUX and the MC enters DVFS mode to track the new reference voltage.

F. Adaptive Deadtime Controller

SVRs need a deadtime between HS and LS pulses to prevent short-circuit current. If the deadtime is too long, the SWD, in Fig. 15, will go down to negative voltage value (near negative V_{TH}) to force M2 on which causes a large conduction loss. If the deadtime is too short, the switching loss will increase [27], [28]. The ideal situation is to turn on the power stage NMOS right after the SWD node reaches zero. Besides, due to the process variation and large supply voltage range, the deadtime usually varies and is tuned manually traditionally, which is not desired in real applications and a large scale of deployment. In [27], the deadtime is adaptively tuned by indirectly detecting the SWD point to decide the moment to enable the LS driver, but it requires an extra bias current, which is not suitable for nanowatt-level low quiescent power dc–dc converter. In this work, we proposed a switch capacitor-based adaptive deadtime controller (ADTC) shown in Fig. 15, which consists of a SC-based pre-charger, a comparator, and a digital counter. The V_{DT} node is first pre-charged to a fixed programmable voltage, and, during deadtime, to maintain the inductor current, I_L, the voltage at SWD reduces from V_{IN} to a negative voltage to generate I_{LS}. Adding a small size of transistor M3 in parallel with M2 generates a small current I_{DT}, which discharges the C_{PRE} capacitor. The time that needs to discharge V_{DT} to GND through I_{DT} is the time that the SWD is at around negative V_{TH}.
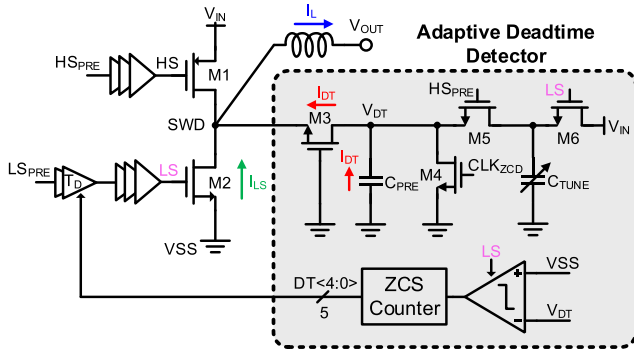
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Fig. 15.   Schematic of the proposed ADTC.

Fig. 16.   Chip micrograph of the buck converter.

In this design, M2 and M3 keep the same length, but the width of M3 is 1/375 of M2 making I_{DT} equal to $I_{LS}/375$. By setting proper C_{PRE} and C_{TUNE} values, the deadtime can be adaptively tuned by the ADTC through the delay cell, T_D. Compared with the traditional work, the SC-based ADTC utilizes the existing HS and CLK_{ZCD} as its clock source achieving low area and power overhead, and at the same time, it can scale its power based on the load current since the HS pulse frequency is proportional to the load power.

IV. EXPERIMENTAL RESULTS

The buck converter is fabricated in a 65-nm CMOS process. The die photograph is shown in Fig. 16 with an active area of 0.237 mm^2. Fig. 17 shows the testing setup. The chip is packaged and tested with a 100-pin quad flat no-lead (QFN) socket. The off-chip components are the 22-μH buck converter inductor, from Coil-Craft LPS5030-223MRC (4.9 mm × 4.9 mm × 3 mm), a 4.7-μF output decoupling capacitor C_{OUT} (0805 package size), and a 10-μF input decoupling capacitor C_{IN} (0805 package size). A Keithley 6430 Sub-Femto Remote Sourcemeter is used to measure the quiescent power from all the blocks.

A. Load-Transient Response and Fast DVFS

The measured load-transient response is shown in Fig. 18(a) and (b). By connecting the output of the buck converter to an 840-Ω off-chip load resistor, a current step can be provided to measure the load-transient response. When the load step changes from 45 nA to around 1 mA, the voltage droop is 56 mV and the settling time is 183 μs, where the sum of T_{DISCH} and T_{COMP} takes 173 μs, and $T_{UP-TRACKING}$ takes 10 μs. As we analyzed in Sections II-C and III-C, T_{DISCH} and T_{COMP} take most of part of the settling time. After the output voltage drops below the guard band (<56 mV), the CT comparator detects the voltage drop and its output changes after a delay time. During the delay time, V_{OUT} keeps decreasing. Then, after the FLTR is enabled, it takes 10 μs for the output voltage to be charged to the reference. As a comparison, when the FLTR function is disabled, even for a small 7- to 105-μA current step, the output voltage has a 400-mV voltage droop and 33.8-ms settling time due to the slow synchronous feedback loop, as shown in Fig. 18(c). When
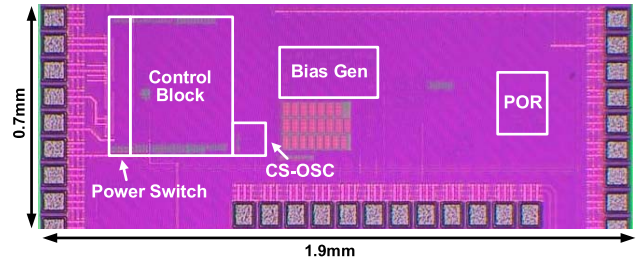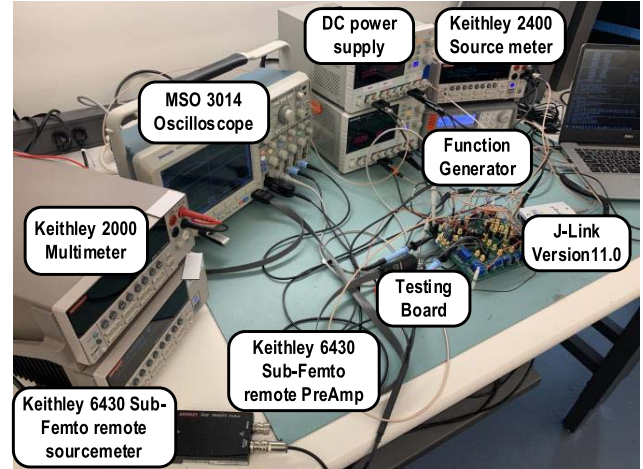

Fig. 17.   Testing and measurement setups.

the load current steps down from 1 mA to 45 nA, as shown in Fig. 18(a), there is no voltage droop observed, which matches with the analysis in Section II-C.

The measured fast DVFS tracking is shown in Fig. 19. Through a JTAG debugger (SEGGER J-Link) and RISCV processor, we changed EN_{DVFS} and SEL_{VREF} at the same time to let the MC enable the DVFS tracking. The fast DVFS tracking achieves 10.57 μs for an 88-mV up-tracking and 19.81 μs for a 92-mV down-tracking. Without the fast DVFS function, measured up-/down-tracking time increases up to 923 ms and 2.65 s, respectively, due to the slow feedback loop and small discharging load current. A ring OSC, VCO_{LOAD}, which provides the clock frequency to the loads, is used in the testing to show the frequency scaling ability. As voltage scales down, the frequency of the ring OSC, powered by the buck converter, also decreases from 2.2 to 0.95 kHz, achieving dynamic frequency scaling. The undershoot and overshoot voltage is less than 4 mV, which is only 0.5% of V_{OUT} at 700 mV and is close to the measured ripple voltage.

The speed of the DVFS and load-transient response is affected by the off-chip decoupling capacitance value, load current, and the energy delivery speed to the load. Smaller capacitance is helpful for achieving faster transition speed. However, it causes larger voltage ripples at the output. Larger V_{IN} is desired for both reference up-tracking and down-tracking because it increases V_{GS} of M5 (in Fig. 6), allowing a large discharging current. Also, higher supply increases the
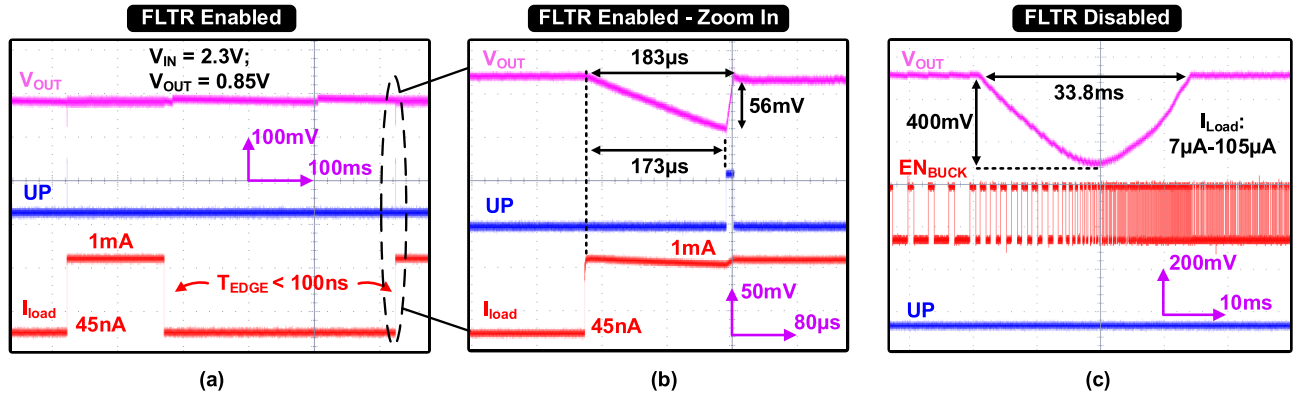
Fig. 18. Measured transient waveform for FLTR. (a) FLTR waveform for an output current step from 45 nA to 1 mA. (b) Detailed waveform from (a). (c) Waveform with FLTR disabled for current step from 7 to 105 μA.
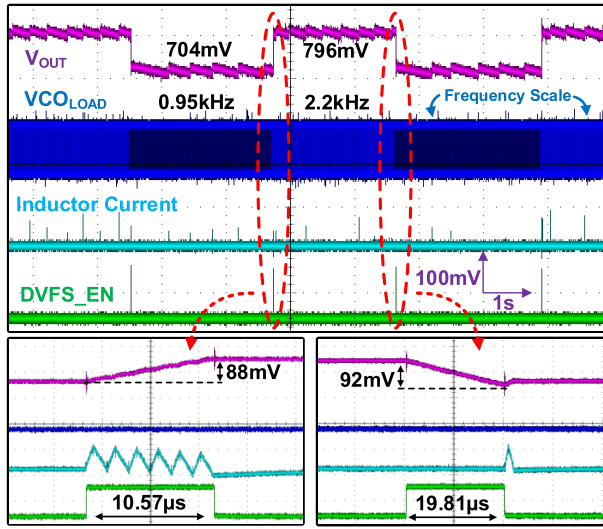

Fig. 19. Measured transient waveform for DVFS up and down reference tracking along with the dynamic frequency scaling.
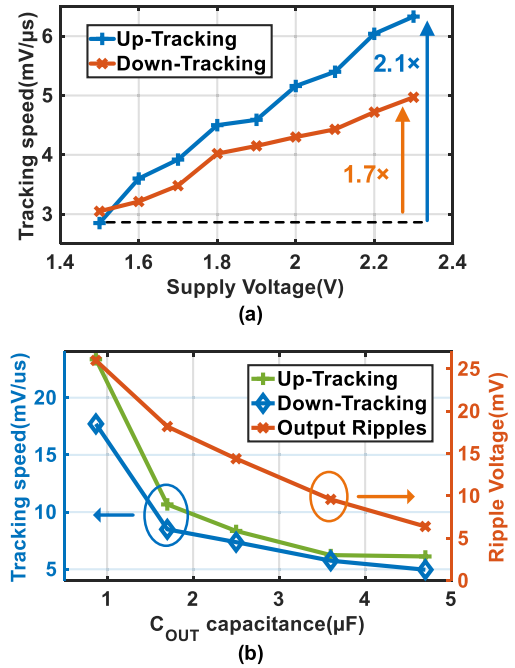

Fig. 20. (a) Measured DVFS tracking speed versus supply voltage changes. (b) Tradeoffs between the tracking speed and ripple voltage in terms of off-chip output capacitance.

inductor peak current to increase the energy per power delivery according to (2), (3), and (6). Notably, unlike the traditional method where the power stage LS FET is used to discharge the current from V_{OUT} to GND. In this design, an extra tunable transistor, M5, is added to control the discharging current amplitude. The power stage FET can generate a large discharging current due to its large W/L ratio. For example, when $V_{IN} = 2$ V and $V_{OUT} = 0.8$ V, the power FET LS transistor can discharge a 4.7-μF capacitor from 0.8 V to 700 mV within 600 ns with a near 800-mA discharging current. This requires the LATH to operate at 34 MHz at least for a 4× oversample rate if the undershoot needs to be less than 20 mV. To meet this high operating frequency requirement, the LATH needs to have larger W/L and bias current for faster speed, which increases quiescent current and dynamic power loss. Therefore, an extra transistor M5 with a small 20 μm × 60 μm area overhead is implemented to tradeoff between speed and power. Fig. 20(a) shows the measured supply voltage versus tracking speed. When supply voltage increases from 1.5 to 2.3 V, the up-

tracking and down-tracking can achieve 2.1× and 1.7× faster speed. Fig. 20(b) shows the measured tradeoffs between the speed of the DVFS transition and the output voltage ripples across different off-chip decoupling capacitance. When the off-chip decoupling capacitor changes from 4.7 to 0.87 μF, though the ripple voltage increases, the tracking speed achieves 3–5× improvement.

B. Power Breakdown and Efficiency

Fig. 21 shows the simulated power loss breakdown at light load (25 nW) and heavy load (10 μW). The control power of the circuits takes only 7% of the total power loss at the heavy load. When the output current decreases down to 25 nW. The control power increases up to 46% of the total power loss

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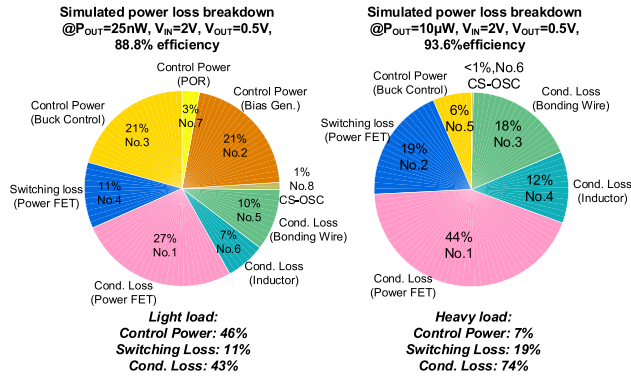

Fig. 21.   Simulated power loss breakdown at light load and heavy load with three categories: conduction loss, switching loss, and control power.
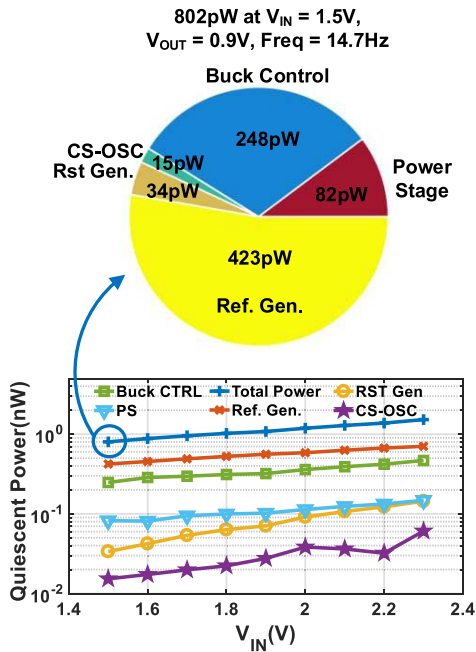

Fig. 22.   Measured quiescent power across V_{IN} from 1.5 to 2.3 V for all the subblocks and power breakdown at V_{IN} = 1.5 V.

due to the infrequent power delivery operation. If the output power keeps decreasing further, the proportion of switching loss and conduction loss will decrease as well since fewer power delivery operations are needed and the control power takes more proportion of the total power loss. Therefore, decreasing the quiescent power of the circuit is critical for light-load efficiency improvement.

The quiescent power of the buck system is measured when there is no output power and the system clock frequency is modulated to its lowest value, 14.7 Hz. Fig. 22 shows the measured quiescent power across different values of V_{IN} for different sub-blocks and the lowest quiescent power for the buck converter is 802 pW at 1.5-V V_{IN}. The pie chart shows the detailed power breakdown of the buck converter. Due to the length split power stage, clock driver optimization, and reusing control paths, the buck converter control, clock, and
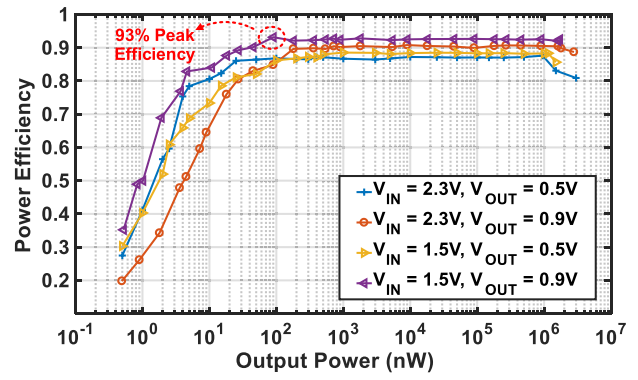

Fig. 23.   Measured power efficiency across different values of V_{IN} and V_{OUT}.

power stage in sum take 43% of the total quiescent power, while the BG takes 52% of the total power. Fig. 23 shows the measured power efficiency across different values of V_{IN} and V_{OUT}, with a 93% peak efficiency. The buck converter achieves a measured dynamic range from 0.5 nW to 2.75 mW, which provides over six orders of magnitude and still keeps an 80% efficiency down to 4.3-nW output power.

C. Comparison to State of the Arts

Table I compares this work with state-of-the-art picowatt–nanowatt dc–dc converters, including the inductor-, SC-, and LDO-based converters. Compared with the LDO and SC-based converters, our converter achieves higher efficiency and wider dynamic range. However, in terms of area consideration, the LDO and SC usually only require one off-chip decoupling capacitor at the output [11], [12] or can be off-chip component-free [31]. For inductor-based dc–dc converter, an extra microhenry-level off-chip inductor along with microfarad-level decoupling capacitors at both input and output is needed for ULP applications as we analyzed in Section II-B. Nevertheless, the volume of the off-chip capacitors can be scaled to <1 mm³ level for most commercial products, for example, 10-μF ceramic capacitors with 0402 footprint (1.00 mm × 0.50 mm) [32]. Also, the inductor (47 μH) can reach a sub-cm³ size as well [33]. Therefore, the proposed inductor-based sub-nW dc–dc converter is still one of the best candidates for ULP IoT cm³ level applications due to its high efficiency, wide dynamic output range, and ultra-low quiescent power.

Fig. 24 benchmarks this work against prior nanowatt- and picowatt-level dc–dc converters in terms of dynamic power range and quiescent power with a consideration of FLTR and DVFS tracking capability. Our buck converter achieves the highest peak efficiency and widest dynamic range among all the sub-nW SVRs. Due to the hybrid loop control scheme, the buck converter also features fast DVFS and FLTR which previous work does not support. In addition, the buck converter integrates all the features on chip, including the proposed ADTC, PoR, BG, and clock generator. All the measured performance and integrated features make the buck converter well suited as the power management solution for ULP IoT applications.

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TABLE I

COMPARISON WITH STATE-OF-THE-ART PICOWATT–NANOWATT DC–DC CONVERTERS

	[12] JSSC'17	[30] ISSCC'16	[11] ISSCC'19	[14] JSSC'14	[16] JSSC'16	[23] JSSC'16	[15] JSSC'17	[17] JSSC'18	This Work
Technology (nm)	65	180	65	180	130	65	65	65	**65**
Topology	SC(Boost)	SC(BUCK)	DLDO	SVR(Boost)	SVR(Buck-Boost)	SVR(Buck)	SVR(Buck)	SVR(Boost)	**SVR(Buck)**
Regulation Scheme	ACRM	Binary-Reconfig	ABS-SLS	PWM	PFM	PWM/PFM/AM	PFM	PFM	**PFM/LM/PWM**
L (µH) / C_{OUT} (µF)	N/A	N/A	N/A/0.1	47/0.2	47/NR	4.7/4.7	47/0.35	47/1	**22/4.7**
V_{IN} (V)	0.25-0.65	0.9-4	0.5-1	0.02-0.07	2.9-4.1	0.55-1.0	1.2-3.3	0.08-0.8*	**1.5-2.3**
V_{OUT} (V)	3.8-4	0.6 1.2 3.3	0.4-0.95	1	0.8-1.1	0.35-0.5	0.7-0.9	0.7-1.1	**0.5-0.9**
Quiescent Power (nW)	0.015	4.6*	0.373	0.544	3.2	50.7*	0.24	1.05	**0.801**
Peak Efficiency (%)	50	81	V_{OUT}/V_{IN}	53	87	92	92	78	**93**
Dynamic Range ($P_{LOAD, MAX}$ / $P_{LOAD, MIN}$)	45.2pW - 0.6µW* (1.3×10^4)	5nW-500µW (1×10^5)	0.32-121.5µW (3.8×10^5)	0.544-4nW (7.4)	10nW–1µW* (1×10^2)	45nW-9mW (2×10^5)	0.4nW-0.8mW (2×10^6)	0.12-160nW (1.3×10^3)	**0.5nW-2.75mW (5.5×10^6)**
Dynamic Range with η > 80%	No	No	3.6nW-121.5µW	N/A	40nW-1µW*	13.5µW-9mW	0.9nW-0.8mW*	N/A	**4.3nW-2.75mW**
Fast Load response	No	Yes	Yes	No	No	Yes	No	No	**Yes**
Voltage droop @ ΔI_{LOAD}	N/A	160mV@1µA	76.5mV@0.27mA	40mV*@N/R	N/A	N/A	30mV*@0.4mA	N/A	**56mV@1mA**
Settling Time @ ΔI_{LOAD}	N/A	>20ms@1µA	48µs@0.27mA	>40s@N/R	N/A	N/A	2ms@0.4mA	N/A	**0.183ms@1mA**
Fast DVFS (T_{UP}/ T_{DOWN})	No	No	No	No	No	No	No	No	**Yes (6µs/10.76µs†)**
Off-chip Components	1 cap	N/A	1 cap	2 caps + inductor + antenna	2 caps + inductor	1 cap + inductor	2 caps + inductor	3 caps + inductor	**2 caps + inductor**

*Observed/Calculated from the waveform
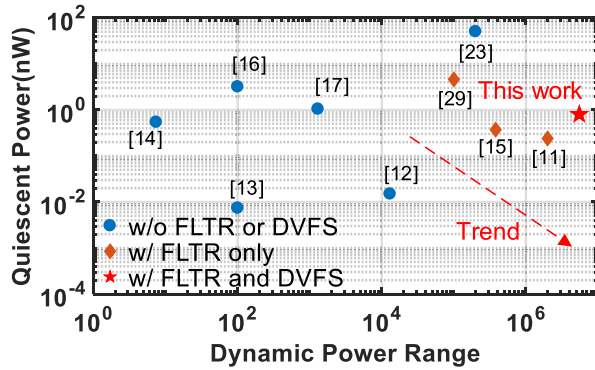†For a 50mV reference tracking step

Fig. 24. Comparison with the existing nanowatt dc–dc converters in terms of dynamic power range and quiescent power with a consideration of FLTR and DVFS tracking capability.

V. CONCLUSION

To achieve high efficiency, low quiescent power, and wide dynamic range while supporting fast DVFS and FLTR, we presented a sub-nW buck converter with hybrid synchronous and asynchronous loop control. The synchronous loop is able to achieve frequency modulation and output regulation with high efficiency and the asynchronous loop generates the maximal timing frequency to achieve fast FLTR and DVFS. By reusing the existing signals and blocks and multiplexing the DVFS up-tracking and FLTR paths, the two control loops achieve 248-pW power overhead in total. The power stage and gate drivers are analyzed and optimized by utilizing the length split techniques and SuWd scheme to achieve higher efficiency and lower leakage. The clock driving stage is optimized to suppress the short-circuit current, achieving 15-pW lowest power and 20-Hz-to-78.8-kHz frequency range. An ADTC with load-proportional scaling is proposed to enhance the efficiency. The measurement results show that this buck converter achieves an 802-pW quiescent power at 1.5-V V_{IN},

93% peak efficiency, and 5.5×10^6 dynamic range with fast DVFS and FLTR. This buck converter shows an optimal power management solution for powering ULP IoT SoCs.

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