A Single-Supply 6-Transistor Voltage Level Converter Design Reaching 8.18-fJ/Transition at 0.3–1.2-V Range or 44-fW Leakage at 0.8–2.5-V Range

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***Abstract*—This letter presents an ultralow-leakage level converter design based on dynamic leakage-suppression (DLS) logic for battery-less Internet-of-Things systems. The design is compact and simple, consisting of six transistors arranged as two digital buffers in series and requires only a single voltage supply corresponding to the high-voltage domain. We analyze the dc switching characteristic of the proposed level converter to create a design guideline which we use to implement two designs that target core (0.3-V to 1.2-V conversion) and I/O (0.8-V to 2.5-V conversion) voltage domains. We fabricated the designs in 65-nm CMOS and present measurements from 17 dies. The core design achieves 8.18 fJ per transition with 2.56 pW of leakage power, while the I/O design achieves 54.23 fJ per transition and 44 fW of leakage power.**

***Index Terms*—Dynamic leakage suppression logic, leakage, level converter, level shifter, voltage level.**

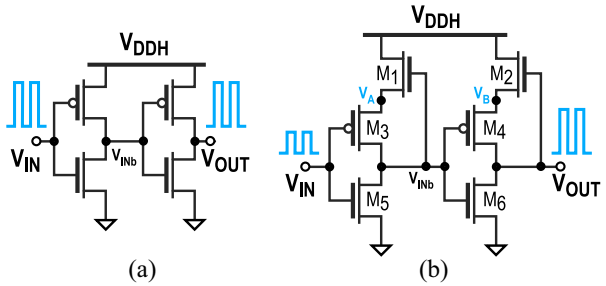

Fig. 1. Schematic of (a) traditional digital buffer and (b) proposed level converter.

I. Introduction

Voltage level converters are essential building blocks that facilitate interconnection of circuits and I/O pads operating at different supply voltages. The popularity of voltage scaling for power reduction over the last two decades has created a demand for wide-range level conversion that can translate signals from subthreshold digital logic levels (0.5 V and below) to typical I/O levels of 1.2, 1.8, or 2.5 V. A large number of designs have emerged to meet this demand by using differential cascode or current mirror-based architectures to achieve wide conversion ranges with delays in the ns-range and only 100s of pW of leakage power [1]–[8].

Efforts to further reduce power consumption have continued with the growth of the Internet-of-Things (IoT), and recently a new class of battery-less IoT sensing systems have emerged that operate at only a few nW or less to sustain operation purely from harvested energy [9], [10]. To achieve this performance, these battery-less systems prioritize low-leakage operation, spend large amounts of time in standby, and run at slow clock speeds in the Hz to kHz-range to minimize dynamic power consumption. Wide-range voltage conversion is still required by these systems, but existing level converter designs target MHz-range operating speeds and consume more leakage power than is desirable for battery-less operation.

This letter presents an ultralow-leakage level converter for battery-less IoT systems based on a design first demonstrated in [11]. The proposed level converter is based on dynamic leakage-suppression (DLS) logic [12] and functions similarly to a digital buffer [Fig. 1(a)] with skewed logic thresholds, where the employed DLS technique significantly reduces static current dissipation caused by the low-voltage input signal. This approach also allows the level converter to operate from only a single supply for the high-voltage domain (V_{DDH}) which reduces routing congestion compared to the existing designs that require an additional low-voltage supply (V_{DDL}) from the input signal domain. The proposed design requires only six transistors which helps to reduce area, and it can be designed for Core (0.3–1.2 V) or I/O (0.8–2.5 V) voltage domain operation.

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II. Proposed DLS Level Converter

Fig. 1(b) shows the schematic of the proposed level converter, which follows the architecture of a traditional digital buffer consisting of two cascaded inverters [Fig. 1(a)]. The traditional digital buffer on a 1.2-V (V_{DDH}) supply may be modified to operate from a 0.3-V (V_{DDL}) input signal by strengthening the nMOS and weakening the pMOS devices in each inverter such that their currents are equal at a logic threshold $V_{TRIP} \approx V_{DDL}/2$, but this leads to several hundred nA of static power dissipation due to short-circuit current through the pMOS when $V_{IN} = V_{DDL}$ or high subthreshold leakage current through the strengthened nMOS when $V_{IN} = 0$ V (Fig. 2).

To preserve the simplicity of the skewed-inverter approach but eliminate the sources of static power dissipation, we propose a modified inverter design based on the DLS technique that modifies the pull-up (PU) network by adding an nMOS header transistor between the pMOS transistor and the V_{DDH} supply rail. This resulting design contrasts with traditional DLS logic by the absence of the pMOS footer transistors. The gate of the nMOS header is controlled using feedback from the output of the inverter such that the header is enabled (shorted) when the PU network is active, and cutoff with a negative V_{GS} (ultralow leakage) when the PU network is inactive. As a result of this DLS behavior, it is possible to skew the PU and PD networks to achieve the desired V_{TRIP} without incurring static power penalties since the nMOS can be sized for low leakage while still being strong enough overpower the DLS-based PU network when $V_{IN} = 0$ V, and when $V_{IN} = V_{DDL}$ the DLS PU network will suppress short-circuit current.

A. DC Characteristics

Fig. 2 shows the schematic and simulated dc transfer characteristics of the proposed DLS-based inverter. When $V_{IN} = 0$ V, M_5 is cutoff with $V_{GS} = 0$, M_3 is active such that $V_A = V_{OUT}$ and, therefore, M_1 is also in cutoff with a $V_{GS} = 0$ V. Provided that the subthreshold leakage through M_1 is stronger than the subthreshold leakage through M_5, the PU network will keep V_{OUT} charged to V_{DDH} in the

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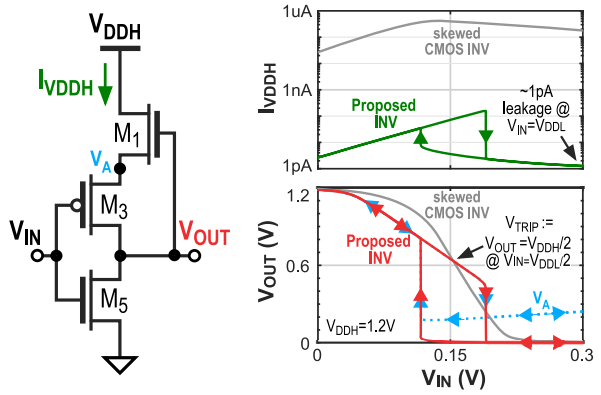

Fig. 2. Simulated dc transfer characteristics of the proposed DLS-based inverter operating from a 1.2-V supply with comparison to a skewed-sizing traditional CMOS inverter.

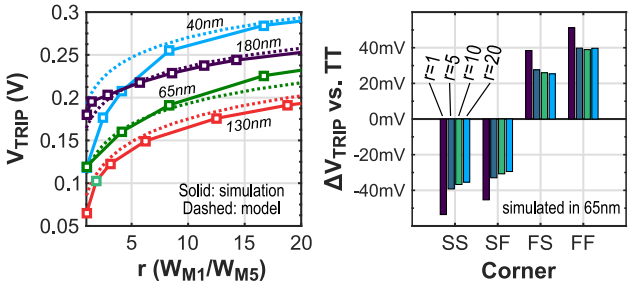

Fig. 3. Modeled and simulated DLS inverter logic threshold V_{TRIP} versus sizing ratio of M_1 and M_5 for multiple technologies in the TT corner (assuming a device selection such that $V_{\mathrm{th0},M1} < V_{\mathrm{th0},M5}$), and impact of process corner on V_{TRIP} value for different sizing ratios.

steady state as well during any noise events that would cause V_{OUT} to droop. The design approach to accomplish this will be discussed later in this section. When V_{IN} is increased, M_3 remains active but the subthreshold current through M_5 (now with $V_{\mathrm{GS}} > 0$) begins to overpower the leakage through M_1 ($V_{\mathrm{GS}} = 0$), which causes V_{A} and V_{OUT} to decrease together. This behavior continues as V_{IN} is further increased until an abrupt transition occurs due to a combination of: 1) M_5 strongly pulling V_{OUT} to $0V$; 2) M_3 pushing further toward cutoff, making it harder for V_{OUT} and V_{A} to remain equal; and 3) increased leakage through M_1 due to DIBL which tries to charge V_{A} above 0 V. After this reaction occurs, V_{OUT} is firmly settled at 0 V, while V_{A} settles at an intermediate value $0 < V_A < V_{\mathrm{DDH}}$ that is determined by the contention in leakage currents between M_1 and M_3. As a result of the positive voltage at V_{A}, both M_1 and M_3 have a negative gate voltage which significantly reduces their subthreshold leakage.

Now, we assess this transition in reverse, when V_{IN} switches from high to low. Once V_{OUT} has transitioned low, it remains fixed there due to the feedback on the gate of M_1, even if V_{IN} starts to decrease back toward 0 V. However, as V_{IN} continues to decrease further, the same chain reaction occurs where: 1) M_5 nears cutoff and will lack the strength to keep V_{OUT} pulled low; 2) M_3 becomes more conductive and allows V_{A} and V_{OUT} to equalize; and 3) subthreshold leakage through M_1 is able to charge the V_{A} and V_{OUT} nodes which creates positive feedback on its own gate. Once this abrupt transition occurs again, V_{A} and V_{OUT} equalize and both approach the V_{DDH} rail value as V_{IN} is decreased toward 0 V. This asymmetric switching behavior provides the inverter with a hysteresis that improves the noise margins for added stability at low input voltages. Note that this letter uses two cascaded inverters to maintain the signal polarity, but an inverting level-conversion operation could

	M1/M2	M3/M4	M5/M6
Core (0.3V – 1.2V)	LVT (W=8 x W_{MIN})	LVT (W=W_{MIN})	HVT (W=W_{MIN})
I/O (0.8V – 2.5V)	NA I/O (W=1.5 x W_{MIN})	I/O (W=W_{MIN})	I/O (W=W_{MIN})

Fig. 4. Device selection and sizing for the proposed level converter in 65-nm CMOS for core (0.3–1.2 V) and I/O (0.8–2.5 V) voltage domains.

be performed with the single inverter structure shown in Fig. 2. The leakage-driven transition results in rise and fall times that are several orders of magnitude greater than the traditional CMOS logic, but this is not an issue when driving DLS gates since they are not susceptible to short-circuit current.

To ensure that the inverter output transition occurs at a switching threshold V_{TRIP} that is compatible with the input domain V_{DDL}, we can follow the approach for the skewed inverter by choosing the relative sizes of M_1 and M_5 such that they are in equal contention when $V_{\mathrm{IN}} = V_{\mathrm{TRIP}} = V_{\mathrm{DDL}}/2$. Therefore, we equate the subthreshold currents of M_1 and M_5 assuming that $V_{\mathrm{IN}} = V_{\mathrm{DDL}}/2$ and $V_A = V_{\mathrm{OUT}} = V_{\mathrm{DDH}}/2$. The standard subthreshold current equation is given as

$$I_{\mathrm{DS}} = I_0 e^{\frac{(V_{\mathrm{GS}} - V_{th0} + \eta V_{\mathrm{DS}})}{nv_T}} \left(1 - e^{\frac{-V_{\mathrm{DS}}}{v_T}}\right) \tag{1}$$

where $I_0 \propto W/L$ is the current at threshold. Since the V_{DS} of each transistor is set to $V_{\mathrm{DDH}}/2$ ($\gg v_T$) for this calculation, we can neglect the final term of (1). For simplicity, we also assume that any difference in the subthreshold swing factor n and DIBL coefficient η of M_1 and M_5 will be negligible. Then, we obtain a sizing ratio r

$$r = \frac{W_{M1}}{W_{M5}} = e^{\frac{(V_{th0,M1} - V_{th0,M5} + V_{\mathrm{TRIP}})}{nv_T}}. \tag{2}$$

If we assume M_1 and M_5 to both have the same threshold voltage, then a V_{DDL} of 0.3 V ($V_{\mathrm{TRIP}} = 0.15$ V) requires M_1 to be sized around 73 times larger than M_5 , which would occupy a significant area. Instead, M_5 is kept as a minimum-sized high threshold voltage (HVT) device for low leakage, and M_1 is implemented with a low threshold voltage (LVT) device. The resulting r values are shown in Fig. 3 for several commercial technologies, and range around 1 to 5 for the targeted $V_{\mathrm{TRIP}} = 0.15$ V. Note that these results are independent of V_{DDL} and V_{DDH} as shown by (2). Lower r-values result in lower overall leakage due to smaller device sizes, but also slightly increases the susceptibility of V_{TRIP} to systematic process variation, assuming devices with different thresholds are equally subjected to the same process variations. Fig. 3 also shows the deviation of V_{TRIP} from the TT corner for different r-values ranging from 1 to 20. Since V_{TRIP} depends on M_1 and M_5 but not M_3, it is mainly sensitive to the nMOS corner. For r-values above 5, the variation in V_{TRIP} is limited to ± 40 mV across all corners. Fig. 4 shows a summary of the device thresholds and sizing for the core voltage domain (V_{DDH}=1.2) level converter in 65-nm CMOS. The same design and sizing approach is also implemented with thick-oxide devices for compatibility with the I/O voltage domain ($V_{\mathrm{DDH}} = 2.5$ V) with a targeted $V_{\mathrm{DDL}} \approx 0.8$ V. To maintain skewed threshold voltages between M_1 and M_5, we used native I/O devices (NA I/O) for the nMOS headers. Fig. 5 shows the simulated delay and leakage of the core and I/O designs across temperature, as well as their susceptibility to $+/-3\sigma$ of device mismatch at 20 °C in the TT corner.

III. Measurements

The proposed core and I/O level converter designs were fabricated in a 65-nm low-power process, occupying areas of 4.44 um^2 and 42.13 um^2, respectively. Fig. 6 shows the annotated micrograph and testing setup of the chip, which contains a single buffered level converter of each type for measuring delay, active power, and energy per

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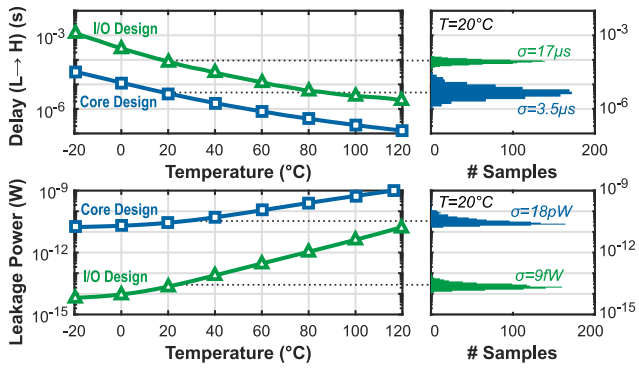

Fig. 5. Simulated delay and leakage power across temperature for both core and IO designs in 65-nm, with 1000-point Monte Carlo simulation at 20 °C for $+/-3\sigma$ of device mismatch. Core operation is from 0.3 to 1.2 V, and IO operation is from 0.8 to 2.5 V.

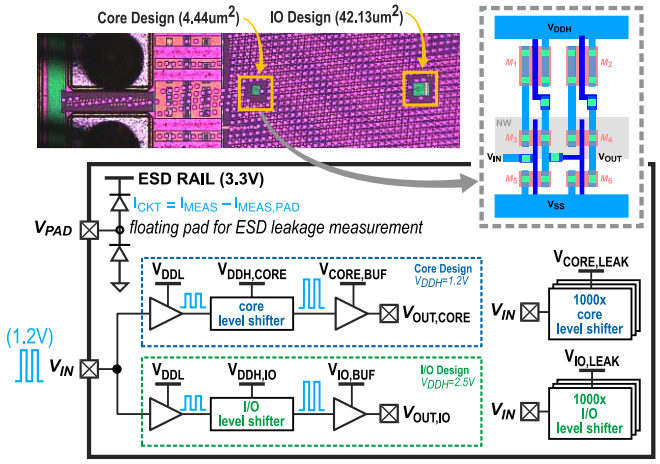

Fig. 6. Chip micrograph, core level converter layout, and test setup for delay, leakage, and power measurements.

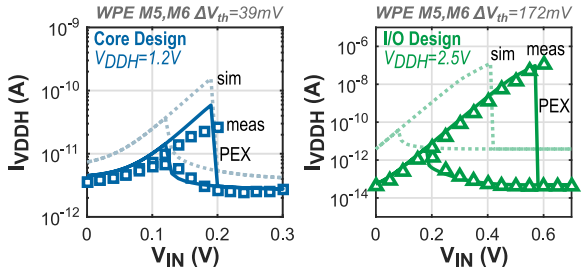

Fig. 7. Impact of WPE on dc transfer characteristic and leakage of core and I/O designs. Dashed lines show ideal simulation data, solid lines show parasitic-extraction (PEX) simulation data, and markers show measured data.

transition. Average leakage power for each design is measured from a structure containing 1000 parallel level converters. The high number of parallel level converters represents a better average measurement that accounts for within-die variation and additionally improves the measurement accuracy by increasing the order of magnitude of measured current from the fA/pA-range to the pA/nA-range which helps to reduce the impact of stray leakage currents in the testing setup. A floating measurement pad is included on each chip to further improve the measurement accuracy by subtracting the leakage contribution of the ESD protection diodes in the analog supply voltage pads, which averaged 360 pA and 28 pA across 17 dies for core and I/O-domain analog pads, respectively.

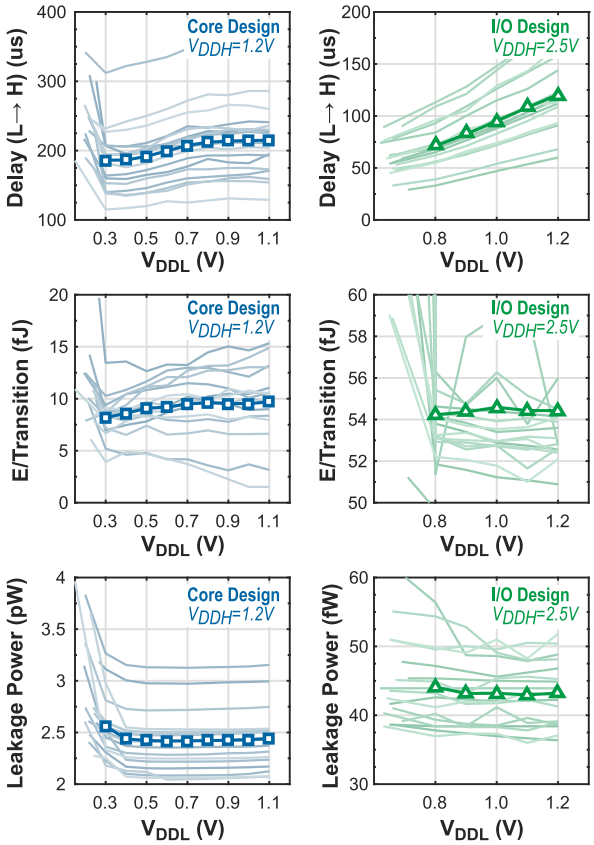

Fig. 8. Measured delay, energy per transition, and leakage power from 17 dies for both core and IO designs. Bold lines with markers show average values from all the measured dies.

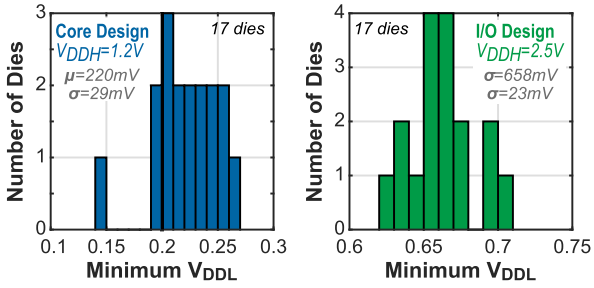

Fig. 9. Minimum operational V_{DDL} measured from 17 dies, shown for both the core and I/O designs.

Fig. 7 shows the measured dc transfer characteristic of the core and I/O designs with comparison to simulated results. Measurement results deviate from simulation due to the WPE causing an increase in the threshold voltages of M_5 and M_6 that reduces their leakage but also decreases V_{TRIP}. Equation (2) can be used to show that the decrease in V_{TRIP} is equal to the increase in threshold voltage of M_5 (or M_6). WPE significantly affects the I/O design, increasing the threshold voltage by over 150 mV which decreases leakage by 100× relative to simulation. The core design is less affected by WPE with its leakage only changing by around 2×. In both designs, extracting the layout (PEX) yields simulation results that better match measured data. Seventeen dies were measured at room temperature (23 °C), and Fig. 8 shows the delay, energy per transition, and leakage power versus the input voltage domain V_{DDL} of each individual die as well as the average values for both core and I/O designs across all dies. Both designs experience an increase in delay as V_{DDL} increases, while the energy consumption and leakage power remain nearly constant across V_{DDL} which is due to the absence of any devices in the design

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TABLE I
PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON

	This work		SSCL '20 [1]	TCAS-II '20 [2]	TCAS-II '19 [3]	SSCL '18 [4]	TCAS-II '17 [5]	TCAS-I '17 [6]	TCAS-I '15 [7]	JSSC '12 [8]
	Core design	IO design								
Technology	65nm		55nm	55nm	28nm	40nm	180nm	180nm	180nm	250nm
# of Required Volt. Supplies	1 (V_{DDH} only)		2 (V_{DDH},V_{DDL})	2 (V_{DDH},V_{DDL})	2 (V_{DDH},V_{DDL})	2 (V_{DDH},V_{DDL})	2 (V_{DDH},V_{DDL})	2 (V_{DDH},V_{DDL})	2 (V_{DDH},V_{DDL})	2 (V_{DDH},V_{DDL})
Area (um^2)	4.44	42.13	154	8.12	8.6	8.0	108.8	229.5	153.01	1880
VDDL (V)	0.3	0.8	0.30	0.12	0.04	0.12	0.10	0.40	0.3	0.23
VDDH (V)	1.2	2.5	2.50	1.2	1.0	1.1	1.8	1.8	2.5	3.0
Delay (ns)	186000	71100	523	17.86	10.1	15.5	31.7	29	167	10000
Leakage Power (pW)	2.56	0.044	256	73.95	6500	550	55	330	340	230
Energy per Transition (fJ)	8.18	54.23	60.5	26.59	5.2	4.2	173	61.5	188	5800

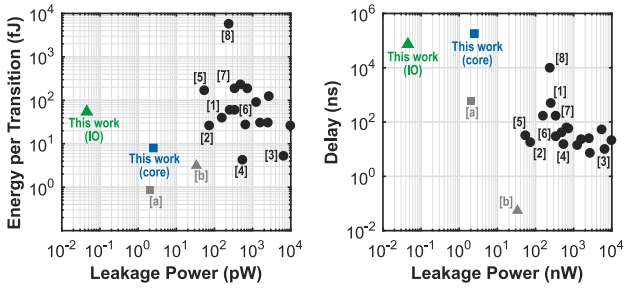

Fig. 10. Comparison with the existing level converter designs (shown by dark markers). As an added reference point for comparison, markers [a] and [b] show the performance of traditional digital buffer standard cells [from Fig. 1(a)] in the same 65-nm technology under normal operation at 0.3 V and 1.2 V supplies, respectively.

operating with V_{DDL} as their supply. Die-to-die variation in energy is due mostly to the variation in delay which dictates the integration time of leakage currents. The leakage-driven design sacrifices operating speed, causing both designs to incur conversion delays in the μs-range. However, leakage-constrained battery-less IoT systems operating at Hz-range frequencies can easily tolerate this leakage-delay tradeoff. Improvements to the delay could theoretically be made by increasing the leakage of the devices by using larger sizes, adding a forward body bias, or adding external leakage bias as in [10]. Fig. 9 shows the distribution of minimum operational V_{DDL} across all measured dies from both designs. The core design averages a minimum V_{DDL} of 220 mV, while the I/O design averages a minimum V_{DDL} of 658 mV, and both designs have comparable standard deviations between 20 and 30 mV.

Table I summarizes the measured performance of both the core and I/O designs and compares them to state-of-the-art low-leakage and low-energy level converters. Both designs presented in this letter achieve less leakage power than any previously published designs with measured verification. Both designs are highly energy efficient when compared to other designs at the same V_{DDH}. The I/O design achieves the lowest energy per transition when compared to other works in the 2.5-V domain, and the core design achieves within a few fJ of the lowest-energy works in the 1.2-V domain. Similarly, both designs have the smallest areas for their respective voltage domains. Fig. 10 shows a graphical comparison of leakage power and energy per transition with existing works, highlighting the significant reduction in leakage power.

IV. CONCLUSION

This letter presented an ultralow-leakage level converter architecture for battery-less IoT systems. The architecture was implemented for core (1.2 V) and I/O (2.5 V) voltage domains, and measurement results show an achieved leakage power of 2.56 pW and 44 fW, respectively. The designs achieve high energy efficiency, showing an energy per transition of 8.18 fJ and 54.23 fJ, respectively.

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