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A Design and Theoretical Analysis of a 145 mV to 1.2 V Single-Ended Level Converter Circuit for Ultra-Low Power Low Voltage ICs [†]

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Abstract: This paper presents an ultra-low swing level converter with integrated charge pumps that shows measured conversion in a 130-nm CMOS test chip from an input at a 145-mV swing to a 1.2-V output. Lowering the input allowable for a single-ended level converter supports energy harvesting systems that need to use very low voltages.

Keywords: level converter; charge pump; subthreshold; energy harvesting

1. Introduction

Energy autonomy is a critical feature required to enable the large-scale deployment of ultra-low power (ULP) systems in the Internet of things (IoT), with energy harvesting being accepted as a more viable means to provide power. Modern energy harvesting circuits can now harvest energy from input voltages as low as 10 mV [1]. However, many challenges face energy harvesting circuits, which require operation at very low power and voltage levels [2]. Figure 1 shows the block diagram of a generic energy harvesting system. The lifetime of the system depends on the energy stored on the energy harvesting capacitor C to provide power for the system. At runtime, as the energy stored on C is being consumed, the voltage on the capacitor, V_{CAP} , is decreasing. The voltage at which the system stops operating (system threshold voltage) must be brought down to increase system lifetime. The minimum energy point has been proposed as the most optimal point to operate a system [3]. However, to maximize the utilization of stored energy on a capacitor, the system needs to operate from the lowest possible voltage. From the energy utilization perspective, the system threshold voltage should be brought down as low as possible to make full use of the stored energy. To more fully take advantage of the energy stored on the energy harvesting capacitor, SoCs (system on chip) under ultra-low voltage have been proposed in [4], which operate below 160 mV. Typical ULP (ultra low power) SoCs frequently use timers to keep the circuit functional, even when the voltage is very low [5]. However, the outputs of these ULP subthreshold circuits also operate at a very low voltage level, which causes communication problems with the core voltage levels off-chip or with other peripheral circuits. Level converters are necessary in such a system to interface between the low voltage domain and the nominal voltage domain. In this paper, we present a low swing level

converter that can convert from the 100-mV (simulation) and 145-mV (measurement) level input signals to 1.2 V using a single-ended charge pump-based topology.

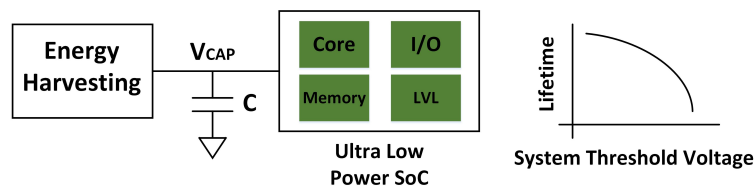


Figure 1. Generic energy harvesting-based SoC. This figure was originally used in [6].

A traditional level converter can convert from nearly 400 mV to 1.2 V via a cross-coupled stage. However, in a low power system, the system life time can be extended by lowering the operation voltage, the same with the energy consumption. Lower input signals can kill the positive feedback and prevent conversion with the traditional design. Several low voltage level converter circuits have been proposed in the literature. A low swing level converter can convert from a range of 210 mV to 950 mV to 1.2 V with a bootstrapping technique [7]. A dynamic logic level converter can convert 300 mV to 2.5 V, which is employed with a clock synchronizer [8]. However, being a dynamic circuit, it can only operate at higher frequencies and uses higher power and area. A single-ended interconnect circuit achieves level conversion from 300 mV [9], but it is dynamic and higher power. In [10], a current mirror structure is proposed, which allows the conversion from 200 mV across technologies. A two-stage ULP level converter can convert from 188 mV to 1.2 V achieving ULP operation [11]. In this work, we present two design constraints for the main stream cross-coupled level converter. Furthermore, we propose a level converter that can potentially convert 100 mV to 1.2 V using a charge pump. The charge pump stage increases the swing before level conversion, which helps in initiating the positive feedback. Our measurement results show conversion from 145 mV to 1.2 V.

This paper is organized as follows: In Section 2, we discuss two main categories of conversion techniques for level converter design: amplification-based conversion and boosted swing-based conversion. In this section, we analyze the level conversion techniques in detail and give two design constraints of an amplification-based subthreshold level converter, which is the mainstream. In Section 3, we propose our own work integrating the two techniques introduced in Section 2. We first introduce our design architecture and two different designs based on this architecture. We then show the simulation results of the proposed work. In Section 4, we show the chip fabricated using 130-nm CMOS technology and the measurement results of the proposed designs. Lastly, we compare our work with the state-of-the-art in Section 5.

2. Level Conversion Techniques

In this chapter, we discuss the state-of-the-art level conversion techniques in the subthreshold domain. We introduce the level conversion techniques in two categories based on their different fundamental structure and working mechanisms: amplification-based and boosted swing-based level conversions. Specifically, we discuss in detail the theoretical analysis of the amplification-based level conversion.

2.1. Amplification-Based Level Conversion

The first main type of level converter design is based on an amplification mechanism that aims to enhance the pull down network. We will analyze this type of design in this subsection.

2.1.1. Designs of Amplification-Based Level Converters

Figure 2a,b shows two of the most traditional amplification-based level converter topologies [12]. Following the naming convention in [10], the level converter shown in Figure 2a is the conventional cross-coupled level converter (CCLC), and the level converter shown in Figure 2b is the current mirror-based level converter (CMLC). CCLC is a full-swing design, which can pull up the input low voltage VDDL up to the high voltage rail VDDH by taking advantage of positive feedback. However, also due to the positive feedback, the conversion capability decreases, because it has to meet the ratio constraint between the pull up network and pull down network. CMLC uses a basic current mirror. CMLC has a stronger conversion capability due to the level shift using the differential amplifier action. However, CMLC cannot eliminate the direct current when input is high, which leads to a higher static power consumption.

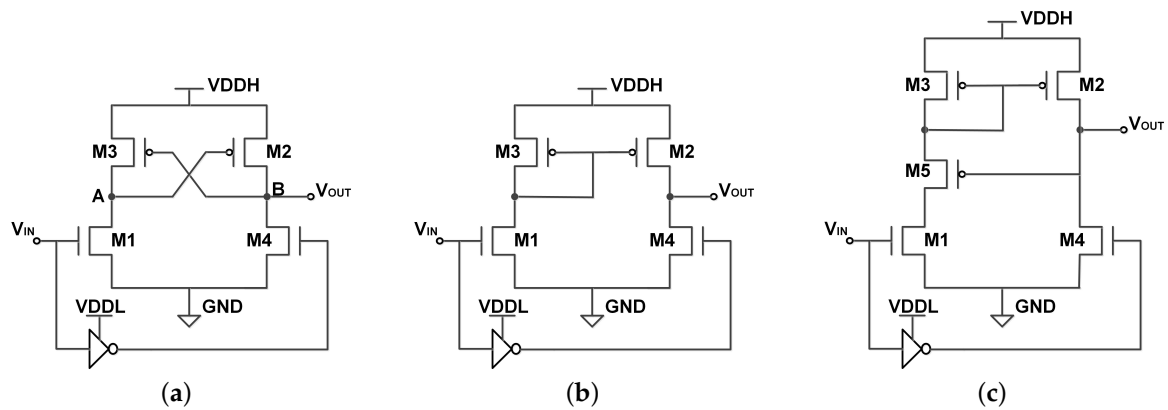


Figure 2. Amplification-based level converter structures. (a) Conventional cross-coupled level converter (CCLC); (b) current mirror-based level converter (CMLC); (c) subthreshold level converter with a Wilson current mirror (WCMLC).

Figure 2c is a design with an Wilson current mirror (WCMLC) [13]. As discussed in the paper and [10], WCMLC is robust, but is not repeatable for the Monte Carlo sizing optimization across different technologies. In [14], they used a three-stage design based on the topology in Figure 2a, which is able to convert from 200 mV to 1.2 V. This cascaded design requires three supply voltages and size adjustment for each of the three intermediate conversion stages, which increases the design and power management complexity. Based on this work in [14], the authors in [11] proposed a two-stage cross-coupled level converter as in Figure 3. They added an NMOS header in the first stage to weaken the pull up network (PUN) to enhance the conversion of the shifter. This simplified the design of [14] and achieves the conversion from 188 mV in the subthreshold. In this paper, we will note this design as a two-stage CCLC (TSCCLC), as in [10].

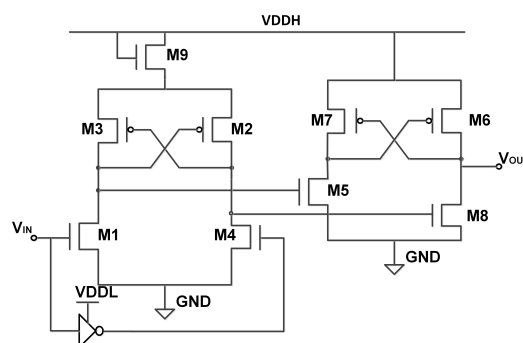


Figure 3. Two-stage CCLC (TSCCLC).

2.1.2. Theoretical Analysis of Amplification-Based Level Converters

We will discuss two design constraints here using the example of CCLC: the sufficient conversion condition and balanced switching condition. We will prove that the latter gives a stronger design constraint. We will perform all of the analysis based on the notation in Figure 4. Finally, we discuss the drawbacks of CMLC.

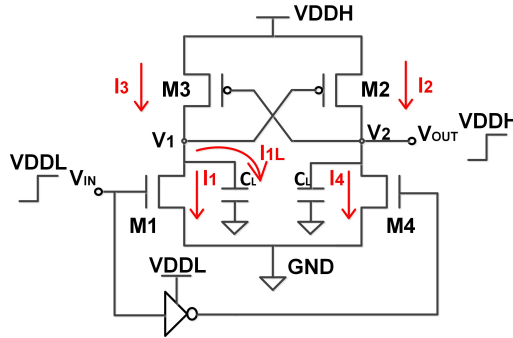


Figure 4. Design constraint analysis of CCLC.

Sufficient Conversion Condition for CCLC

The essential point of a subthreshold amplification-based level converter design is to adjust the ratio of the pull up network and pull down network, so that the pull down network is strong enough to achieve the conversion when the input is ‘high’ in the subthreshold. As in CCLC, we perform a specific analysis of the design constraints for a sufficient conversion in the subthreshold, as marked in Figure 4.

In the analysis, we use V_{tn} and V_{tp} to represent the threshold voltage for NMOS and PMOS, respectively. k_n and k_p are the gain factor of NMOS and PMOS, while k_{sn} and k_{sp} are for the subthreshold. When input switches from ‘low’ to ‘high’, at this moment, V_1 is V_{DDH} , so M_1 works in saturation region:

$$I_1 = k_n(V_{gs} - V_{tn})^2 = k_n(V_{DDL} - V_{tn})^2 \tag{1}$$

M_3 works in linear region:

$$I_3 = k_p((V_{DDH} - V_2 - V_{tp})(V_{DDH} - V_1) - (V_{DDH} - V_1)^2) \tag{2}$$

M_2 and M_4 are off, so we get I_2 and I_4 :

$$I_2 = I_{DP0} \frac{W}{L} e^{\frac{qV_{gs}}{nkT}} = k_{sp} e^{\frac{q(V_{DDH}-V_1)}{nkT}} \tag{3}$$

$$I_4 = I_{DN0} \frac{W}{L} e^{\frac{k_B q V_{gs}}{nkT}} = k_{sn} \tag{4}$$

For a successful conversion, when input switches from ‘low’ to ‘high’, the pull up network should be able to overcome the pull down network at node V_2 to break the internal equilibrium and trigger the positive feedback:

$$I_2 \geq I_4 \tag{5}$$

Represent I_2 and I_4 by Equations (3) and (4):

$$k_{sp} e^{\frac{q(V_{DDH}-V_1)}{nkT}} \geq k_{sn} \tag{6}$$

Thus, for the minimum scenario:

$$q \frac{V_{DDH} - V_1}{nkT} = \ln \frac{k_{sn}}{k_{sp}} \quad (7)$$

Then, we get:

$$V_{DDH} - V_1 = \frac{nkT}{q} \ln \frac{k_{sn}}{k_{sp}} \quad (8)$$

Assuming that in subthreshold region, the leakage very slowly charges C_L (on the right part of CCLC), V_2 will not rise fast and stays close to zero, and V_1 will stay close to V_{DDH} .

Thus, in Equation (2), let $V_2 = 0$:

$$I_3 = k_p(V_{DDH} - V_{tp})(V_{DDH} - V_1) \quad (9)$$

The sufficient condition for a successful conversion is to break the equilibrium between the pull up network and pull down network and be able to pull down V_1 :

$$I_1 \geq I_3 \quad (10)$$

Take Equations (1) and (9). Thus:

$$k_n(V_{DDL} - V_{tn})^2 \geq k_p(V_{DDH} - V_{tp})(V_{DDH} - V_1) \quad (11)$$

Then, take Equation (8) into Equation (11), we get the final sufficient condition for a conversion:

$$\frac{k_n}{k_p} \geq \frac{V_{DDH} - V_{tp}}{(V_{DDL} - V_{tn})^2} \frac{nkT}{q} \ln \frac{k_{sn}}{k_{sp}} \quad (12)$$

Equation (12) shows that NMOS and PMOS cannot be arbitrarily sized to get the desired ratio for k_n and k_p , because the sizing of NMOS and PMOS also determines the ratio of k_{sn} and k_{sp} at the same time. Therefore, the cross-coupled level converter (CCLC) cannot be used reliably for subthreshold operations, as the subthreshold leakage plays a part in triggering the positive feedback.

Balanced Switching Condition for CCLC

In a level converter design, to get a balance of rising and falling time (i.e., $t_{LH} = t_{HL}$), we must consider the following constraint:

$$I_2 = C_L \frac{dV_2}{dt} \quad (13)$$

Additionally, at the same time, I_2 is:

$$I_2 = k_p(V_{DDH} - V_1 - V_{tp})^2 \quad (14)$$

Thus, we get:

$$C_L \frac{dV_2}{dt} = k_p(V_{DDH} - V_1 - V_{tp})^2 \quad (15)$$

Similarly for I_{1L} , we have:

$$I_{1L} = k_n(V_{DDL} - V_{tn})^2 - k_p(V_{DDH} - V_1 - V_{tp})^2 \quad (16)$$

Additionally:

$$I_{1L} = C_L \frac{dV_1}{dt} \quad (17)$$

Therefore, we get:

$$C_L \frac{dV_1}{dt} = k_n(V_{DDL} - V_{tn})^2 - k_p(V_{DDH} - V_1 - V_{tp})^2 \quad (18)$$

Let $dt = dt$ using Equations (15) and (18):

$$[k_n(V_{DDL} - V_{tn})^2 - k_p(V_{DDH} - V_1 - V_{tp})^2]dV_2 = k_p(V_{DDH} - V_1 - V_{tp})^2dV_1 \quad (19)$$

In a balance design where $t_{LH} = t_{HL}$, when V_1 changes from zero to V_{DDH} , V_2 changes from V_{DDH} to zero. Take this into Equation (19):

$$\int_{V_{DDH}}^0 [k_n(V_{DDL} - V_{tn})^2 - k_p(V_{DDH} - V_2 - V_{tp})^2]dV_2 = \int_0^{V_{DDH}} k_p(V_{DDH} - V_1 - V_{tp})^2dV_1 \quad (20)$$

Solve Equation (20); we get the design constraint for a subthreshold balanced level converter:

$$\frac{k_n}{k_p} = \frac{2V_{DDH}(V_{DDH} - V_{tp})}{(V_{DDL} - V_{tn})^2} \quad (21)$$

The balance design constraint Equation (21) is a much stronger bound than the sufficient conversion constraint Equation (12). In other words, it is more difficult to make a subthreshold level converter with an equal rising and falling time. The bound of Equation (12) gives a design constraint of a successful conversion, but cannot guarantee the balance of switching performance.

Drawback of CMLC

In the current mirror design (CMLC), the biggest problem is the direct current and the slow conversion in the subthreshold. We will do a simple analysis using Figure 5.

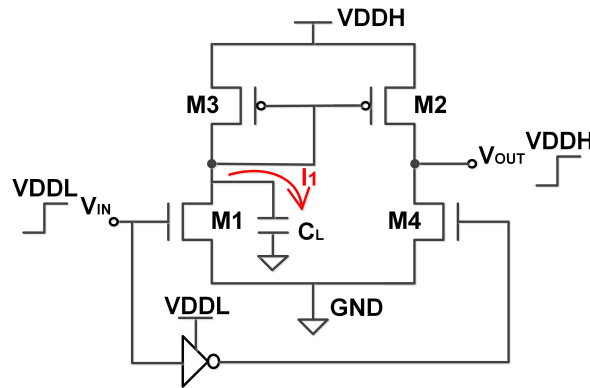


Figure 5. Drawback analysis of CMLC.

When input is ‘high’ (V_{DDL}), M1 works in the saturation region:

$$I_1 = k_n(V_{gs} - V_{tn})^2 = k_n(V_{DDL} - V_{tn})^2 \quad (22)$$

However, in the subthreshold, the case in Equation (22) will be:

$$I_1 = k_{sn}e^{\frac{qV_{DDL}}{nkT}} \quad (23)$$

With the existence of the current mirror, we also have:

$$I_1 = C \frac{V_{DDH}}{T_{rise}} \tag{24}$$

Combine Equations (23) and (24):

$$T_{rise} = \frac{C_L V_{DDH}}{k_s n} \frac{1}{e^{\frac{qV_{DDL}}{nkT}}} \tag{25}$$

From Equation (25), a current mirror level converter has a very slow conversion in the subthreshold (low VDDL). This is the biggest bottleneck of this kind of design.

2.2. Boosted Swing-Based Level Conversion

The other type of level converter is the boosted swing-based level converter. Different with amplification-based level converters, boosted swing-based conversions happen by pulling the ‘high’ input signal higher first through boosting techniques. This is usually achieved by taking advantage of the characteristics of a capacitor.

Designs of Boosted Swing-Based Level Converters

Figure 6 is a design based on the bootstrapping effect as reported in [15], lrc-converter as called in [7]. The drivers are enhanced by the bootstrapping techniques through the capacitor C_b . In a boosted swing-based level converter like Figure 6, when the input is low, the output is pulled up to VDDH by M4. The left plate of C_b is ‘0’, and the right plate is pulled up to VDDL by M0. When the input is high (VDDL), M2 passes a ‘0’ to M0’s gate and turns it on, while M1 is turned on at the same time. In this phase, the left plate of C_b is pulled up from zero to VDDL (in the previous phase), and the right plate is pulled up from VDDL to $2 \times VDDL$. The boosted $2 \times VDDL$ is passed to the gate of M4. In order to pull down the output to zero, it has to meet this condition to turn off M4 completely:

$$2 \times VDDL > VDDH \tag{26}$$

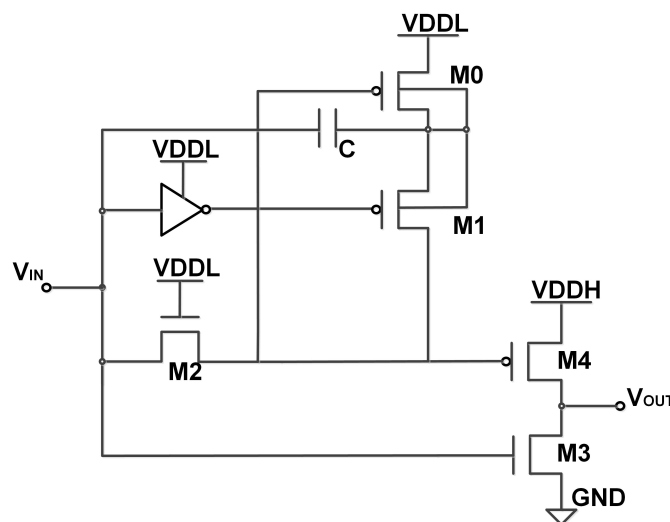


Figure 6. Boosted swing-based level converter structure [15].

If this condition is not met, it will result in static current through M4. This design requires two power supplies, VDDH and VDDL, which increases the design complexity. In conclusion, the major problem of this level converter design is that it is dynamic and only works at high frequency.

For example in Figure 6, the gate of M_4 will slowly decrease to V_{DDL} at a lower frequency of signals, which causes high static current.

The proposed work in [7] is based on the same bootstrapping effects and reduced the circuit complexity with an improvement of power and delay. A similar design is proposed in [9]. The boosted swing-based design is usually preferred in the interconnect design to work with reducing the power consumption or re-boost the signals to communicate with the core chip.

3. Proposed Low Voltage Level Converter

In this section, we introduce our proposed low power subthreshold single-ended level converter. Our design is based on both the amplification-based and boosted swing-based conversion techniques. The combination of the two design types of level converters achieves a stronger conversion capability that allows a deeper application in subthreshold ICs. This proposed design uses a two-staged architecture: boosting stage and conversion stage. The boosting stage is implemented with a subthreshold charge pump design, while the conversion stage uses the amplification-based techniques.

First, we propose the boosting part: a subthreshold charge pump. Next, we introduce our uniform design architecture, which takes advantage of this subthreshold charge pump. According to the architecture, we introduce two level converter designs and show the simulation results accordingly.

3.1. Subthreshold Charge Pump

Figure 7 shows the schematic of a $2\times$ charge pump used in the proposed work and its sizing. When V_{IN} is low, M_1 turns on, which turns on M_3 . X is pulled up to V_{DDL} , while B is pulled down to GND by the inverter connected to it. Next, V_{IN} goes high and turns on M_2 and M_5 , which leads to the up-conversion of B from zero to V_{DDL} . Since X was charged to V_{DDL} previously, the up-conversion of B causes X to go from V_{DDL} to $2\times V_{DDL}$ at the output of the charge pump. In this design, M_4 works as a capacitor to implement the boosting.

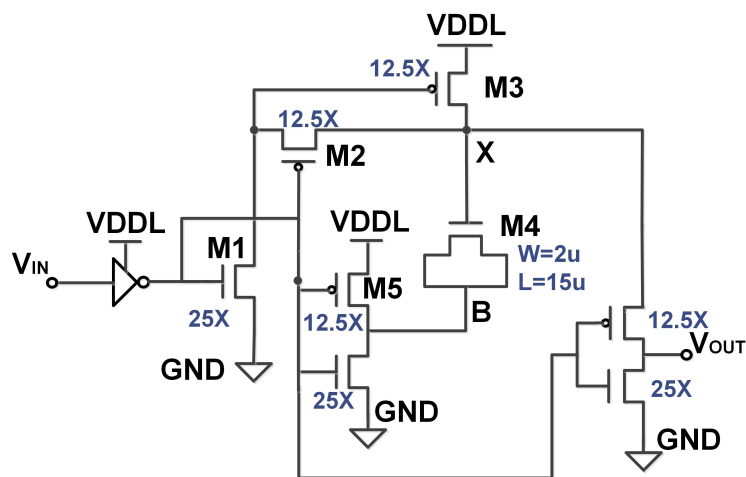


Figure 7. Schematic of the $2\times$ charge pump used in the proposed work.

In deep subthreshold operation with a V_{DD} between 100 mV and 300 mV, node X falls ideally at 200 mV and 600 mV, respectively. However, in the subthreshold, the low slew rate prevents a full doubling of voltage when V_{DD} is very low (<200 mV) because of the higher discharge caused by leakage. Thus, we enhanced the pull down network. In this charge pump design, we do not require an additional body bias control circuit.

3.2. Implementation of the Proposed Level Converter

We propose two designs that use charge pump outputs to drive a traditional level converter CCLC, as in Figure 2a, and the improved two-stage amplification-based level converter from [11], as in Figure 3, respectively. We call the former proposed level converter the charge pump boosted level converter (CPBLC) in the rest of the paper, and we call the latter proposed level converter the charge pump boosted ultra-low swing level converter (CPBULS). Following the same naming convention, we use ULS to represent TSCCLC in the following comparison to simplify the relationship between different structures.

Uniform Architecture

Figure 8 shows the architecture of the proposed topology, which combines two charge pumps and a level converter design. The first stage provides the differential inputs doubled by the $2\times$ charge pumps. The second stage is a cross-coupled differential inverter (e.g., the level converter designs in Figure 2) that restores the final output to full swing (zero to V_{DDH}). The output of the charge pump stage overpowers the equilibrium of the second stage and drives the PMOS to pull up the internal node (e.g., A or B in Figure 2a and triggers the positive feedback within the conversion stage).

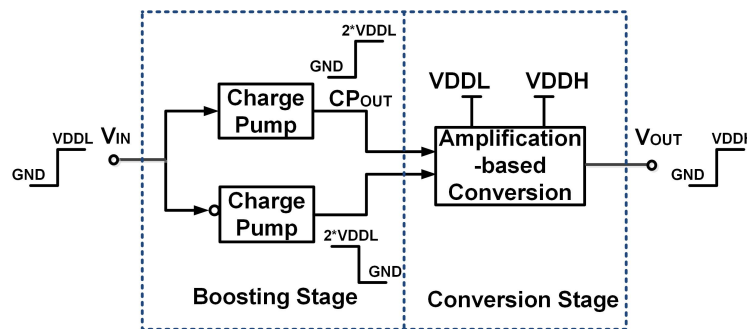


Figure 8. Architecture of the proposed level converter.

3.3. CPBLC and CPBULS

Deriving from the same proposed architecture, we use the boosting power of the subthreshold charge pump to trigger the conversion. We will omit the schematic of CPBLC and CPBULS, since their second stages have the same structure of CCLC as in Figure 2a and TSCCLC as in Figure 3.

Simulations

In Figure 9, it shows the functional waveform of CPBULS from the simulation of a V_{DDL} of 120 mV. In fact, CPBLC works in a similar way. The signals labeled in Figure 9 correspond to the signals in Figure 8. As V_{IN} goes high or goes low, one of the charge pump outputs, e.g., CP_{OUT} , increases and thus initiates the positive feedback in the conversion stage, resulting in the amplification-based voltage conversion. From observation, when V_{IN} just reaches its highest value (120 mV), the conversion cannot be successfully triggered. Instead, the boosting stage takes in V_{IN} and pulls it up to 200 mV from 120 mV, as shown as CP_{OUT} . When CP_{OUT} is boosted to around 200 mV, the voltage conversion of the second stage successfully happens. This is as explained in Section 2: the boosted CP_{OUT} successfully satisfies the sufficient conversion constraint in Equation (12). In other words, the boosting stage lowers the constraint of a sufficient conversion for the same amplification-based level converter design. Furthermore, in Figure 9, we can see that CP_{OUT} will slowly decrease to V_{DDL} , as well, like the design in Figure 6. However, the difference is, in our design, this will not cause static current.

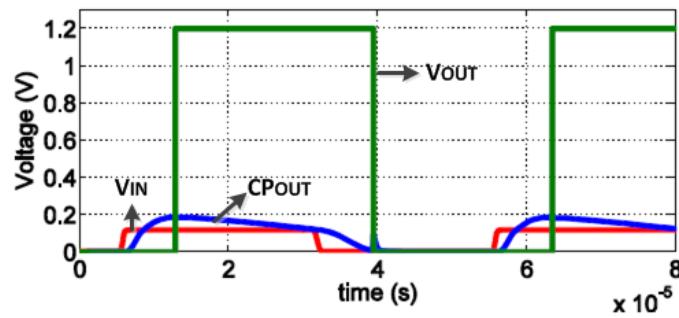


Figure 9. Functional waveform of charge pump boosted ultra-low swing level converter (CPBULS). This figure was originally used in [6].

Figure 10 shows the minimum input swing results of 100 Monte Carlo simulations for CPBULS, CPBLC and ULS level converters. The charge pump technique decreases the minimum operating voltage of [11] (TSCCLC), further lowered down to an average of 128 mV, while the best case (among the 100 iterations) is 99.6 mV in CPBULS and an average of 171 mV in CPBLC.

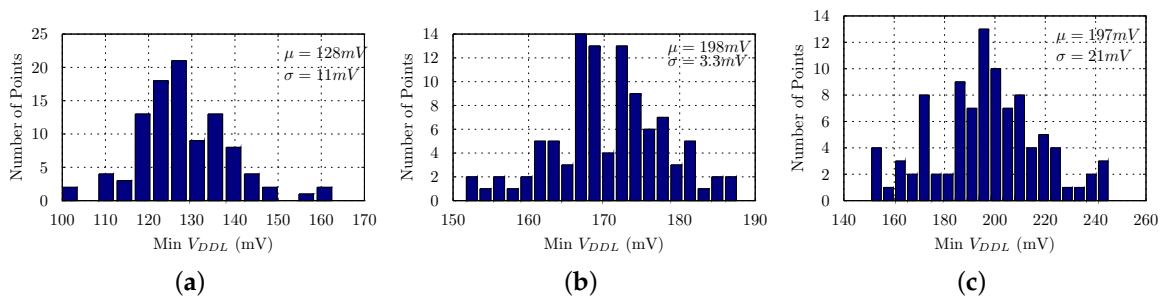


Figure 10. Monte Carlo simulation results of the minimum input voltage of (a) CPBULS, (b) charge pump boosted level converter (CPBLC) and (c) ULS level converters (100 iterations).

Figure 11 shows the simulation results of the minimum input voltage of CPBULS (red) and CPBLC (blue) level converters under different temperatures. At $-20\text{ }^{\circ}\text{C}$, CPBULS and CPBLC can work at 145.4 mV and 192.8 mV respectively, while at $100\text{ }^{\circ}\text{C}$, they can work at 116.4 mV and 144.3 mV, respectively. Simulation shows that our charge pump-based level converter has lower temperature dependence for the minimum operating voltage.

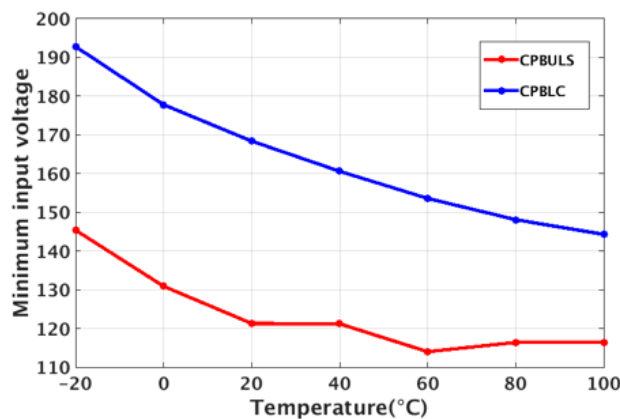


Figure 11. Simulation results of the minimum input voltage vs. temperature of CPBULS and CPBLC level converters. This figure was originally used in [6].

The proposed design was fabricated in a 130-nm CMOS process. Figure 12 shows the die photo of the test chip. The subthreshold charge pump takes $280 \mu\text{m}^2$, while CPBLC and CPBULS take around $466 \mu\text{m}^2$ with an unoptimized layout design and necessary peripheral circuits.

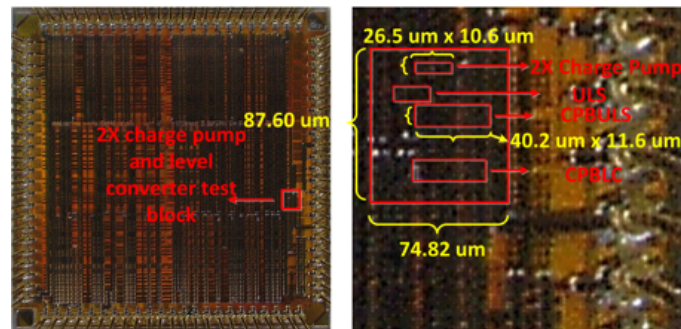


Figure 12. Die photo of the fabricated chip under 130-nm technology. This figure was originally used in [6].

4. Measurements

Figure 13 shows the measurements of the $2\times$ charge pump from 15 chips, which starts working from a 170-mV input in the worst case. We show the simulation result together with the measurement results: the blue lines are the measurement results, while the red line is from simulation. After V_{IN} is higher than 200 mV, the boosting factor is stable at $2\times$.

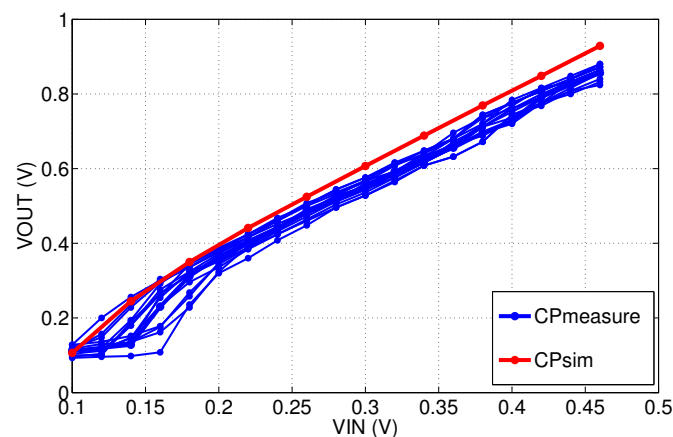


Figure 13. Simulation and measurement results of the input vs. output voltage of the charge pump stage of the level converter. This figure was originally used in [6].

Figure 14 shows the measurement results of the minimum operational input swing for CPBULS, CPBLC and ULS level converters across the 15 chips. The CPBULS can achieve a mean minimum input voltage of 157 mV, while the CPBLC achieves the same at 198 mV. The CPBULS can reach a lowest input voltage of 145 mV. The limitation of this design is slower transition times that lead to higher energy per conversion due to the extra leakage.

Figure 15 shows the energy-delay measurement of CPBLC and CPBULS across 15 fabricated chips. The measurements were taken at three points: 200 mV, 300 mV and 500 mV. CPBLC and CPBULS can operate with a frequency of 35.6 kHz (28 μs) and 50.1 kHz (19.96 μs), respectively, at 200 mV for the best case, with a mean value of 12.8 kHz and 22.0 kHz, respectively. The best operation frequency is 66.9 kHz and 136.6 kHz at 300 mV, 109.7 kHz and 139.4 kHz at 500 mV, for CPBLC and CPBULS, respectively. As the operation voltage increases, the delay decreases,

which is expected in an energy harvesting system where the worst case is when the operation voltage is the lowest. In the subthreshold energy harvesting system, there is much voltage variation. The proposed work is designed for an unregulated power supply, which can still successfully work in the worst cases (also known as when the operation voltage goes very low). From the measurement results of the 15 chips we fabricated, the best EDP value is 0.0015 pJ·ms for CPBLC and 0.0006 pJ·ms for CPBULS.

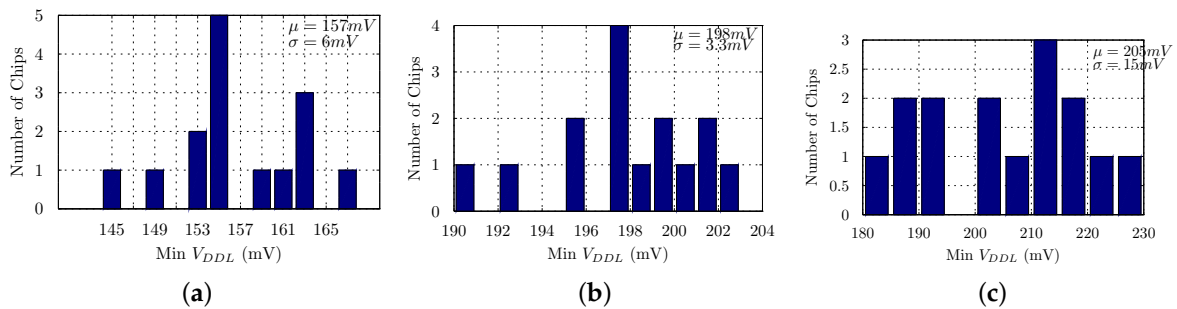


Figure 14. Measurement results of the minimum input voltage of (a) CPBULS, (b) CPBLC and (c) ULS level converters.

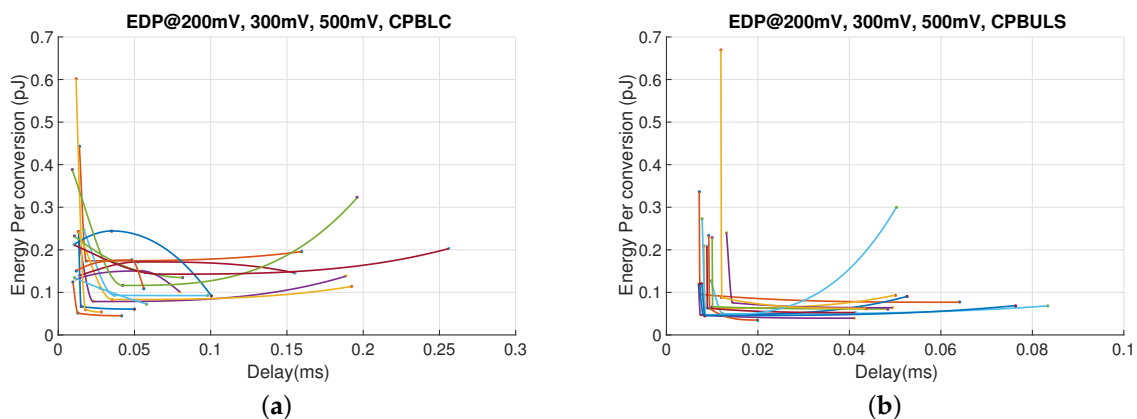


Figure 15. Energy-delay for (a) CPBLC and (b) CPBULS from measurement across 15 chips.

Another source of variation, the process, can also affect the behavior of this design. As in Figure 7, in the subthreshold, the low slew rate results in that node X cannot be charged to $2 \times V_{DDL}$ due to the discharge caused by leakage. Thus, in the slow-fast corner, the discharge will further affect the boosting of X; and vice versa, in the fast-slow corner, the discharge is weakened; thus, the boosting is enhanced. For the same reason, as in Figure 7, we enhanced the pull down network.

5. Conclusions

This proposed level converter design is based on a subthreshold charge pump design, as shown in Figure 7. Due to the charge and discharge time of M_4 , the capacitor, its performance is not as good as conventional level converters at their operating voltages (300 to 400 mV). However, this design is a better choice for an ultra-low power energy harvesting system where performance is not the first priority, but the ability of using stored energy is instead, as discussed in Section 1. Thus, we try to make more use of the energy collected in the capacitor in Figure 1. The challenge is, the lower the level converter can operate at, the more energy the system can use to obtain a longer lifetime.

Table 1 compares prior work, both simulations and chip measurements. This proposed charge pump-based level converter CPBULS up-converts reliably from 145 mV to 1.2 V, which is a wider

conversion range. The best energy per conversion is reported as 10 fJ in [10] from simulation results with a 90-nm technology. This work has a relatively lower maximum operating frequency with the lowest input swing, but achieves 1.2 pJ energy per conversion, which is 30% less than that in [8] from chip measurement and a 2× conversion ability. This proposed work can further improve the energy utilization of an ultra-low power system, such as an energy harvesting system.

Table 1. Comparison between the proposed work and prior work.

	[11]	[10]	[16]	[8]	This Work
Minimum VDDL	188 mV	200 mV	400 mV	300 mV	145 mV
Energy/bit	-	10 fJ	327 fJ	1.7 pJ	1.2 pJ
Chip/simulation	Chip	Sim	Sim	Chip	Chip
Maximum frequency	17.3 MHz	10 MHz	1 MHz	8 MHz	8 kHz
Area (um²)	-	-	120.9	112,000	466
Technology	130 nm	90 nm	180 nm	130 nm	130 nm

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

ULP	Ultra low power
IoT	Internet of things
SoC	System on chip
CCLC	Cross-coupled level converter
CMLC	Current mirror-based level converter
WCMLC	Wilson current mirror level converter
PUN	Pull up network
PDN	Pull down network
TSCCLC/ULS	Two-stage cross-coupled level converter
CPBLC	Charge pump boosted level converter
CPBULS	Charge pump boosted ultra-low swing level converter

References

1. Shrivastava, A.; Wentzloff, D.; Calhoun, B.H. A 10 mV-input boost converter with inductor peak current control and zero detection for thermoelectric energy harvesting. In Proceedings of the 2014 IEEE Custom Integrated Circuits Conference (CICC), San Jose, CA, USA, 15–17 September 2014; pp. 1–4.
2. Klinefelter, A.; Roberts, N.E.; Shakhsheer, Y.; Gonzalez, P.; Shrivastava, A.; Roy, A.; Craig, K.; Faisal, M.; Boley, J.; Oh, S.; et al. 21.3 A 6.45 μ W self-powered IoT SoC with integrated energy-harvesting power management and ULP asymmetric radios. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 22–26 February 2015; pp. 1–3.
3. Calhoun, B.H.; Chandrakasan, A. Characterizing and modeling minimum energy operation for subthreshold circuits. In Proceedings of the 2004 International Symposium on Low Power Electronics and Design (ISLPED'04), Newport Beach, CA, USA, 9–11 August 2004; pp. 90–95.
4. Kulkarni, J.P.; Kim, K.; Roy, K. A 160 mV, fully differential, robust schmitt trigger based sub-threshold SRAM. In Proceedings of the 2007 International Symposium on Low Power Electronics and Design, Portland, OR, USA, 27–29 August 2007; pp. 171–176.

5. Shrivastava, A.; Kamakshi, D.A.; Calhoun, B.H. A 1.5 nW, 32.768 kHz XTAL Oscillator Operational from a 0.3 V Supply. *IEEE J. Solid-State Circuits* **2016**, *51*, 686–696.
6. Huang, Y.; Shrivastava, A.; Calhoun, B.H. A 145 mV to 1.2 V single ended level converter circuit for ultra-low power low voltage ICs. In Proceedings of the 2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Burlingame, CA, USA, 10–13 October 2015; pp. 1–3.
7. García, J.C.; Nelson, J.A.M.; Nooshabadi, S. High performance bootstrapped CMOS low to high-swing level-converter for on-chip interconnects. In Proceedings of the 18th European Conference on Circuit Theory and Design (ECCTD 2007), Sevilla, Spain, 26–30 August 2007; pp. 795–798.
8. Chang, I.J.; Kim, J.j.; Kim, K.; Roy, K. Robust level converter for sub-threshold/super-threshold operation: 100 mV to 2.5 v. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2011**, *19*, 1429–1437.
9. Shrivastava, A.; Lach, J.; Calhoun, B. A charge pump based receiver circuit for voltage scaled interconnect. In Proceedings of the 2012 ACM/IEEE International Symposium on Low Power Electronics and Design, Redondo Beach, CA, USA, 30 July–1 August 2012; pp. 327–332.
10. Luo, S.C.; Huang, C.R.; Chiou, L.Y. Minimum convertible voltage analysis for ratioless and robust subthreshold level conversion. In Proceedings of the 2012 IEEE International Symposium on IEEE Circuits and Systems (ISCAS), Seoul, South Korea, 20–23 May 2012; pp. 2553–2556.
11. Wooters, S.N.; Calhoun, B.H.; Blalock, T.N. An energy-efficient subthreshold level converter in 130-nm CMOS. *IEEE Trans. Circuits Syst. II: Express Briefs* **2010**, *57*, 290–294.
12. Koo, K.H.; Seo, J.H.; Ko, M.L.; Kim, J.W. A new level-up shifter for high speed and wide range interface in ultra deep sub-micron. In Proceedings of the IEEE International Symposium on IEEE Circuits and Systems (ISCAS 2005), 23–26 May 2005; pp. 1063–1065.
13. Lütke-meier, S.; Rückert, U. A subthreshold to above-threshold level shifter comprising a wilson current mirror. *IEEE Trans. Circuits Syst. II: Express Briefs* **2010**, *57*, 721–724.
14. Zhai, B.; Pant, S.; Nazhandali, L.; Hanson, S.; Olson, J.; Reeves, A.; Minuth, M.; Helfand, R.; Austin, T.; Sylvester, D.; et al. Energy-efficient subthreshold processor design. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2009**, *17*, 1127–1137.
15. Moisiadis, Y.; Bouras, I.; Arapoyanni, A. High performance level restoration circuits for low-power reduced-swing interconnect schemes. In Proceedings of the 7th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2000), Jounieh, Lebanon, 17–20 December 2000; Volume 1, pp. 619–622.
16. Hosseini, S.R.; Saberi, M.; Lotfi, R. A low-power subthreshold to above-threshold voltage level shifter. *IEEE Trans. Circuits Syst. II: Express Briefs* **2014**, *61*, 753–757.



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