A 65nm 16kb SRAM with 131.5pW Leakage at 0.9V for Wireless IoT Sensor Nodes

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Abstract

This paper presents a 16kb SRAM that achieves an ultra-low leakage of less than 132pW across its entire operational V_{DD} range (0.3-0.9V). It is implemented using a new robust two-port bitcell with 614aW leakage, which, to the best of the authors' knowledge, is the lowest leakage bitcell reported to date. Additionally, new peripheral techniques enable 1000x reduction in bit-line (BL) leakage, up to 69% improvement in access speed at low V_{DD}, and up to 63.6% reduction in peripheral circuitry area over state-of-the-art works. The SRAM achieves an array area efficiency of 67.87%, leakage power of 51.8pW to 131.5pW for V_{DD} at 0.3V and 0.9V, and >6.5 MHz access frequency.

Introduction

There has been an ever-increasing demand for wireless sensor nodes with longer lifetimes for a variety of applications including medical, infrastructure, and environmental. Sensor nodes for these applications typically spend most of their time in standby, only waking up periodically to sense and store data in an on-chip memory until it needs to be processed or transmitted. Due to their significant idle time, the energy consumption of these nodes is dominated by leakage power, which is typically constrained by the memory. To improve system energy and lifetime, memories for sensor nodes have used a multitude of techniques including low-V_{DD} operation and power gating to reduce leakage power to less than 10fW/bit [1]-[3], but this low-leakage is only obtained at ultra-low V_{DD} where other performance metrics such as speed and reliability are insufficient for some applications. Additionally, these designs trade off low power with poor array area efficiencies and are implemented in older low-leakage technologies that prohibit integrated system scaling. In this work, we demonstrate an SRAM in 65nm CMOS with ultra-low power across a wide supply voltage range that maintains high area efficiency and fast read and write times. This performance is achieved through several innovations. We introduce a new bitcell with sub-fW intrinsic leakage that is used in conjunction with an ultra-low power word-line over-drive technique that reduces BL leakage by 1000x. Additionally, a new bank and sub-bank level signal decoding architecture is used to achieve an array area efficiency of 67.87%, which is a 63.6% reduction in peripheral circuitry area over previous state-of-the-art works.

Architecture and Design

The maximum noise margin in conventional SRAMs is limited by the inherent $V_{DD}/2$ limit of the transfer characteristic of an inverter. This problem is exacerbated by the weak effect of device sizing on noise margins in subthreshold region. To maintain sufficient noise margins, we incorporate hysteresis into the bitcell by using dynamic leakage suppression (DLS) logic [4]. This increases the switching threshold of the inverter to greatly increase the noise margin, while simultaneously reducing leakage. Fig. 1 shows the schematic of the proposed bitcell, which is designed using cross-coupled DLS inverters, pMOS access transistors, and a data-independent leakage read-port [5]. The bitcell uses all IO devices to reduce subthreshold leakage even further than existing DLS logic and prevent the onset of gate leakage at high V_{DD}. The ultra-low leakage of the bitcell causes it to be susceptible to data corruption via BL disturbances and leakage currents, so the word-line is boosted to VDDH (V_{DD} + 0.3V) using a level converter to super-cutoff the access transistors. The word-line level converter is DLS logic-based (Fig. 2) to reduce the power by 2700x compared to conventional (differential cascode) level converters to maintain a pW-level power budget. The boosted BL voltage cuts off subthreshold leakage through pMOS access transistors, reducing the BL leakage by up to 1000x compared to conventional nMOS access transistors. The higher supply voltage need not be regulated and clean and can therefore be generated using a Switched Capacitor Voltage Regulator (SCVR) with minimal power overhead, or another readily available on-chip supply may be used. Fig. 3 shows the schematic of the alternating partial-level-precharge single-ended read sensing architecture that allows faster access speeds at low V_{DD}. At each level of hierarchy, bitlines are combined using tri-state buffers with alternating logic at each stage. Unlike the conventional Hierarchical BL architecture, the proposed implementation doesn't need a keeper-cell. Consequently, there is no keeper-cell-read-port-cells/column-tradeoff. Additionally, unlike the Ripple BL architecture [6], the non-accessed bitcells are isolated, and the read access operation doesn't aggressively slow down with increase in number of local bitline stages. Instead of a local block-select implementation and read-write multiplexing for each bitcell row, this work pre-multiplies read-write enable signals with block-select and leaf-select signals (Fig. 4), and then routes them across the entire X-Y peripheral circuitry, thereby reducing the total number of gates. This translates to up to 64% reduction in peripheral circuitry area when comparing to similar read-write decoupled works (Fig. 5).

Measurement Results

The proposed SRAM was fabricated in a bulk 65nm technology. Fig. 6 shows the measured leakage power and performance metrics across supply voltage. While the leakage power of previous works increases exponentially with V_{DD} to several nW at room temp., the leakage of the proposed SRAM remains relatively constant (~100pW) between 0.3V and 0.9V. Measurement results from 10 chips show a best-case chip data retention voltage (DRV) of 115mV, 10-chip avg. DRV of 156.5mV and full functionality across temperature from 0°C to 60°C (Fig. 7). The freq. measurement was limited by the on-chip SPI to a max. 6.5MHz (at room temp.). With over 3x reduction in bitcell leakage and over 48x reduction in total leakage power at high V_{DD}, this SRAM enables significant leakage reduction for longer lifetimes in wireless sensor nodes.

Acknowledgements

This work was funded in part by the NSF NERC ASSIST Center (EEC-1160483).

References

[1] S. Hanson, *JSSC*, pp. 1145 – 1155, 2009. [2] M. Fojtik, *JSSC*, pp. 801 – 813, 2013. [3] D. Kim, *ISCAS*, pp. 69 – 72, 2011 [4] W. Lim, *ISSCC*, pp. 146 – 148, 2015. [5] S. Gupta, *TCAS-I*, pp. 978 – 988, 2019. [6] C. Lu, *TCAS-II*, pp. 863 – 867, 2012.

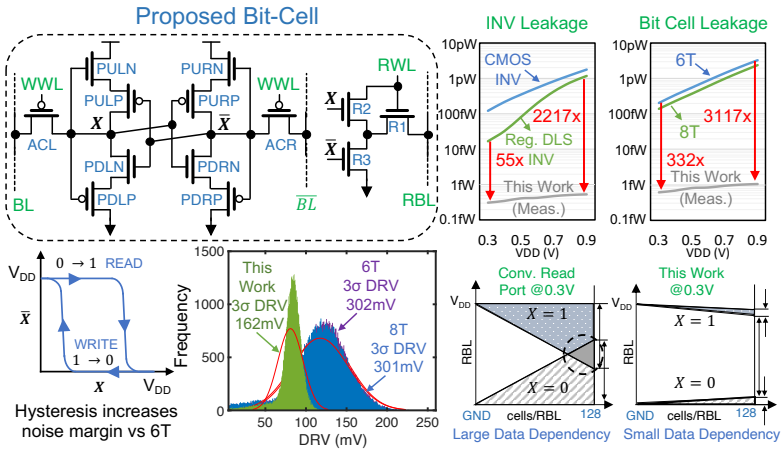

Fig. 1. Schematic of proposed bitcell and its comparison with conventional 6T and 8T based on data retention voltage, leakage power and single ended read operation.

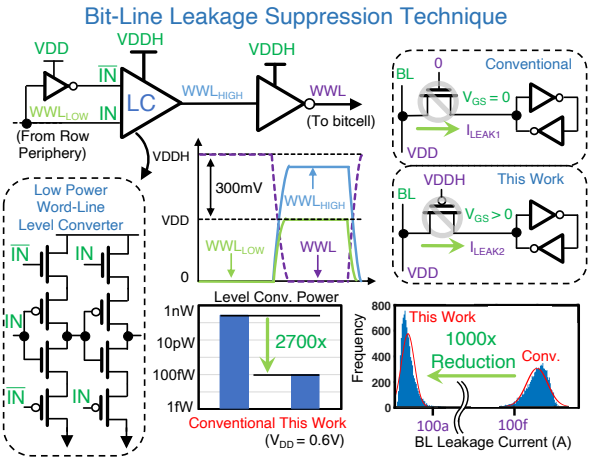

Fig. 2. Schematic of Word-Line level converter and its effect on Bit-Line Leakage

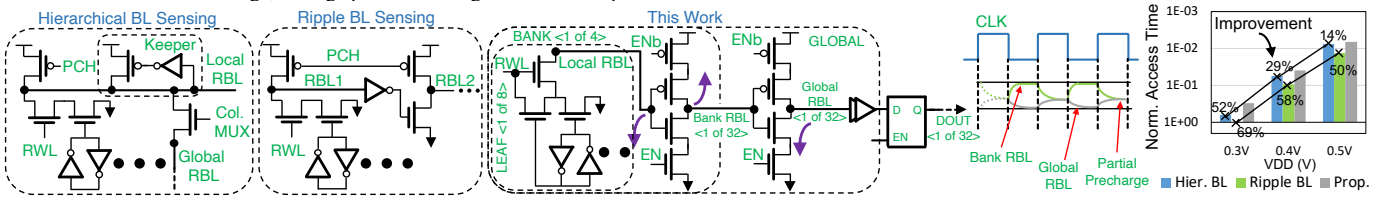

Fig. 3. Schematic of conventional Bit-Line Sensing Techniques (Hierarchical and Ripple-BL) and proposed sensing architecture, waveform of bit-line levels in this work, comparison of access speed performance for various architectures.

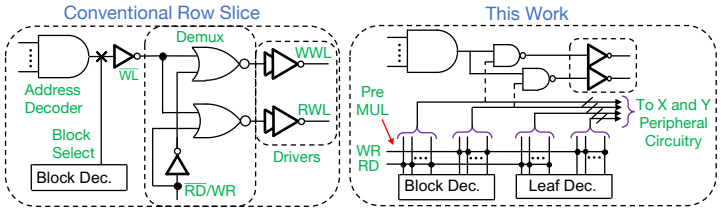

Fig. 4. Schematic of conventional row-slice for a read-write decoupled memory (e.g. 8T) and proposed periphery decoding architecture show reduction in no. of gates.

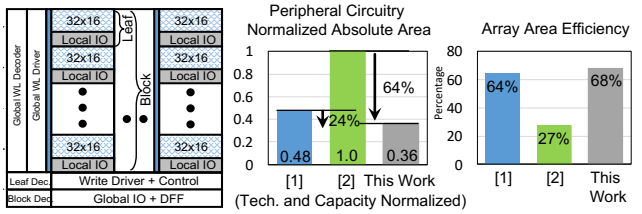

Fig. 5. Block diagram of SRAM, comparison of peripheral circuitry area (technology and capacity normalized), comparison of array area efficiency.

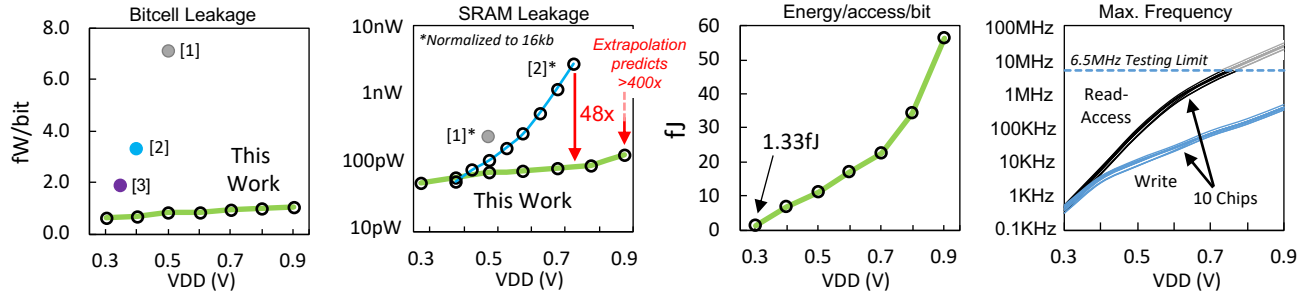

Fig. 6. Measurement results show low leakage power, read-access energy, and speed across V_{DD}.

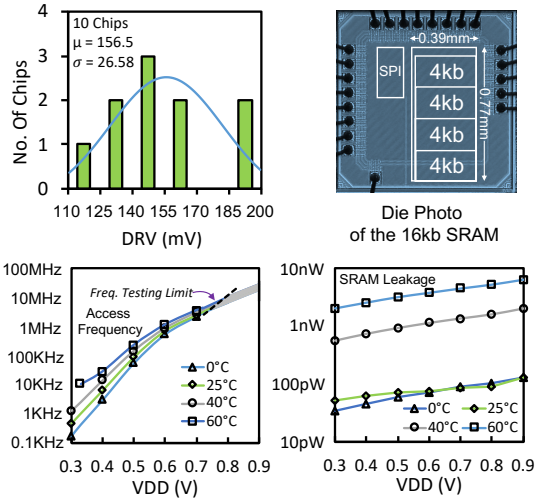

Fig. 7. DRV across 10 chips, frequency and leakage vs temp.

TABLE I. COMPARISON WITH STATE-OF-THE-ART

Metric	Hanson [1]	Fojtik [2]	Kim [3]	This Work
Technology	180nm	180nm	180nm	65nm
Bit-Cell	14T	10T	10T	13T
Bit-Cell Area (μm²)	40	17.48	17.48	12.44
Access Frequency	100KHz @0.5V	3.5KHz @0.35V	1KHz @0.3V	6.9KHz @0.4V
Write Frequency	Async	Multi-Cycle	Multi-Cycle	3.6KHz @0.4V
V_{MIN} (V)	0.5V	0.35V	0.3V	0.3V
Best DRV (mV)	-	-	-	115
Energy/acc./bit @V_{MIN} (fJ)	-	-	-	1.33
Leakage/bit @V_{MIN} (fW)	7.1	3.3	1.85	0.61
SRAM Leakage (pW)	22	80.53	-	51.87
Capacity	1kb	24kb	24kb	16kb
Array Area Efficiency	64%	27%	27%	67.87%