

# A 640 pW 22 pJ/sample Gate Leakage-Based Digital CMOS Temperature Sensor with 0.25°C Resolution

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**Abstract**— This work presents a 640 pW, 22 pJ/conversion gate leakage-powered temperature sensor with 0.25°C resolution and -2.7/1.8°C worst-case inaccuracy from -20°C to 100°C. Gate leakage currents drive both the sensing and sampling elements to provide compact but reliable operation that balances low power and low energy for flexible application use. This low-power, low-energy performance enables continuous sub-nW temperature sensing for the Internet of Things.

**Keywords**— temperature sensor, gate leakage, ultra-low power

## I. INTRODUCTION

Temperature sensing is a critical ability for IoT system-on-chips (SoCs) with applications in health, environmental, and structural monitoring. SoCs in these applications increasingly use energy harvesting to supplement or replace battery use for long-term continuous sensing, so these systems must support low-power operation at the nW level during energy harvesting as well as low-energy operation at the pJ level when powering from stored energy. Until recently, on-chip temperature sensors consume power and energy at several orders of magnitude above these requirements [1]. Sub-nW power consumption in [3, 5] comes at the expense of low conversion rates and heavy duty-cycling, which lead to increased energy. Conversely, [3] reaches single-digit pJ/conversion by scaling up to a high sampling frequency, which increases power consumption to hundreds of nW.

This work presents an integrated temperature sensor that achieves both 640 pW power consumption and 22 pJ/conversion with 0.25°C rms resolution from -20°C to 100°C. This design reduces energy/conversion by 7x and improves resolution-FOM by 16x relative to other sub-nW temperature sensors, while simultaneously improving the operating range, decreasing the area, and providing competitive resolution and inaccuracy that are suitable for energy-harvesting IoT applications. The key to this performance is the use of gate leakage currents for both the sensing and sampling elements, which enable ultra-low power operation and a highly compact area. We demonstrate a gate leakage-powered oscillator for direct temperature-to-frequency conversion using a resolution-inaccuracy co-optimization design methodology. Additionally, we present a digitally-trimmable, gate leakage-based relaxation oscillator that serves as a voltage and temperature-robust internal sampling frequency reference for the sensor.

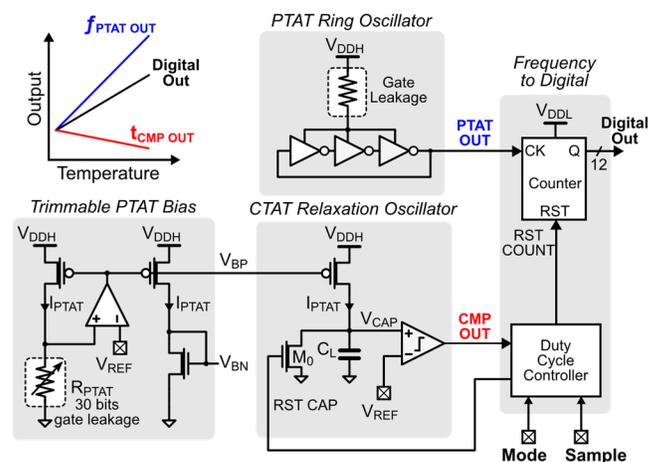


Fig. 1: Schematic diagram of the proposed gate leakage-based temperature sensor.

## II. ARCHITECTURE AND DESIGN METHODOLOGY

Fig. 1 shows the system architecture of the proposed temperature sensor, which consists of a proportional-to-absolute-temperature (PTAT) ring oscillator with output PTAT OUT, a PTAT reference current  $I_{PTAT}$ , a complementary-to-absolute-temperature (CTAT) relaxation oscillator (RXO) with output CMP OUT, and a frequency-to-digital converter with a duty cycle controller. Temperature samples are taken either continuously or on-demand by counting the frequency of PTAT OUT during the charging time of the CTAT RXO, resulting in a digital output with a PTAT characteristic. This all-digital quantization approach avoids the inherent conversion nonlinearity and high area overheads caused by resistor and capacitor-based alternatives such as in [5], and allows the counter and controller to be run at a lower supply voltage than the rest of the sensing system to reduce power consumption. Fig. 2 demonstrates timing waveforms of the sensor operation. During a sample, PTAT OUT oscillates and clocks the counter, while the PTAT bias charges  $V_{CAP}$  in the RXO until it crosses  $V_{REF}$  and toggles CMP OUT. The controller detects this event, duty-cycles the RXO, and resets the digital counter. Due to the pA-level bias current used in the RXO, unanticipated leakage currents at the  $V_{CAP}$  node such as subthreshold leakage through the reset switch  $M_0$  or gate leakage through the comparator input can cause temperature instability. To control leakage,

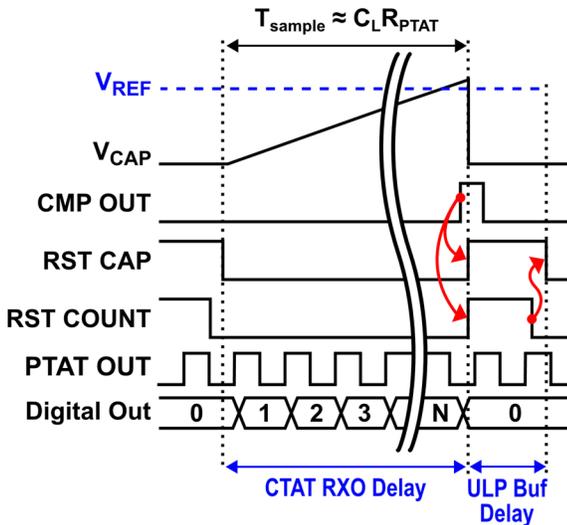


Fig. 2: Timing diagram of sensor operation.

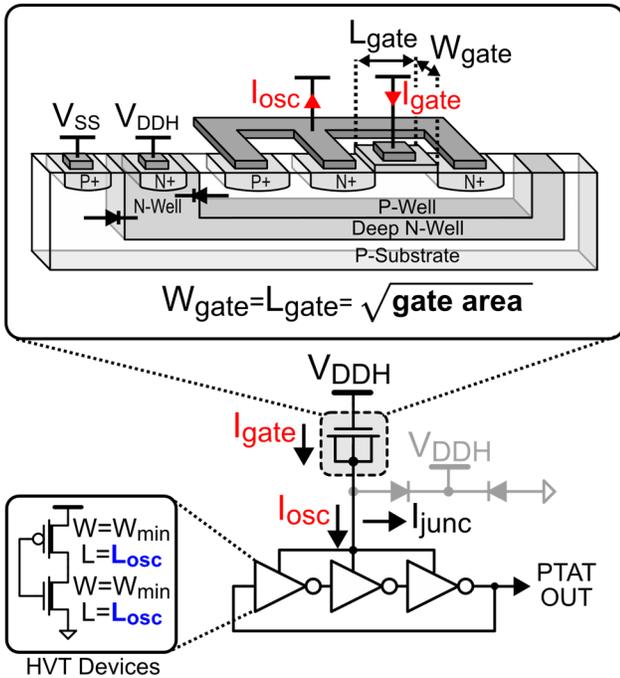


Fig. 3: Direct PTAT frequency generation using a performance co-optimized gate leakage-powered oscillator.

both the comparator and  $M_0$  use thick-oxide devices, and  $M_0$  is divided into stacked devices with long channel lengths to further minimize subthreshold conduction. This increases the on-resistance of  $M_0$ , causing  $C_L$  (820 fF) to discharge slower at the end of each RXO cycle. To improve the discharge speed, we level shift RST CAP to the high-voltage domain to overdrive  $M_0$ . Also, a leakage-based ultra-low-power (ULP),  $\mu s$ -delay buffer gives  $C_L$  adequate time to discharge between temperature samples.

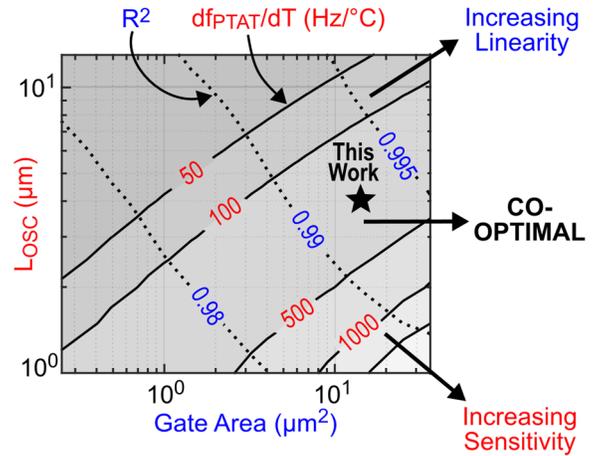


Fig. 4: Resolution-inaccuracy co-optimization design methodology used to pick sizing for the PTAT oscillator.

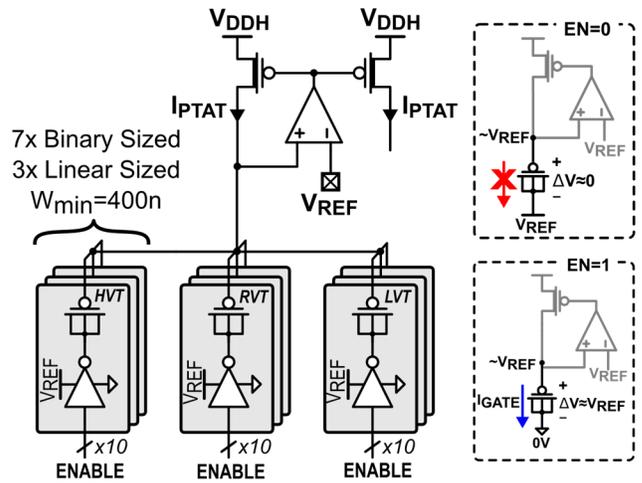


Fig. 5: Digitally-trimmable PTAT reference current using multi-threshold gate leakage.

#### A. PTAT Ring Oscillator

Fig. 3 shows the proposed PTAT gate leakage-powered oscillator. The structure uses a standard ring oscillator that is current-starved by NMOS gate leakage, resulting in a PTAT output frequency characteristic. The PTAT oscillator should have both high temperature linearity ( $R^2$ ) and sensitivity ( $df_{PTAT}/dT$ ), which lead to low inaccuracy and high quantization resolution, respectively. Therefore, we co-optimize these metrics by tuning the gate leakage area and the channel lengths in the ring oscillator,  $L_{osc}$ . This is performed in simulation for each sizing combination by sweeping temperature, fitting the resulting output frequency characteristic to a polynomial regression, and measuring its slope and  $R^2$  value. The tradeoff between the sizing knobs, shown in Fig. 4, reveals orthogonal gradients of increasing linearity and sensitivity. Thus, for co-optimal performance, sizing should be picked for minimal inaccuracy at the desired level of resolution. For this work, we use a gate area of  $11.5 \mu m^2$  and an  $L_{osc}$  of  $4 \mu m$ .

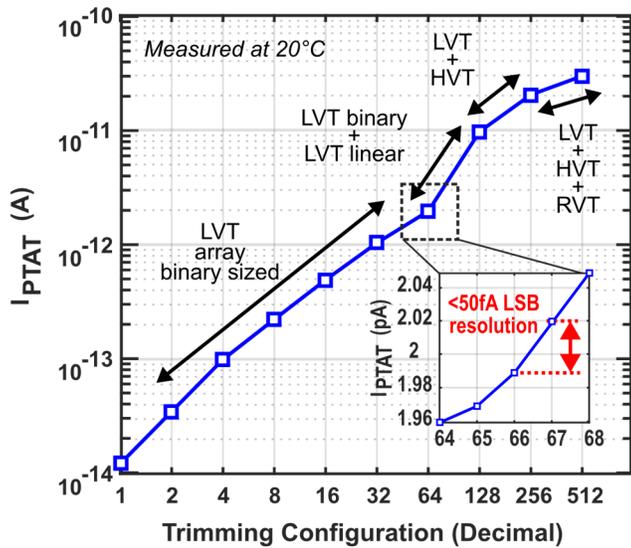


Fig. 6: Measured trimming characteristic of the PTAT reference current.

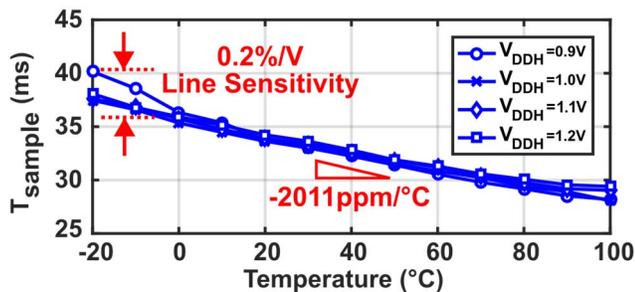


Fig. 7: Measured temperature characteristic and line sensitivity of the CTAT sampling period.

### B. CTAT Relaxation Oscillator

The digitally-trimmable gate leakage-based PTAT current reference ( $I_{PTAT}$ ) shown in Fig. 5 biases the RXO to create a CTAT sampling period.  $I_{PTAT}$  is generated using a voltage-to-current approach in which a self-biased amplifier drives a voltage  $V_{REF}$  across a tunable-area PMOS gate-leakage structure that creates an effective gate-leakage resistance  $R_{PTAT}$  that is  $G\Omega$ -level, allowing tuning of  $I_{PTAT}$ . To tune the effective resistance, the structure is divided into 3 groups of 10 transistors, each group using a different  $V_T$ . Each group contains 7 binary-sized devices (minimum width of 400 nm) and 3 additional devices at the MSB width of 25.6  $\mu\text{m}$ . To enable or disable individual transistors, an inverter directly drives the bottom ‘terminal’ of a device (source, drain, and body) to either  $V_{SS}$  or  $V_{REF}$ , respectively. This allows the voltage drop across each device to be precisely switched on or off without adding any instability to the current source via alternate leakage paths. Fig. 6 shows the measured tuning characteristic of  $I_{PTAT}$  at 20°C. With  $V_{REF}=0.5\text{V}$  and  $V_{DDH} = 0.9\text{V}$ , we extract  $I_{PTAT}$  via measurement of the RXO frequency and show an  $I_{PTAT}$  range of 12 fA to 29 pA with an LSB resolution of <50 fA. Fig. 7 shows the measured sampling period line sensitivity of 0.2%/V from 0.9V to 1.2V and a

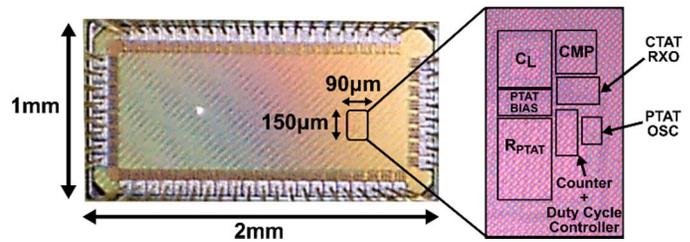


Fig. 8: Chip micrograph of the proposed sensor.

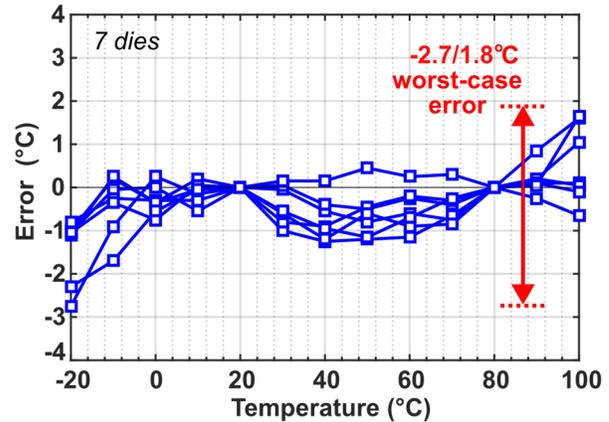


Fig. 9: Measured temperature error from 7 dies.

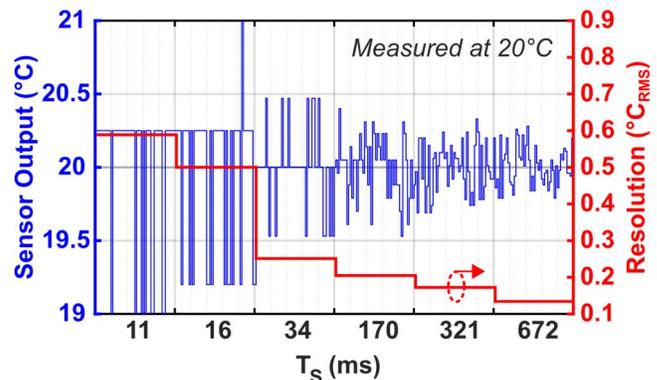


Fig. 10: Measured transient output and RMS resolution versus sampling time.

temperature coefficient (TC) -2011 ppm/°C across the operational temperature range of -20°C to 100°C. Because  $I_{PTAT}$  is proportional to  $V_{REF}$  and the RXO period is inversely proportional to  $V_{REF}$ , the RXO period depends only on  $R_{PTAT}$  and  $C_L$ , allowing relaxed stability requirements for  $V_{REF}$ .

### III. MEASUREMENT RESULTS

The proposed temperature sensor, shown in Fig. 8, was fabricated in a 65nm process and occupies an area of 0.013  $\text{mm}^2$ . At 20°C, the sensor consumes 490 pA from  $V_{DDH}$  (0.9V) and 390 pA from  $V_{DDL}$  (0.5V) for a total power consumption of approximately 640 pW. A sampling period of 34.3ms (20°C) yields approximately 22 pJ/conversion with a quantization noise-limited rms resolution of 0.25°C. Sensors across 7 dies were tested from -20°C to 100°C, and Fig. 9 shows the worst-

TABLE I. COMPARISON WITH STATE-OF-THE-ART LOW-POWER TEMPERATURE-SENSORS

	This Work	CICC'18 [2]	SSCL'18 [3]		ISSCC'17 [4]	Sci Rep'17 [5]	ISSCC'14 [6]	JSSC'14 [7]
Tech	65nm	180nm	65nm		180nm	65nm	160nm	180nm
Temperature Range (°C)	-20 – 100	-20 – 80	0 - 100		-20 – 100	-20 – 40	-40 - 125	0 – 100
Area (mm <sup>2</sup> )	0.013	0.065	0.06	0.11	0.0086	0.15	0.085	0.09
Sampling Time (ms)	34.3	840	1000	0.005	8	4800	6	30
Power (nW)	0.64	13	0.174	242.9	75	0.110	600	71
Energy/Conversion (nJ)	0.022	11	0.174	0.002	0.6	0.540	3.6	2.2
Resolution (°C)	0.25	0.11	0.61	0.88	0.07	0.2	0.06	0.3
Inaccuracy (°C)	-2.7/1.8	-0.7/1.3	-1.1/1.5	-3.9/1.7	-0.22/0.19*	±1.93	±0.4*	-1.4/1.5
Supply Voltage (V)	0.9-1.2 + 0.5	0.8-1.4	1.0 + 0.65		1.2	0.5	0.085	1.2
Resolution-FOM (nJ*K <sup>2</sup> )	0.0014	0.14	0.0648	0.0018	0.0032	0.023	14.29	0.19

\* 3σ value, min/max for the rest

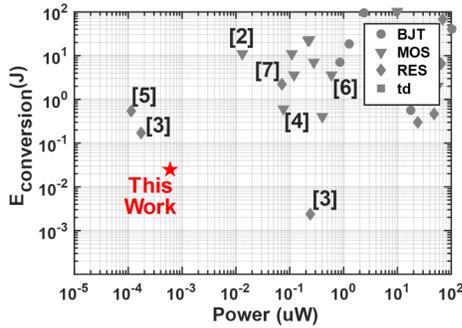


Fig. 11: Energy-Power comparison with existing works

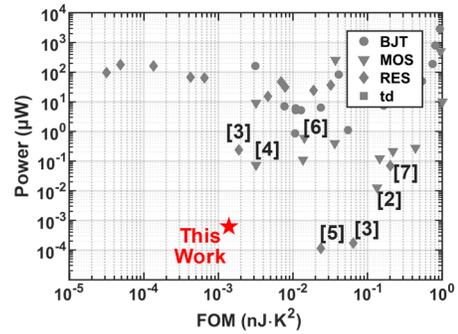


Fig. 12: Power-FOM comparison with existing works

case measured inaccuracy of  $-2.7/1.8^{\circ}\text{C}$  after two-point calibration at  $20^{\circ}\text{C}$  and  $80^{\circ}\text{C}$  with systematic nonlinearity correction. Fig. 10 shows the transient sensor output and RMS resolution versus sampling time, obtained from using different trimming configurations on  $I_{\text{PTAT}}$ .

#### IV. CONCLUSION

Table I summarizes the measured performance and compares this temperature sensor with other state-of-the-art low power and low energy temperature sensors. Fig. 11 and Fig. 12 show that this work achieves the lowest energy reported to date for sub-100 nW sensors and  $>100\times$  power reduction over works with comparable resolution-FOM [3,4]. Amongst sub-100 nW temperature sensors, this work achieves a  $7\times$  reduction in energy and a  $16\times$  improvement in resolution-FOM [2,3,4,5,7]. These state-of-the-art performance improvements are all achieved while maintaining a competitive low area, a full operational temperature range from  $-20^{\circ}\text{C}$  to  $100^{\circ}\text{C}$ , and a low inaccuracy that are ideal for IoT SoCs.

#### ACKNOWLEDGEMENTS

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