University of Virginia

A 23 nW CMOS ULP Temperature Sensor Operational from 0.2 V

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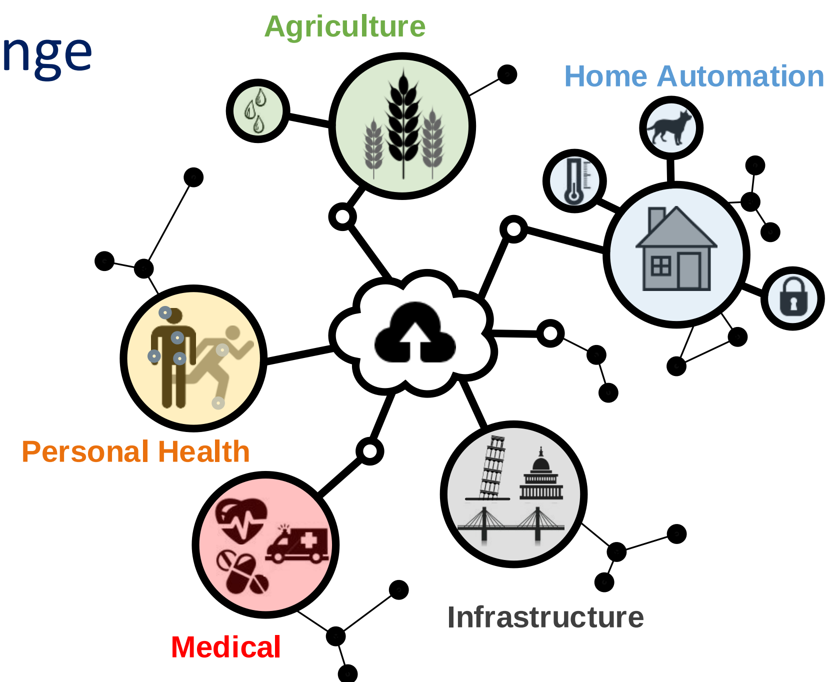
Robust Low Power VLSI

Motivation

- Internet of things (IoT)
- Power consumption is a challenge
- Ultra low power, battery less
- Ultra low voltage operation
  - 2.4 GHz RF receiver at 0.3 V [1]
  - Band gap reference at 0.4 V [2]
  - Energy harvesting from as low as 10mV [3]

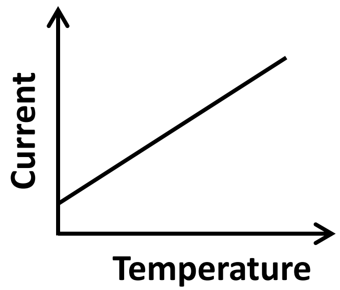


- Temperature sensor integral to IoTs
  - Ultra low power temperature sensor
  - 23 nW, +1.5/-1.7°C max inaccuracy (0°C to 100°C)

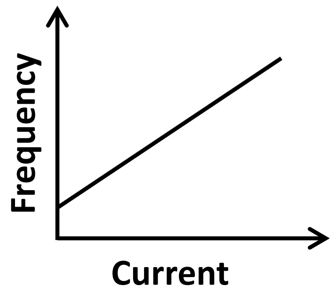
Illustration: Alicia Klinefelter

How does it work?

- Proportional-to-absolute-temperature current source

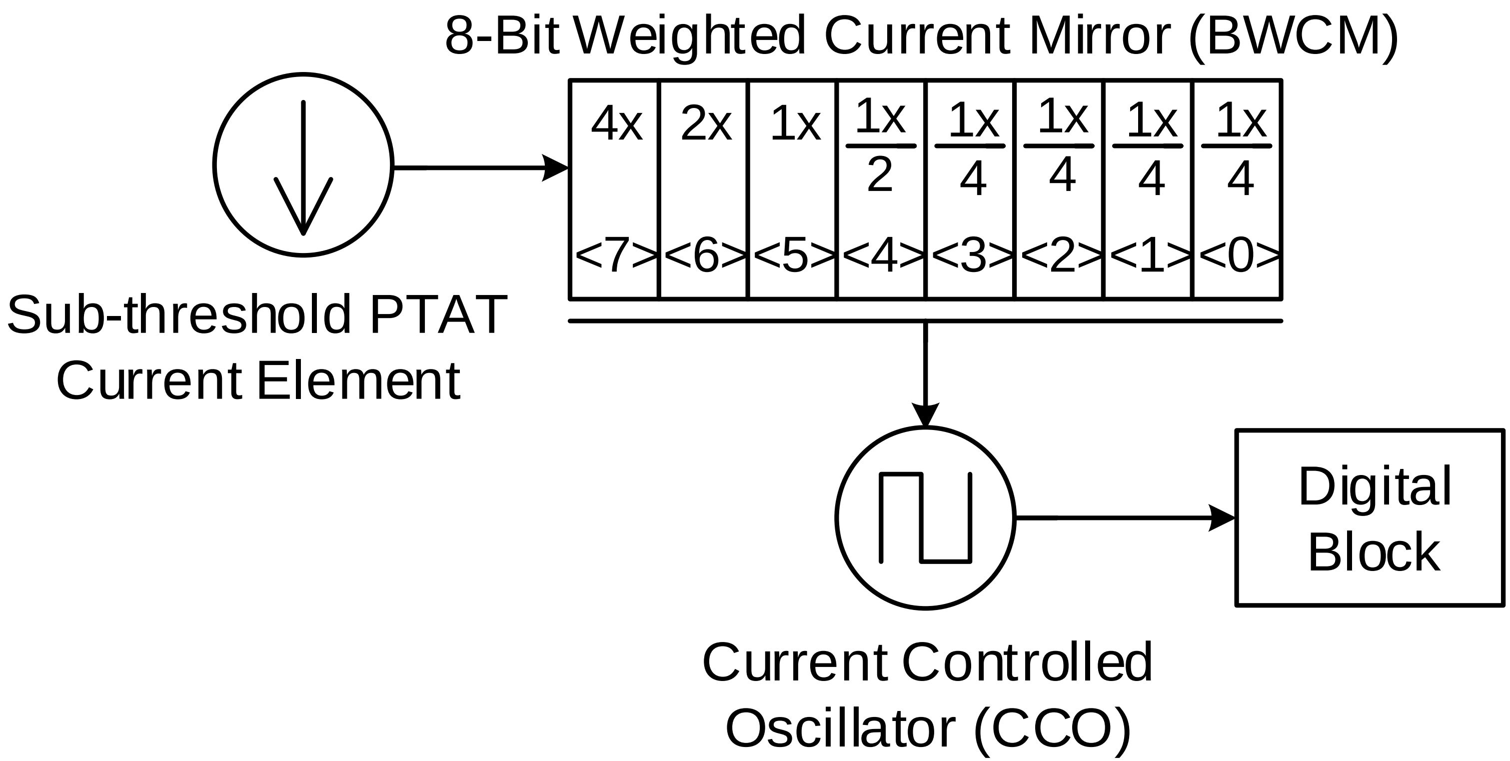


- Current-controlled oscillator



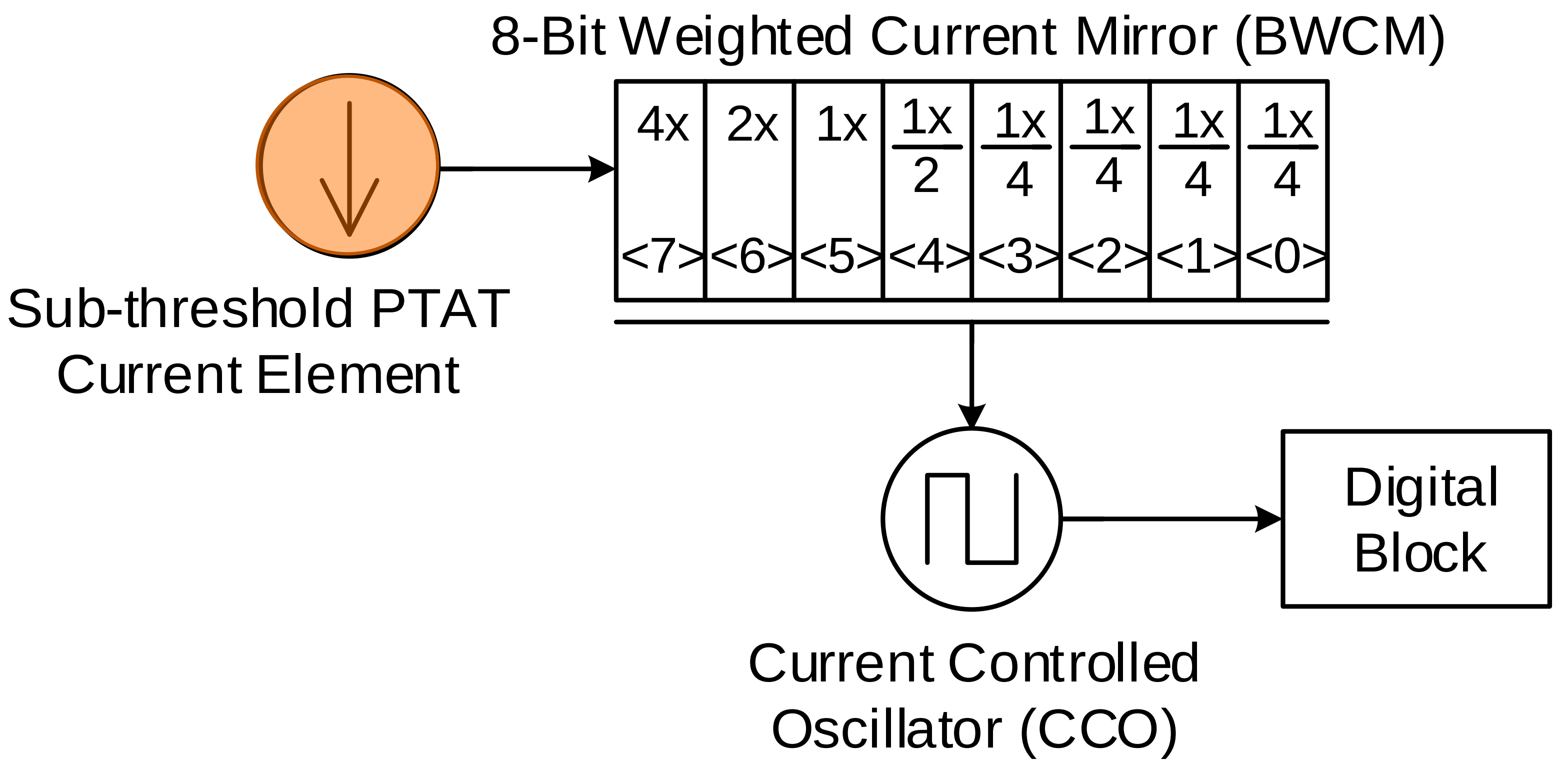
- Frequency proportional to temperature
- How to operate the design at ultra low voltage and power ?

System Diagram

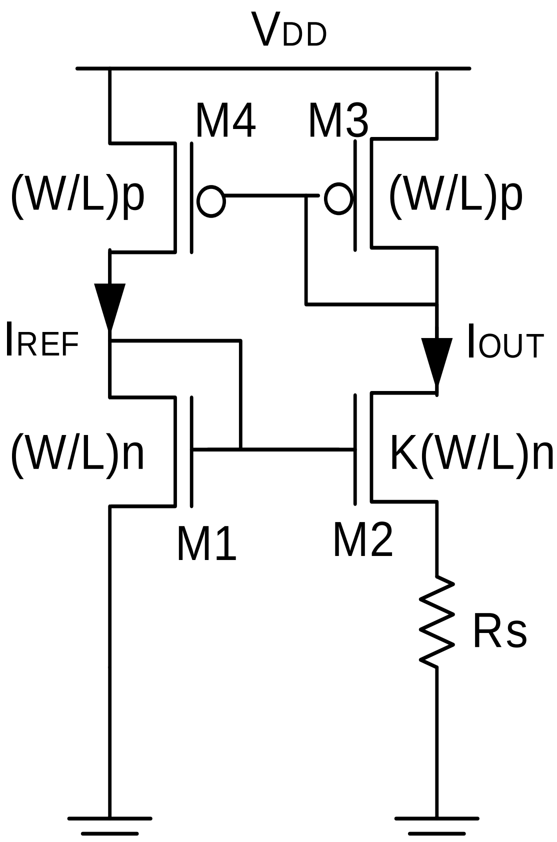


- Core (PTAT + BWCM + CCO) operates at 0.2 V
- Digital block operates at 0.5 V

System Diagram

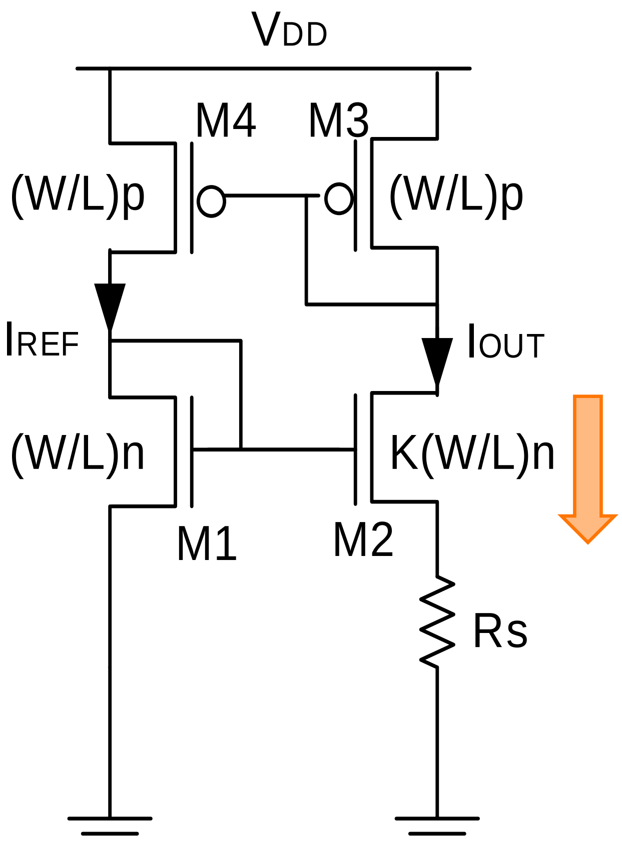


Sub-V_t PTAT Current Element



- Current proportional to temp
- Low headroom at 0.2 V
- Thin oxide standard-V_t devices
  - Threshold voltages ~0.2 V
- Long channel
  - Avoids short channel effects
- Sub-V_t saturation region
  - $V_{DS} > 3\phi_t$ (ϕ_t=kT/q).

Sub-V_t PTAT Current Element



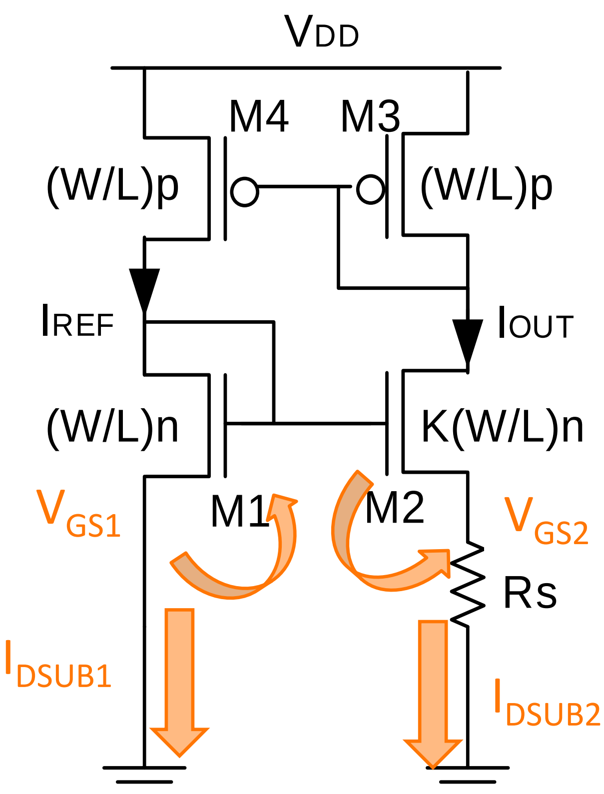
Drain current:

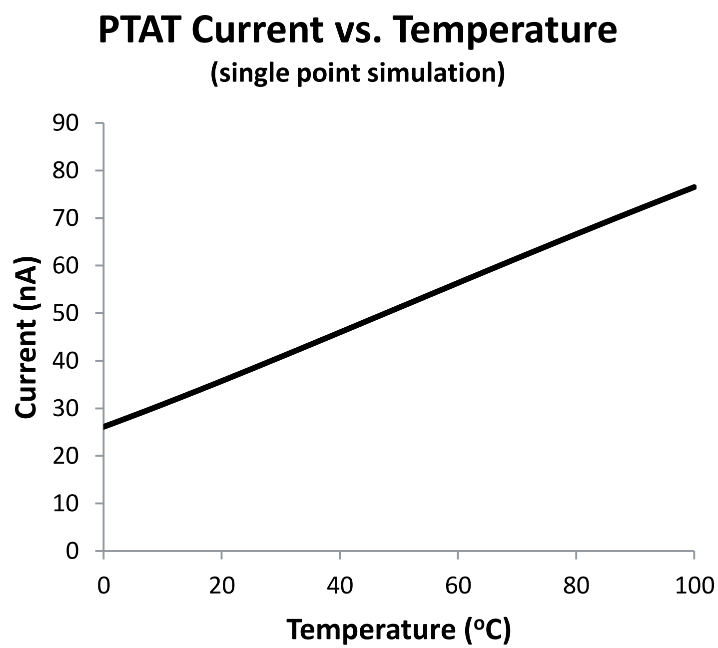
$I_{DSUB}=I_O\exp((V_{GS}-V_T)/n\phi_t)$ for $V_{DS} > 3\phi_t$.

$I_O = \mu_O C_{OX} (W/L) (n-1) \phi_t^2$
(drain current @ $V_{GS} = V_T$)
μ_o: carrier mobility
C_{ox}: gate oxide capacitance
W and L: channel width and length
n: subthreshold slope factor.

Equation for V_{GS} : $n\phi_t \log_e(I_{DSUB}/I_o)+V_T$

Sub-V_t PTAT Current Element





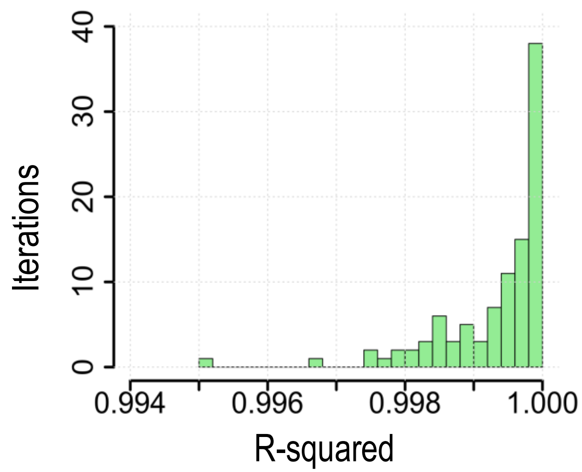
Kirchoff's voltage law: $V_{GS1} = V_{GS2} + I_{DSUB2}R_S$

$I_{DSUB1} = I_{DSUB2} = I_{OUT}$, $V_{T1} = V_{T2}$

$I_{OUT}=n\phi_t \log_e K/R_S$ ➔ I_{OUT} proportional to temperature

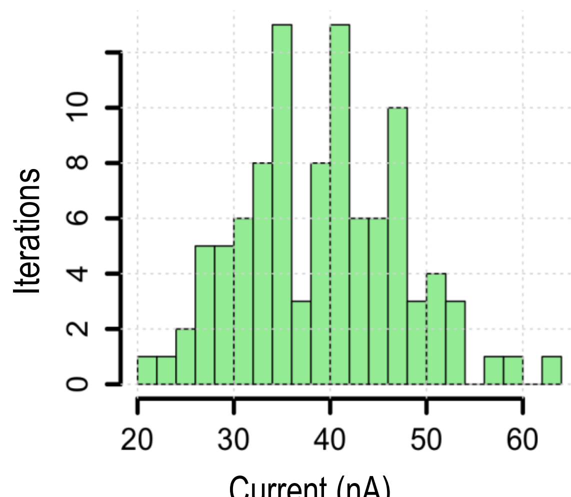
Sub-V_t PTAT Current Element

- Linearity



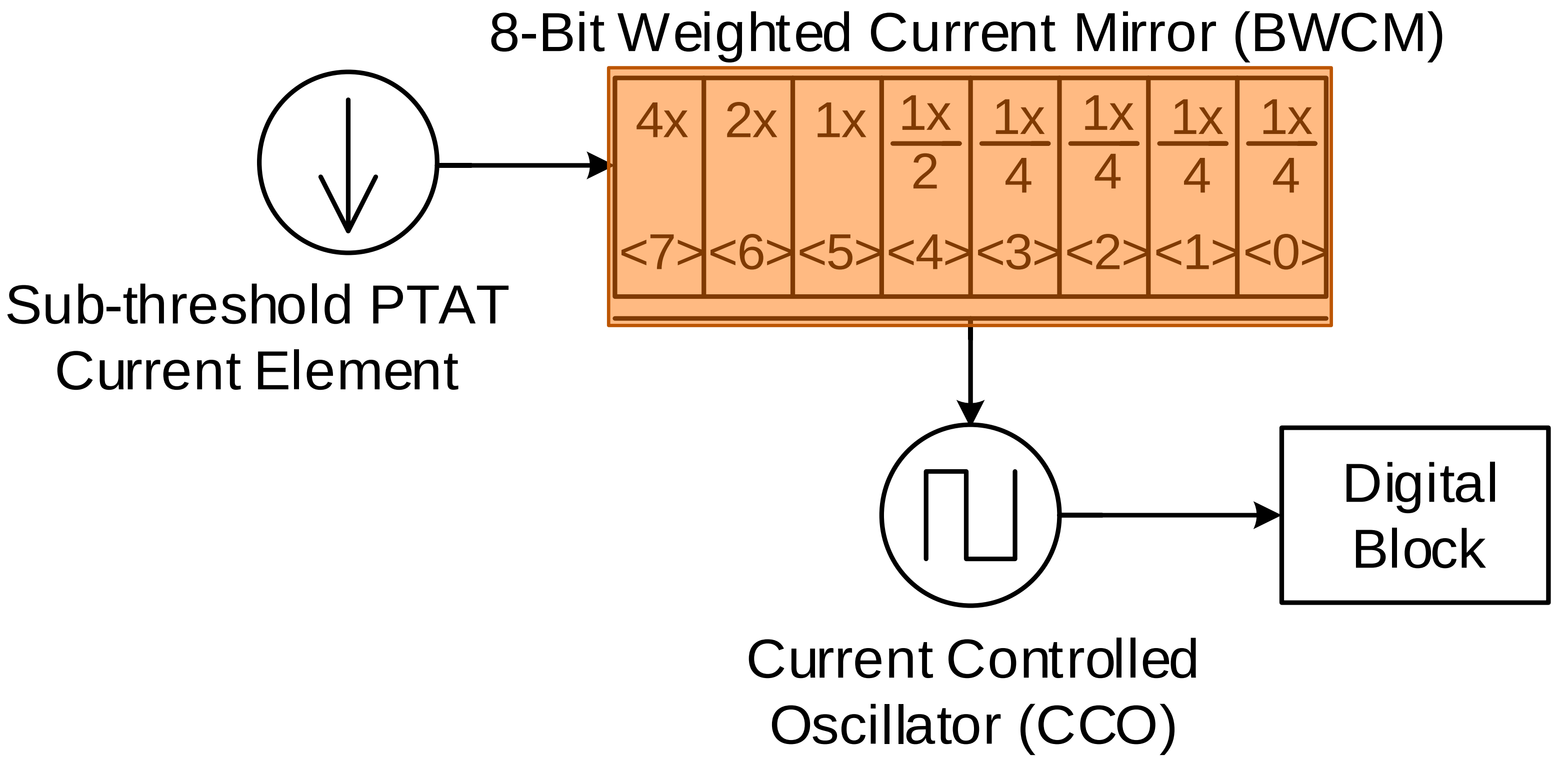
Mean R^2 = 0.9993,
3σ R^2 = 0.0024.

- Current

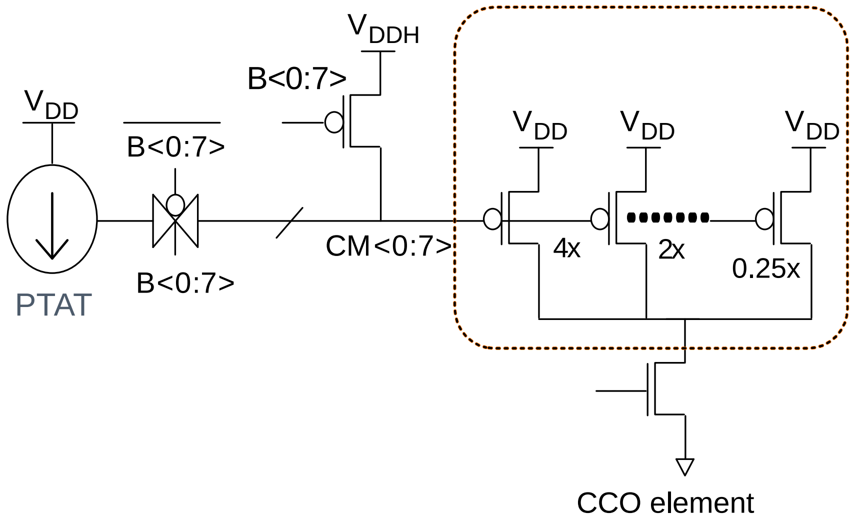


Mean current at 25ºC = 39nA
3σ variation = 25nA
Quite high! Bit weighed current mirror to deal with it

System Diagram

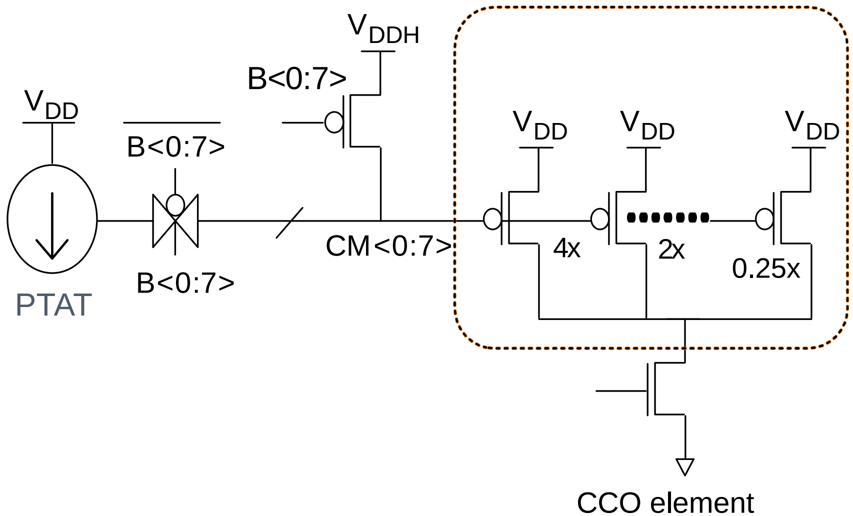


Bit-weighted Current Mirror



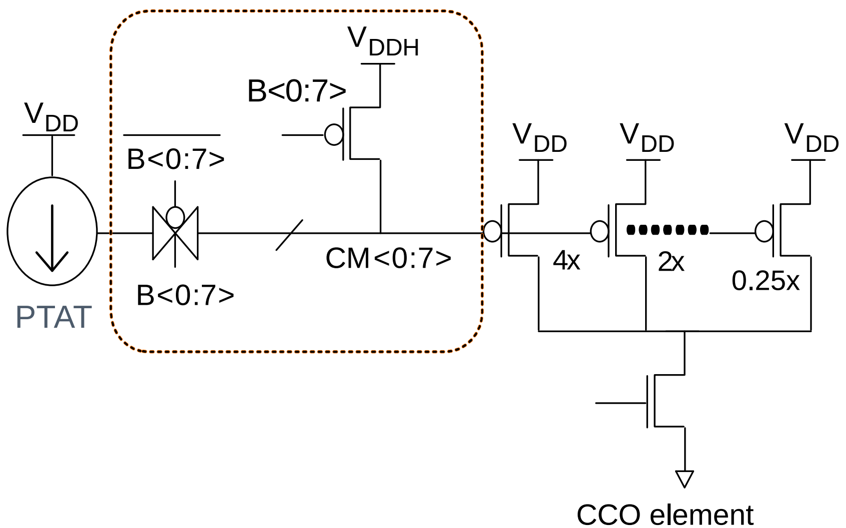
- BWCM starves oscillator transistors

Bit-weighted Current Mirror



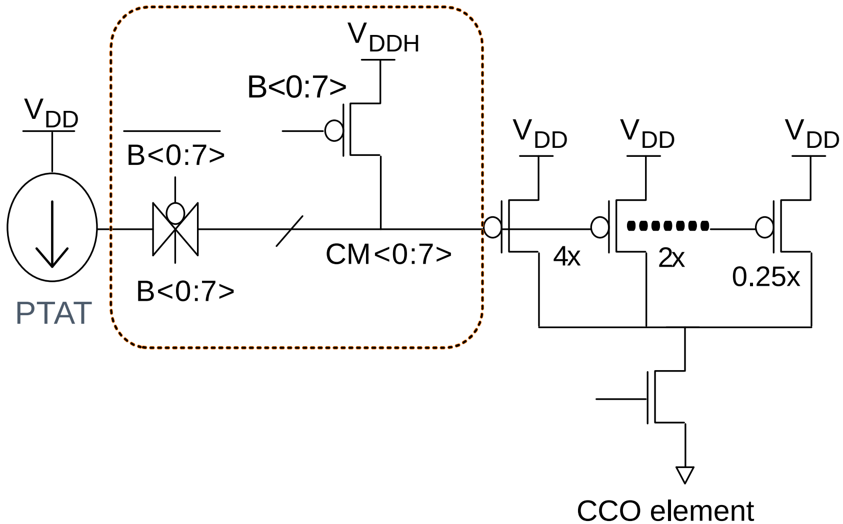
- BWCM starves oscillator transistors
- 8 weighted branches
- Strong process ➔ high PTAT current ➔ lower bit setting ➔ scales BWCM current

Bit-weighted Current Mirror

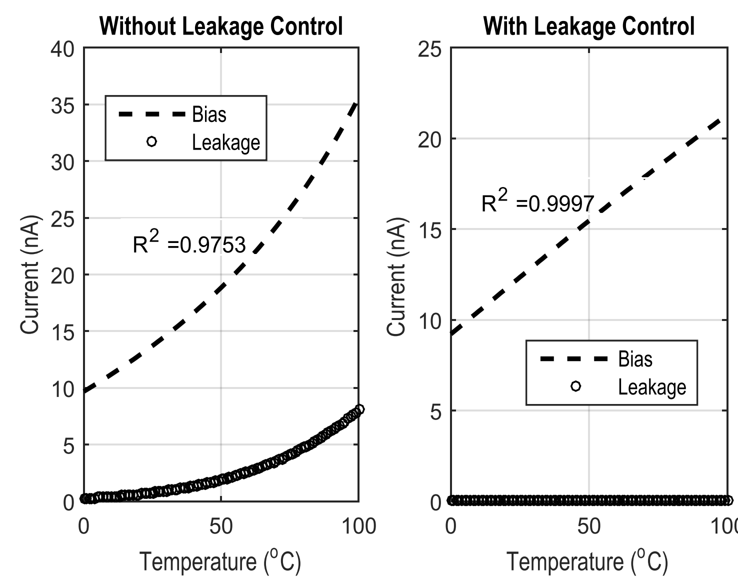


- BWCM starves oscillator transistors
- 8 weighted branches
- Strong process ➔ high PTAT current ➔ lower bit setting ➔ scales BWCM current
- Off transistors ➔ leakage current dominates
- Leakage control

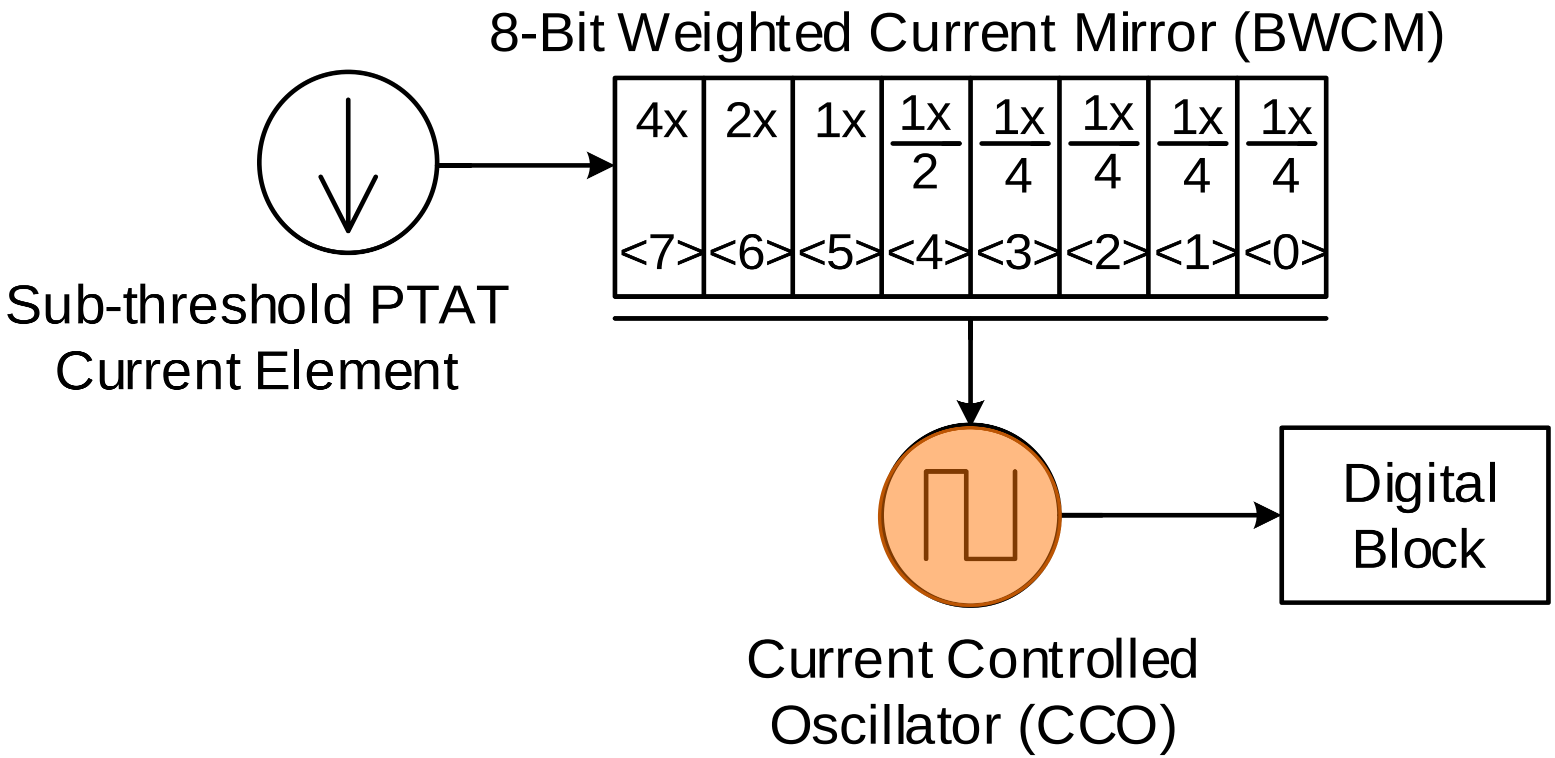
Bit-weighted Current Mirror



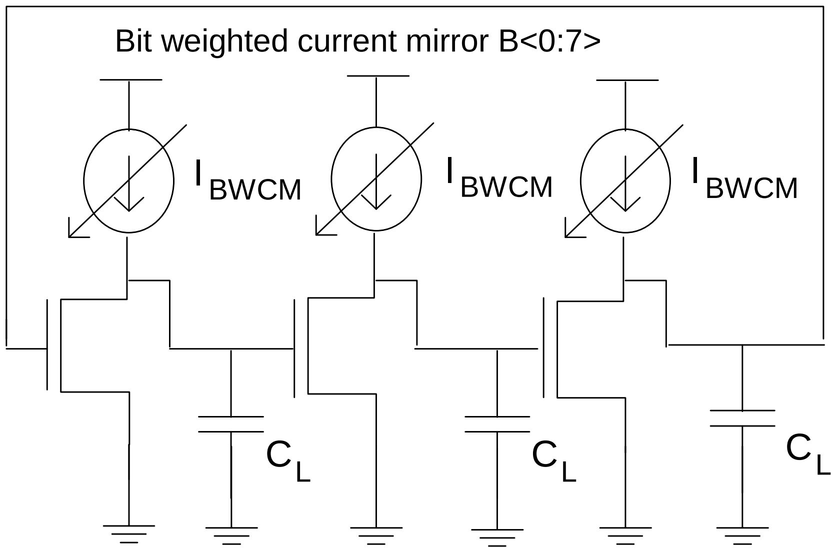
- Leakage control
- Transistor gate tied to 0.5 V
- Negative V_{GS} reduces leakage



System Diagram

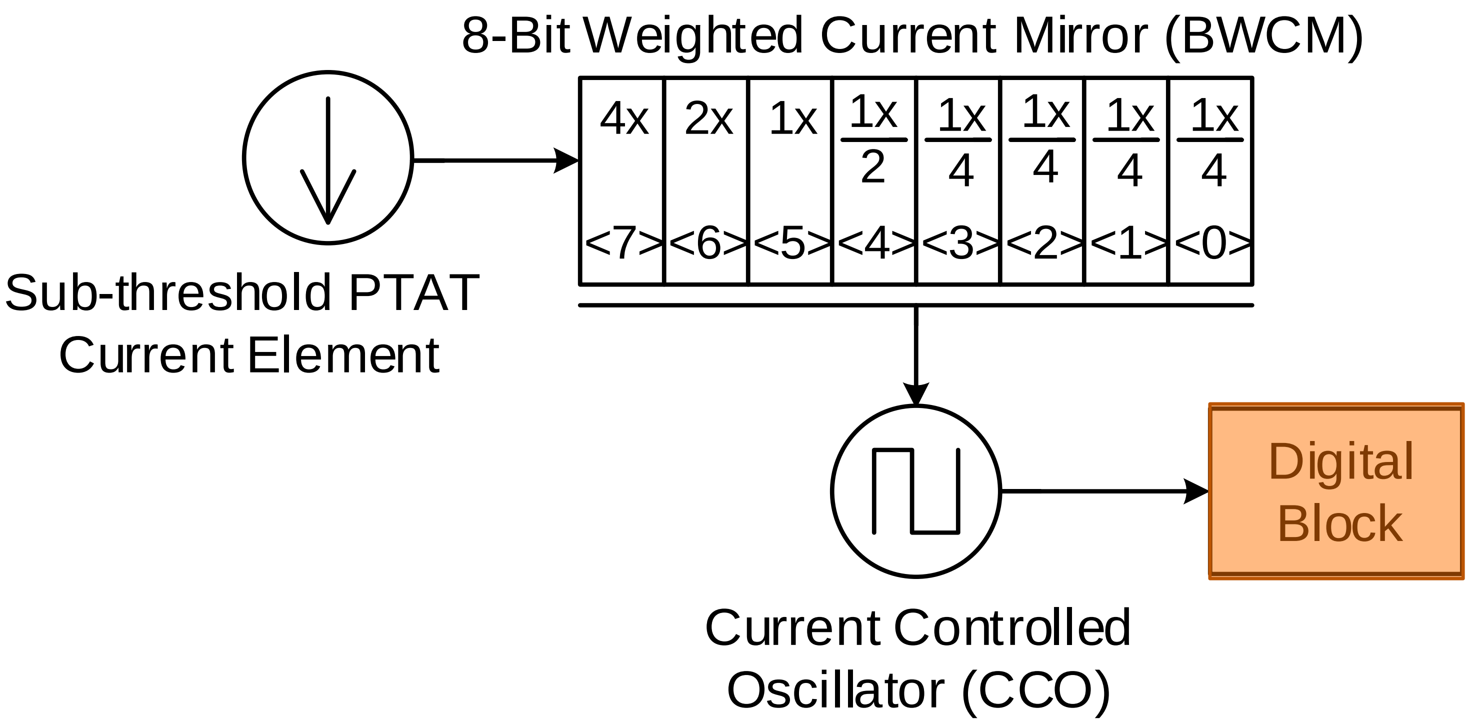


Current Controlled Oscillator

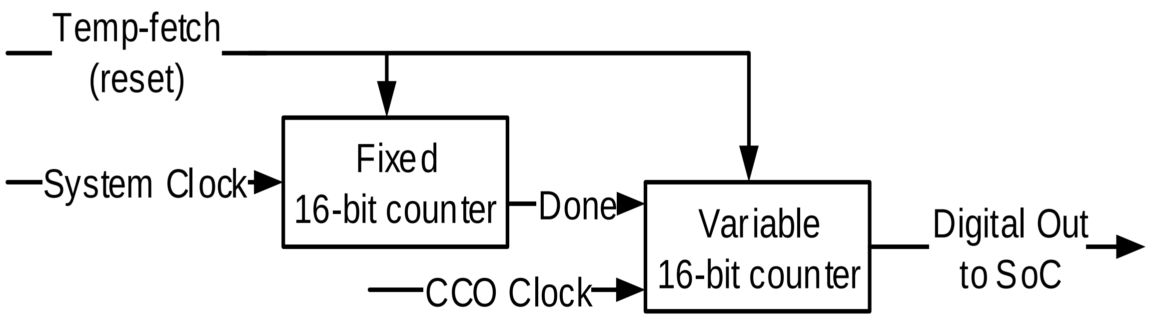


- NMOS-only CCO
- Its drive strength is process trimmed
- Frequency determined by I_{BWCM} and C_L (MIM cap)

System Diagram

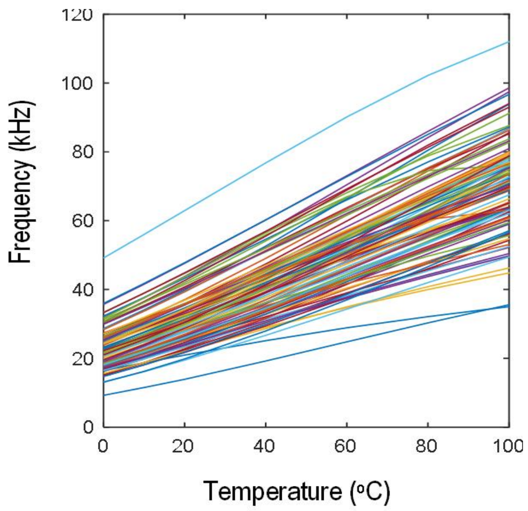


Digital Block



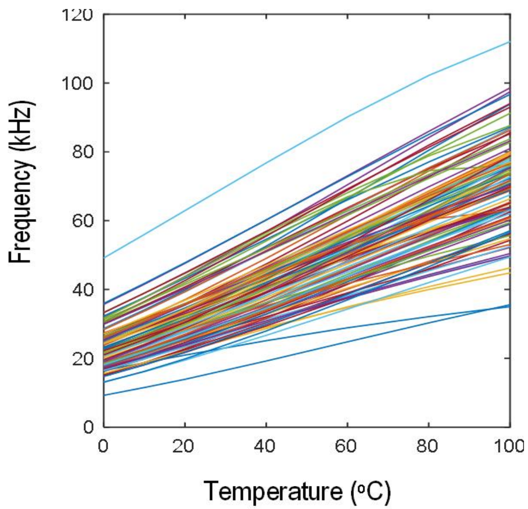
- Digitally synthesized using low leakage high-V_t logic
- 2 counters: fixed and variable
- Fixed counts system clock cycles and asserts *done*
- Variable counts CCO clock cycles until *done*
- Output: digital code

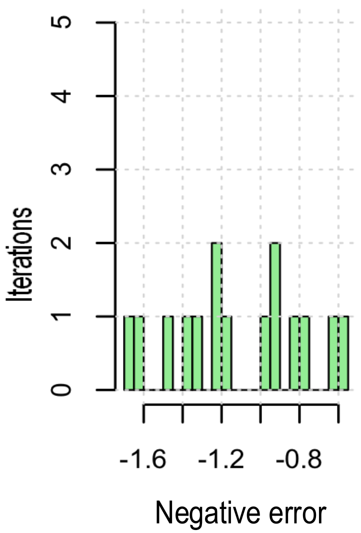
Results

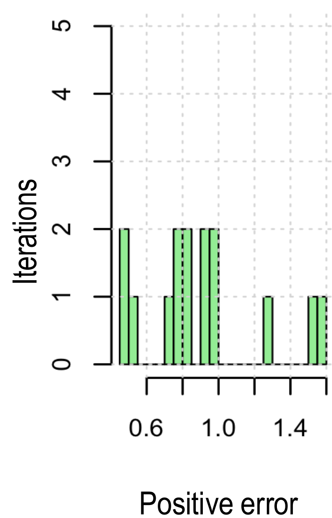


- Frequency vs. temperature w/o process trimming

Results







- Frequency vs. temperature w/o process trimming
- To measure inaccuracy
  - Set B<0:7> to control BWCM
  - Set P<0:3> to control drive strength
  - 2-point calibration at 10^{o}C and 80^{o}C
- Inaccuracy
  - Mean = +1.0/-1.2 ^{o}C
  - Max = +1.5/-1.7^{o}C
- Resolution
  - Programmable counters enable resolution-power trade-off
  - 0.008^{o}C/LSB

Results

- Supply noise variation
  - 0.032^{o}C/mV
  - Improved by decoupling capacitors
  - Focus on low-load systems, LDO can provide well-controlled supply
- Power consumption
  - Core power = 18 nW at 0.2 V
  - Total power (+ locking circuit, + level shifters, + digital block at 0.5 V) = 23 nW
  - Lower sampling rate ➔ further power savings

Comparison with Prior-art

Work	Node (µm)	V_{DD} (V)	Inaccuracy	Power (nW)	Energy/ conversion
This work	0.13	0.2,0.5	+1.5/-1.7°C	23	0.23nJ
S. Jeong et al JSSCC 2014 [4]	0.18	1.2	+1.3 /-1.4 °C	71	2nJ
S.C. Luo et al TCASI-2014[9]	0.18	0.5,1	+1/-0.8 °C (-10-30°C)	120	3.6nJ
Y. S. Lin et al CICC-2008[10]	0.18	1	+3/-1.6 °C	220	22nJ
M. K. Law et al TCASII-2009[11]	0.18	1.2	+1/-0.8 °C	405	0.41nJ
K. Souri et al ISSCC-2012[6]	0.16 DTMOST	0.85	+/-0.4°C(3σ) (-40-125°C)	600	3.6nJ
Node is CMOS and sensor range is 0-100°C unless mentioned otherwise					

- 3x lower power than recent work [4]
- Comparable inaccuracy to recent work [4]

Conclusion

- ULP temperature sensor for IoT applications
- Core operates down to 0.2 V, digital block at 0.5 V
- Sub-V_t operation of PTAT
- BWCM resists process-induced power variations

- System power consumption = 23 nW
- Max inaccuracy = +1.5/-1.7^{o}C from 0^{o}C to 100^{o}C with a 2-point calibration
- The analog core is 150x100µm^2 and the total system is 250x250µm^2

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Questions?