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A 1pJ/bit Bypass-SPI Interconnect Bus with I²C Conversion Capability and 2.3nW Standby Power for Fabric Sensing Networks

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***Abstract*— Enabling self-powered in-fiber or in-textile sensing systems necessitates the development of a compact, highly expandable, and ultra-low-power (ULP) communication protocol. This work presents an ULP "bypass-SPI" chip-to-chip interconnect bus designed specifically for fabric-based network communication, requiring only a fixed set of four wires. This interconnect bus allows the chips to bypass the interconnect signals to the downstream chips using a dedicated bypass procedure, facilitating small form factors. A voltage and direction controller is integrated on-chip, which allows the expansion of interconnect signals in multiple directions, supporting mesh-style distributed fiber networks and enabling voltage shifting. Moreover, this interconnect bus is synthesizable, compatible with the standard SPI interfaces, and can be converted into an I²C protocol, significantly improving its flexibility. Fabricated in 65nm CMOS technology, measurements of the chip show that the chip achieves a minimum standby power of 2.3 nW and reduces the energy per cycle by over 17× down to 1 pJ/bit, compared to prior art. The communication between bypass-SPI chips and a RISC-V SoC is also measured, confirming the suitability of this interconnect bus for energy-and-space-constrained fabric-based sensing applications.**

Keywords—communication protocol, interconnect bus, fabric system, network communication, bypass-SPI, I²C, ultra-low-power.

I. INTRODUCTION

Aggressive power and size reduction of modern internet-of-things (IoT) systems-on-chip (SoCs) has opened possibilities for the development of self-powered fiber computers that are integrated so thoroughly into fibers that they are invisible in the garment. These computers offer sensing and computation capabilities for applications such as on-body sensing, smart cables/carpet, and invisible surveillance [1]. However, the design of interconnect buses within the confined space of mm-scale dimensions presents significant challenges. These interconnects need to accommodate a fixed wire count for small form factor, ensure high efficiency with nW power consumption for energy saving, and be fully synthesizable and compatible for low-cost adoption. Additionally, in future fabric-based networks that integrate a multitude of electronic components, it is crucial to handle network flexibility in terms of protocol conversion, routing directions, and voltage choices. This flexibility is crucial as different regions of the network may employ their own unique protocols with varying voltage levels and speeds.

Several recent systems achieve system-in-fiber (SiF) operations [1]-[8]. The SiF [1] achieves self-powered Na+ sensing with a display screen controlled by a 10-bit I/O interface. But it consumes >4 mW power and it is impractical for sensing network due to the increasing complexity of the I/O interface with the number of components. The work in [3] supports self-powered I²C communication between SoCs and sensors but needs μW power and relies on bulky batteries. For the microsystems in [4]-[7], although self-powered operation with nanowatt (nW) power and mm-scale size are achieved, they all need a dedicated base station to power, communicate, and program the SoCs, which limited inter-SoC communication. More recently, a study in [8] achieves nW operation, full autonomy, and asynchronous in-fiber SPI communication, but the SoC can only communicate with the adjacent SoCs in one dimension, limiting the expandability and speed. As a result, none of the prior SiFs or microsystems can support flexible chip-to-chip communication in a fabric-based sensing network.

In addition, existing bus standards failed to address this limitation. Open-drain/collector-based designs (e.g., I²C [9]) allow the devices to drive 0 on the bus. This results in high active power consumption due to the large current flowing through the pull-up resistor when the bus is driven low. A low power variant of I²C [10] was proposed to replace the pull-up resistors with logic circuits to reduce active power, but it still requires a local clock running 5× faster than the bus clock and custom design, limiting its scalability. Another variation, a 1-wire bus [11], uses only one wire to power and communicate, saving space. But the data transmission relies on driving the lines to 0 for different period of time, which limits the maximal transmission rate to 16.3 kbps and requires strict timing. The SPI protocol [12], while not having the pull-up overhead, requires a chip-select signal for each slave chip, resulting in an excessive number of wires and violating the area constraints. The daisy-chained SPI variation, eliminates the chip-select overhead but introduces a significant overhead when sending a command to a device, as the command buffer of all the devices in between must be filled. Recently, Mbus [13] is proposed specifically designed for microscale system achieving low power and a fixed wire count. However, it is a complex protocol that lacks compatibility with most commercial standards, thereby hindering its adoption in various applications. Therefore, fabric systems have a pressing need for new interconnect buses that meet the challenges of fixed

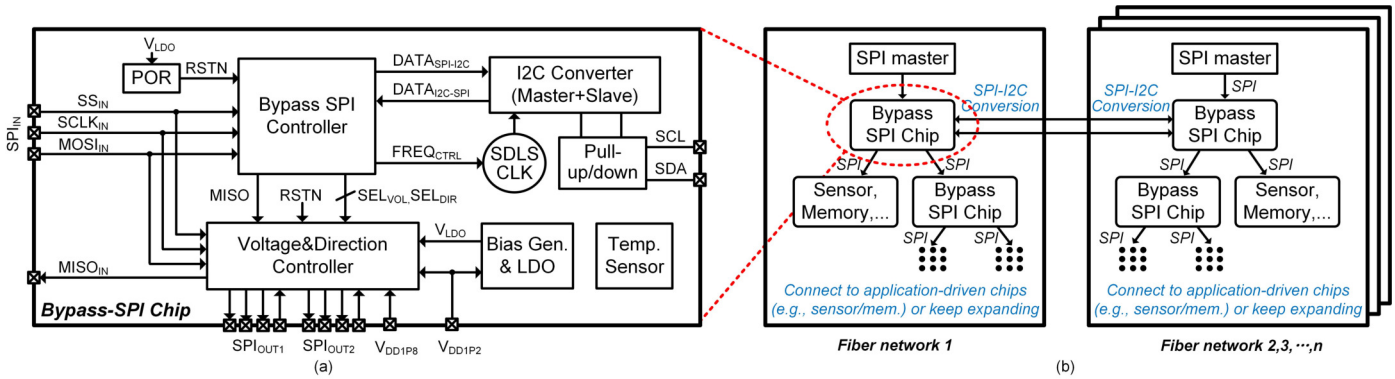

Fig. 1. (a) the block diagram of the proposed bypass-SPI chip. (b) The connection and architecture of a fabric sensing network enabled by the bypass-SPI chips.

wire count, ultra-low-power (ULP), compatibility, and flexibility in protocol conversion, signal re-routing, and voltage choices for fabric-based sensing network.

This paper proposes a synthesizable ULP interconnect scheme that expands on a SPI protocol to allow communication to any nodes sharing the SPI bus without needing chip select signals. Called bypass-SPI, this scheme gives a low overhead way to configure and operate a network of in-fiber or in-textile devices with multiple convenient features. These features include master-to-multi-slave communication using only 4 fixed wires, support for direction expansion and voltage level shifting, protocol (I^2C) conversion, compatibility with standard SPI protocol, as well as integrated ID-check and ID-update functions for dynamic chip identification (ID) allocation and management without the reliance on non-volatile memories or complex factory pre-programming [14]. Fabricated in 65 nm CMOS, this chip achieves a minimum of 2.3 nW standby power, a maximum operating speed of 1.5 MHz at 0.6 V, and a minimum of 0.9 pJ/bit energy consumption, demonstrating its low power consumption, high throughput, and high energy efficiency. Three of the chips were tested with a RISC-V SoC, showing its expandability, I^2C conversion capability, and compatibility with a modern SoC and the standard SPI protocol.

II. System Architecture and Implementation

A. System Overview

Fig. 1(a) shows the block diagram of the proposed bypass-SPI chip. The chip includes a bypass-SPI (slave) controller, a voltage and direction controller (VDC), a pW temperature sensor [15], a power-on-reset (POR) block, an I^2C converter, a pull-up/down block, a clock for I^2C, and an LDO with bias generator (BG). The entire system operates using a single supply voltage, V_{DD1P2} (1.2 V). The on-chip nW LDO with the BG generates an internal V_{LDO} (0.6 V) to power all the components on-chip except for the level-shifters (LS) in the VDC, which are powered by the V_{DD1P8}. The bypass-SPI chip has one input SPI port (SPI_{IN}) and two output ports (SPI_{OUT1} and SPI_{OUT2}) as well as an I^2C interface (SDA, SCL). With the proposed VDC, the signals from the SPI_{IN} can be bypassed and level-shifted to either SPI_{OUT1} or SPI_{OUT2}. The I^2C converter can convert the SPI signals to SCL/SDA lines, facilitating I^2C communication. With all these functions integrated on-chip, the chip can provide a fully self-contained, expandable, and flexible communication solution for fabric-based sensing networks. In addition, as shown in Fig. 1(b), the proposed bypass-SPI chip empowers the SPI master to establish communication with any device within the network. Additionally, the SPI-to-I^2C conversion capability enables network-to-network communication.

B. Voltage and Direction Controller for Expandability

Fig. 2 shows the schematic of the voltage and direction controller. Two control signals, SEL_{DIR} and SEL_{VOL}, are utilized to control the bypass direction and interface voltage. The direction controller utilizes AND gates to determine the appropriate bypass direction. The voltage controller (VC) incorporates multiple LS and transmission gates to control the voltage level of the $SPI_{OUT1,2}$ among 0.6 V, 1.2 V, and 1.8 V. By default, the SEL_{VOL} is 0 such that no LS is enabled, and the SPI output ports work at 0.6 V. Since the $MISO_{OUT}$ line does not need voltage up-shifting, a digital buffer is used for this line. To avoid floating voltages and short circuit current, the EN_{ZERO} signal by default is set high to ensure the SS, SCLK, and MOSI are set to 0. This digital implementation with LSs contributes to the low power consumption at sub-nW levels.

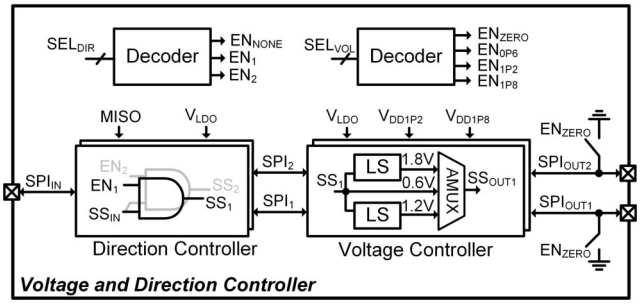

Fig. 2. The schematic of the voltage and direction controller (VDC).

C. Bypass-SPI Control Algorithm and Chip-ID Setup

Fig. 3 (a) demonstrates the flow chart of the bypass-SPI control algorithm. The bypass-SPI supports five commands: *global control*, *ID check*, *ID update*, *write*, and *read*. When a SPI master intends to talk to a bypass-SPI chip, two methods can initiate the conversation. The first method involves checking the chip's ID by sending a specific *ID check* command followed by the chip's ID. Each chip has a dedicated register to store the chip ID, ID_{LOCAL}. If the ID sent by the master matches with the ID_{LOCAL}, the bypass-SPI chip sets the

CHK_{IN} signal to high, indicating that it has been selected (enabled). Then the bypass-SPI chip becomes responsive to the *read*, *write*, and *ID update* commands from the master. Conversely, when the CHK_{IN} signal is low, the bypass-SPI chip ignores these commands. The other method is to use the *global control* command which has higher priority than other commands. This command allows the master to write data into all the bypass-SPI chips it has access to in a broadcast fashion. Once the master successfully selects (enables) the bypass-chip with the correct chip ID, it can modify the SEL_{VOL} and SEL_{DIR} registers to decide the bypass direction and interface voltages. Furthermore, the master can enable the I^2C converter by modifying the $DATA_{SPI\text{-}I2C}$ to convert from SPI to I^2C, further improving the expandability and compatibility.

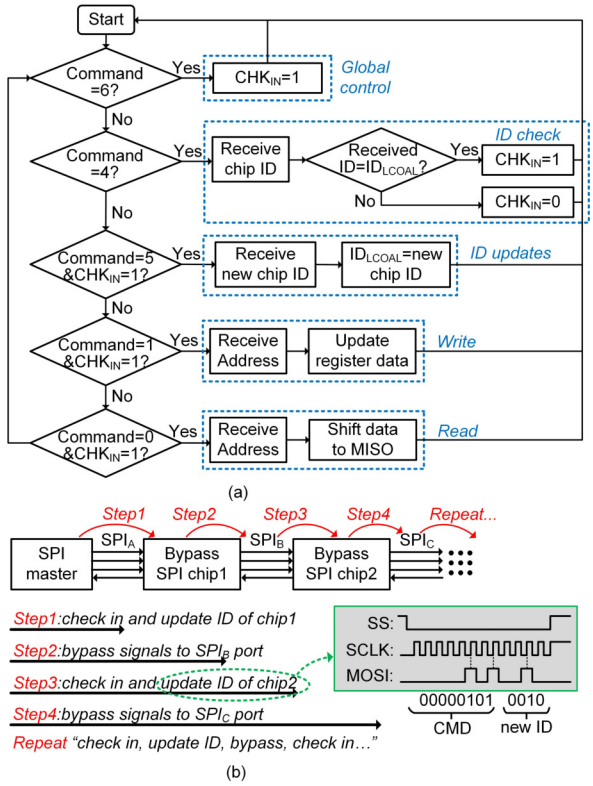

Fig. 3. (a) the flow chart of the proposed bypass-SPI control algorithm. (b) the procedure and example of chip ID setup.

In addition, these functions and commands enable flexible chip ID setup and management. They facilitate the convenient integration of new devices and bypass-SPI chips into a networked system. Fig. 3(b) shows the chip ID setup procedure. Initially, all the bypass-SPI chip IDs are 0 after fabrication, and their bypass functions remain disabled. Therefore, the SPI master can only access the nearest bypass SPI chip, which is chip1 in Fig. 3(b). The SPI master needs to select (enable) it by using chip ID "0". Then, it can update chip1's chip ID to a non-zero value and modify the SEL_{DIR} register value to bypass the signals to chip2. Since the default chip ID of chip2 is also 0, the SPI master can repeat the previous process to check ID with chip2, update its ID and access the bypass-SPI chips farther away. In this design, the command width is set to 8 bits and the chip ID is set to 4 bits. Fig. 3 (b) also provides an example of how to update the chip ID.

D. I^2C Conversion

To achieve SPI-to-I^2C conversion, the I^2C converter block incorporates a I^2C master and slave based on [16]. Through the $DATA_{SPI\text{-}I2C}$ and $DATA_{I2C\text{-}SPI}$ data bus, the SPI master can talk to the bypass-SPI controller to change the data value on the $DATA_{SPI\text{-}I2C}$ buses to enable either the I^2C master or slave. The required data set is transferred to the I^2C converter over the $DATA_{SPI\text{-}I2C}$ bus, including the write/read enable signals, Chip ID, register address, etc. Furthermore, a small 64-bit buffer is added, allowing the SPI master to read data that the I^2C received and stored when the I^2C acts as a slave. This buffer is small for testing purposes but can be enlarged for improved performance if needed.

III. Measurement Results

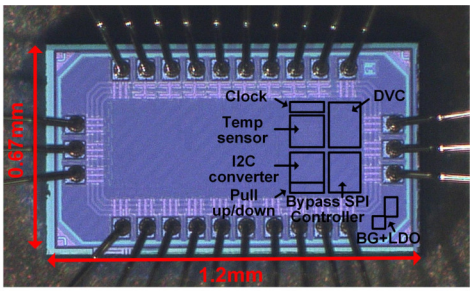

Fig. 4. Chip micrograph of the bypass-SPI chip.

The bypass-SPI chip is fabricated in 65 nm CMOS technology with an active area of only 0.084 mm^2. Fig. 4 shows the chip micrograph of the bypass-SPI chip.

A. System Behaviors with an ULP RISC-V SoC

An ULP RISC-V SoC [17] is co-tested with three bypass-SPI chips to validate the functionality. The SoC connects the three bypass SPI chips in a serial configuration, as shown in the top of Fig. 5. The SPI interfaces between these chips from left to right are SPI_A to SPI_D. The bottom of Fig. 5 shows the measured waveform for the chip-to-chip communication. Here, we only show the SCLK and MOSI lines to be concise. The SoC first checks ID with the bypass SPI chip1 and updates its chip ID. Then the SEL_{VOL}, and SEL_{DIR} are modified by the SoC to bypass the signals to the second bypass-SPI chip. By iteratively repeating the process, the SoC can assign each slave chip a unique ID. After the ID setup, the bypass chain is built and the SoC can easily communicate with any of the chips within the chain. The SoC sends ID check commands with chip1's ID and changes the SEL_{VOL} to control the interface voltage. All slave chips receive these commands, and only chip1 responds and alters the voltage of the SPI port from 1.2 V to 0.6 V. The functionality of the global control command was also validated, as all chips in the chain executed the command to up-shift the interface voltage back to 1.2 V.

B. Power Consumption and Energy Efficiency

The quiescent power of the bypass-SPI and I^2C converter are measured across supply voltage, as shown in Fig. 6 (a), with VDD_{IP8} connected to GND. The bypass-SPI controller with the VDC achieves a 1.26 nW quiescent power.

Meanwhile, the I²C converter, including the pull-up/down blocks and clock, achieves a 1 nW quiescent power. Therefore, the overall chip demonstrated a quiescent power of 2.26 nW. The measured active power and energy per bit, E_{PB}, is shown in Fig. 6 (b)(c). When the LS is disabled and the SPI interfaces are operating at the V_{LDO} domain, the chip achieves a minimum E_{PB} of 1 pJ/bit at 50 kHz, and 0.6 V VDD during data writing. The chip also achieves a maximal operating frequency of 125 kHz with 91 nW active power at 0.7 V (limited in this chip by the driving ability of the PAD driver). When the LS is enabled to up-convert the SPI signals to 1.2 V, the system can work at a higher frequency of 1 MHz at 0.6 V. In post-APR simulation, the bypass SPI can support >100 MHz operation at 1.2 V.

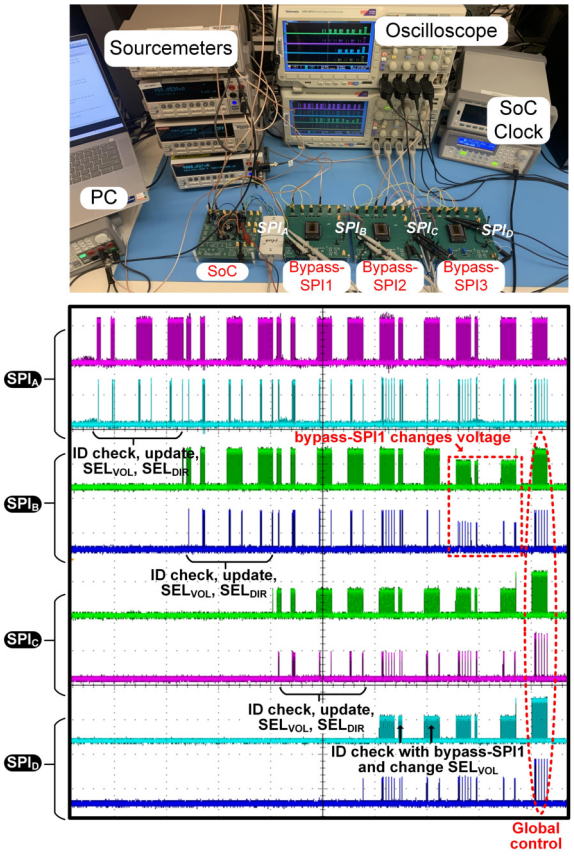

Fig. 5. The testing setups and measured timing waveform for chip-to-chip communication.

C. Comparison with the state-of-the-art

Table I compares the proposed bypass-SPI interconnect bus with the state-of-the-art custom protocols for mm-scale system. Our interconnect bus offers full duplex and the highest energy efficiency of 1pJ/bit, which is more than 17× lower than the previous art. Besides, it is compatible with the standard SPI protocol, fully synthesizable, and can support chip ID management, which shows better flexibility and scalability. By eliminating the pull-ups and operating at a low supply voltage, our bypass-SPI achieves a 2.3 nW quiescent power at 0.4 V and 91 nW active power at 125 kHz with a VDD of 0.7 V. By integrating the I²C converter, POR, BG, and LDO on-chip, this chip is fully self-contained and provides an excellent solution for the next generation fabric-based sensing networks.

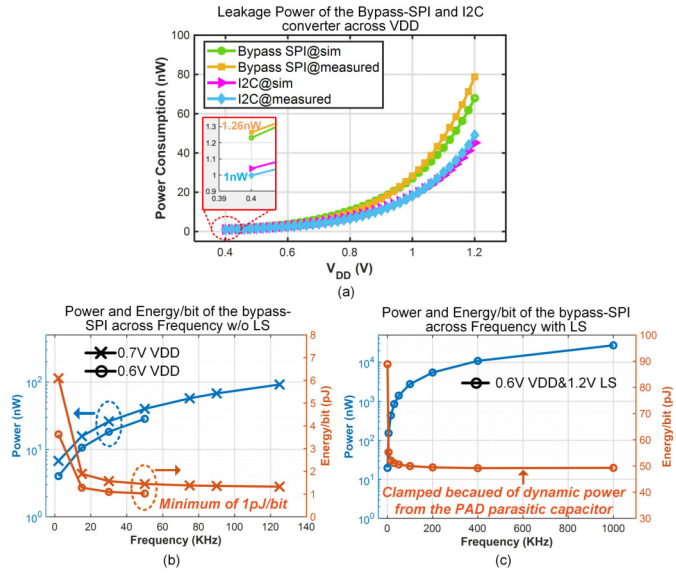

Fig. 6. (a) Measured and simulated leakage power of the bypass-SPI and I²C converter across VDD. (b) The active power and energy per bit of the chip across frequency without voltage level-shifting and (c) with 1.2 V LS.

Table I: Comparison of the state-of-the-art for mm-scale applications.

	1-Wire [11]	Mbus [13]	Lee-I2C [10]	This Work
Number of Lines	1 with pull-ups	2	2	**4**
Data Transfer	Half duplex	Half duplex	Half duplex	**Full duplex**
No. of Master Devices	Single	Multiple	Multiple	**Single**
Devices ID Management	No	No	No	**Yes**
Standby Power	N/R	8nW@Bus System	<11nW	**2.3nW**
Synthesizable	Yes	Yes	No	**Yes**
Broadcast Messages	No	Yes	No	**Yes**
Compatibility	No	No	With Standard I2C	**With Standard SPI**
Energy Efficiency	N/R	17.6pJ/bit	88pJ/bit	**1pJ/bit**

IV. Conclusion

To achieve ULP wire communication in a mm-scale fabric-based sensing network with high energy efficiency, compatibility with commercial standards, and flexible expandability, this work designed a dedicated 4-wire bypass-SPI interconnect bus and proposed a 2.3 nW custom chip that supports the bypass-SPI protocol, I²C conversion, signal rerouting, interface level shifting and chip ID management. The measurements show that the bypass-SPI chip achieves the highest energy efficiency of 1 pJ/bit, 1 MHz operating frequency at 0.6 V, and successful communication with an RISC-V SoC, demonstrating its reliability and deployability in real applications.

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