

A 0.6-V 44.6-fJ/Cycle Energy-Optimized Frequency-Locked Loop in 65-nm CMOS With 20.3-ppm/°C Stability

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Abstract—This letter presents an energy efficient, temperature-compensated frequency-locked loop (FLL) for use as an on-chip clock source. We first present a fully integrated FLL architecture that significantly improves energy efficiency by using a loop divider to boost the output frequency without requiring increased static power dissipation. We develop models for the FLL energy-per-cycle and temperature stability and use them to implement an energy-optimized and highly temperature-stable FLL design in 65-nm CMOS that achieves 20.3-ppm/°C temperature stability from -20°C to 60°C and an energy efficiency of 44.6-fJ/cycle at 23°C (45.3 nW at 1.016 MHz), which is the highest energy efficiency reported to date for a fully on-chip oscillator, regardless of architecture, operating frequency, or temperature stability.

Index Terms—Clocking, digital clock, energy efficient, frequency-locked loop (FLL), low energy, oscillator.

I. INTRODUCTION

On-chip oscillators are a popular choice as clock sources for battery-powered digital circuits and systems-on-chip (SoCs) since they can operate at low power and do not require off-chip passives, unlike crystal oscillators (XTALs). Two key performance requirements for on-chip oscillators are high energy efficiency to improve battery lifetime and high-temperature stability to ensure robust data sampling and reliable communication synchronization. Previous work in on-chip oscillators includes a variety of structures, such as comparator-based relaxation oscillators (RXOs) [1]–[4] and amplifier-based frequency-locked loops (FLLs) [5]–[7] that leverage RC time constants to provide good temperature stability, generally in the range of 1–100 ppm/°C. However, the energy-per-cycle of these oscillators remains in the pJ-range, which is comparable to the energy-per-cycle of an entire digital processor. In RXOs, this energy limitation is typically due to the dynamic power consumption of the comparator. FLLs improve on this issue by replacing the comparator with a low-power amplifier, therefore becoming limited by the static power consumption of bias currents and bias circuitry [4], [7].

To improve the lifetime of battery-powered SoCs, we present an energy-efficient FLL architecture that significantly reduces energy-per-cycle to a level that is over an order of magnitude lower than that of a digital processor while maintaining state-of-the-art temperature stability. To accomplish this, we model the energy efficiency of the FLL architecture and introduce design optimizations to reduce the energy contributions of the biasing circuitry that typically limits FLL energy efficiency. Key design choices to enable this optimization are: 1) the use of a loop divider to boost output frequency without needing to increase bias currents or static power; 2) designing the FLL to

Manuscript received August 2, 2019; revised September 17, 2019 and October 3, 2019; accepted October 4, 2019. Date of publication October 10, 2019; date of current version October 30, 2019. This article was approved by Associate Editor Pui-In Mak. This work was supported by NSF NERC ASSIST Center under Grant EEC-1160483. (*Corresponding author: Daniel S. Truesdell.*)

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Digital Object Identifier 10.1109/LSSC.2019.2946767

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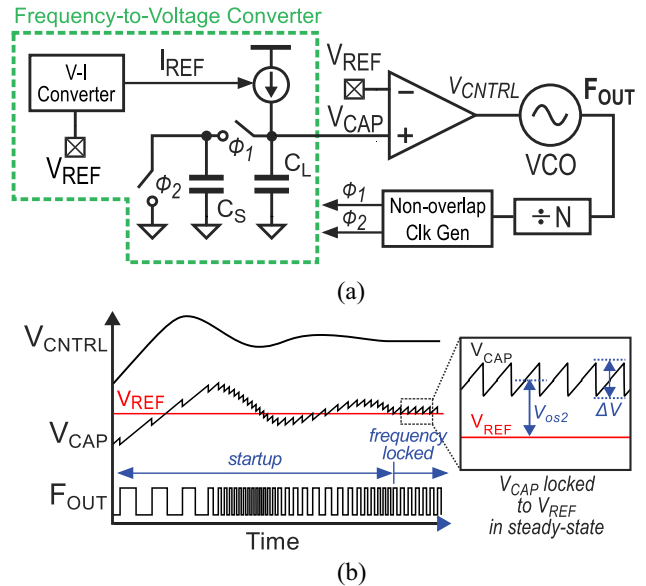


Fig. 1. (a) Architecture of the proposed energy-efficient FLL and (b) conceptual startup waveforms.

operate at low supply voltage; and 3) using an ultralow 0.1-V loop reference voltage.

II. FLL DESIGN AND ANALYSIS

A. Architecture and Operation

Fig. 1(a) and (b) shows the architecture and conceptual operating waveforms of the FLL, respectively. The operating principle of the FLL is to regulate a voltage-controlled oscillator (VCO) to a fixed frequency by driving it with an error signal (V_{CNTRL}) between the VCO output frequency and a fixed input reference voltage V_{REF} . To continuously compare the VCO frequency to V_{REF} , a frequency-to-voltage converter (FVC) transforms the instantaneous VCO frequency into a voltage V_{CAP} . Variations in temperature cause shifts in the VCO gain which causes the output frequency F_{OUT} to drift, however, the loop amplifier detects this drift on V_{CAP} and compensates for it in real-time by adjusting V_{CNTRL} . Because changes in temperature are not very fast, the amplifier does not require high bandwidth. The FVC is implemented by injecting a reference current $I_{\text{REF}} = V_{\text{REF}}/R_{\text{REF}}$ onto a switched-capacitor C_S , creating a voltage that is inversely proportional to F_{OUT}

$$V_{\text{CAP}} = \frac{I_{\text{REF}}N}{F_{\text{OUT}}C_S} \quad (1)$$

where the reference current I_{REF} generated by the V - I converter is calculated as

$$I_{\text{REF}} = \frac{V_{\text{REF}} + V_{\text{os1}}}{R_{P0} + R_{N0} + (R_{P0}\alpha_{N0} + R_{N0}\alpha_{N0})T} \quad (2)$$

where R_{P0} and R_{N0} are the 0°C resistances of two series resistors with complementary temperature coefficients α_{P0} and α_{N0} , respectively, V_{os1} is the offset voltage of the amplifier in the $V-I$ converter (shown in Fig. 2), and T is the temperature. The charge redistribution between C_L and C_S during switching in the FVC creates a voltage ripple ΔV on V_{CAP} equal to $V_{CAP}(C_S/(C_S + C_L))$, however, due to the low amplifier bandwidth and a large sizing ratio between C_L and C_S , this ripple is filtered out and does not significantly affect F_{OUT} . F_{OUT} can be solved by equating V_{CAP} and V_{REF}

$$F_{OUT} = \frac{N(V_{REF} + V_{os1})}{C_S(V_{REF} + V_{os2})} \times \frac{1}{(R_{P0} + R_{N0} + (R_{P0}\alpha_{P0} + R_{N0}\alpha_{N0})T)} \quad (3)$$

where V_{os2} is the offset voltage of the loop amplifier. As long as the mismatch between the two amplifiers is low, any shifts in V_{os1} and V_{os2} due to temperature or input common-mode (V_{REF}) should affect both amplifiers equally and therefore cancel out in (3) resulting in no changes in F_{OUT} . Then, if $V_{os1} = V_{os2}$ and $R_{P0}\alpha_{P0} = -R_{N0}\alpha_{N0}$, (3) can be simplified as

$$F_{OUT} \approx \frac{N}{R_{REF}C_S} \quad (4)$$

B. Energy-Per-Cycle

The total power consumption is expressed as a sum of the individual blocks

$$P_{TOTAL} = P_{IREF} + P_{FVC} + P_{AMP} + P_{DIV} + P_{VCO} \quad (5)$$

where $P_{IREF} \approx 3I_{REF}V_{DD}$ is the power consumption of the self-biased $V-I$ reference current generator (current is equally divided between R_{REF} and the two stages of the self-biased amplifier), $P_{FVC} = I_{REF}V_{DD}$ is the power dissipated through C_S in the FVC, and $P_{AMP} = I_{REF}V_{DD}$ is the power consumption of the loop amplifier, which is biased with I_{REF} . The dynamic power of an M -stage digital divider being clocked at a frequency F can be approximated as

$$P_{DIV} = FC_{FF}V_{DD}^2 \sum_{i=0}^M \frac{1}{2^i} \approx 2FC_{FF}V_{DD}^2 \text{ for } M \gg 1 \quad (6)$$

where C_{FF} is the total switched gate capacitance of a single flip-flop. As long as F_{OUT} is sufficiently high, the leakage power of the divider can be neglected. The total energy-per-cycle of the FLL can then be expressed as

$$E_{CYCLE} = \frac{mC_S V_{REF} V_{DD}}{N} + 2C_{FF} V_{DD}^2 + E_{VCO} \quad (7)$$

where m is a fitting parameter for the number of current mirrors ($m = 5$ for this design). Term ① in (7) corresponds to the energy consumption of $V-I$ reference current generator, switched-capacitor C_S , and the loop amplifier. Term ② corresponds to the divider, and term ③, E_{VCO} , is the intrinsic energy consumption of the VCO at a given supply voltage, which sets the absolute minimum achievable energy consumption of the FLL. That is, if all other parts of the FLL were removed so that only the free-running VCO was left, E_{CYCLE} would equal E_{VCO} .

C. Implementation

Fig. 2 shows the full schematic of the FLL design targeting energy-efficient operation. To optimize the energy efficiency, several design steps are chosen in an accordance with (7) to minimize the energy contributions of each FLL component. First, the VCO is controlled with a linear regulation approach using transistor M_0 that reduces its energy dependency on supply voltage from V_{DD}^2 to $V_{DD}V_{RO}$, where $V_{RO} < V_{DD}$. To further reduce the VCO energy, the core

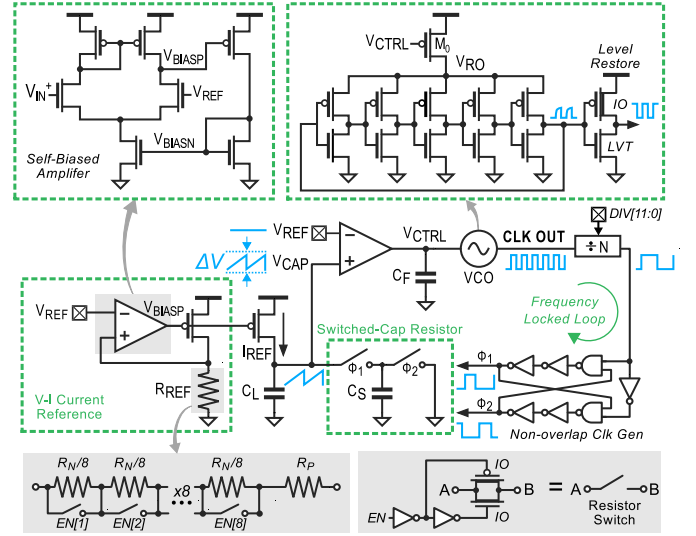


Fig. 2. Full schematic of the FLL.

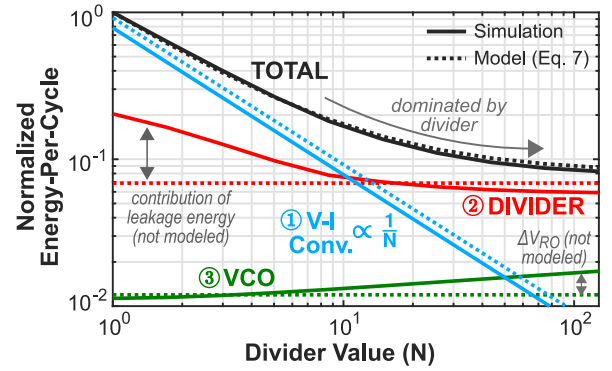


Fig. 3. Energy-per-cycle of the FLL with contributions of individual components obtained from simulation and the model (7).

oscillator is implemented as a 5-stage ring-oscillator (a 7-stage RO increases energy and a 3-stage RO exhibits reduced swing at some operating points) with minimum-sized devices to reduce the total switched capacitance C_{INV} each cycle. Variability in VCO gain due to the small devices does not affect performance since it is automatically compensated within the FLL loop. Thus, term ③ becomes

$$E_{VCO} = 5C_{INV}V_{DD}V_{RO}. \quad (8)$$

The FLL is designed to operate at a low supply voltage of 0.6 V which quadratically reduces term ② and linearly reduces terms ① and ③. The low-voltage operation is accomplished by biasing both amplifiers in the subthreshold region. Finally, significant energy reduction of term ① is achieved by picking a small C_S value of 300 fF ($C_L = 20$ pF and $C_F = 10$ pF), using a low V_{REF} value of 0.1 V, and scaling up the divider value N . Fig. 3 shows the normalized energy-per-cycle of this design versus the divider value N for both simulated values and the model in (7). When $N = 1$, term ① dominates the total energy. Increasing N provides a proportionally higher F_{OUT} which proportionally increases P_{DIV} and P_{VCO} but causes no change in P_{IREF} , P_{FVC} , and P_{AMP} . As a result, terms ② and ③ remain unchanged versus N , but term ① decreases inversely with N .

Temperature compensation is achieved by splitting R_{REF} into two separate resistors with opposing temperature coefficients as mentioned in (2). R_P is implemented as a $P+$ diffusion resistor without salicide, and R_N is an 8-bit trimmable $P+$ poly resistor without salicide. Together, their total resistance equals 49 M Ω in our target

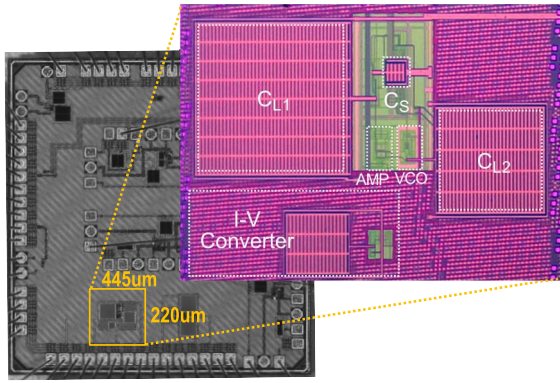


Fig. 4. Annotated chip micrograph of the FLL in 65-nm CMOS.

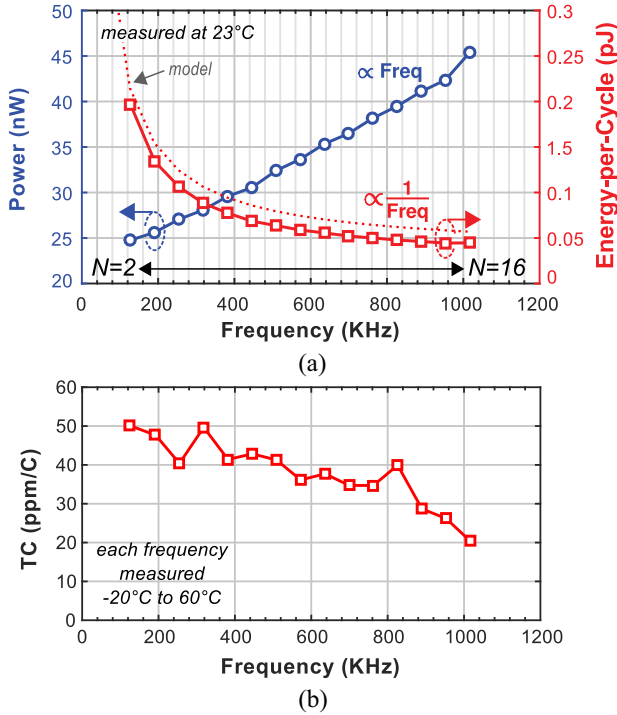


Fig. 5. (a) Measured power and energy versus output frequency and (b) temperature coefficient versus output frequency. Output frequency is tuned by changing divider value N .

design. The optimal trim setting R_N can be determined by measuring the FLL output versus trim setting at two different temperatures (e.g., room temperature and 40 °C) in order to find the setting that yields the smallest slope [see Fig. 7(b)]. Further absolute frequency trimming could be implemented by adding trim to R_P or C_S .

III. MEASUREMENT RESULTS

The proposed FLL design was fabricated in a 65-nm low-power process occupying an area of 0.098 mm². Fig. 4 shows an annotated chip micrograph. At room temperature (23 °C), the base frequency ($N = 1$) is approximately 63.5 kHz, which deviates from the theoretical value of $1/R_{REF}C_S$ by 10 kHz, which is equivalent to an added parasitic capacitance on C_S of around 35 fF. Fig. 5(a) shows the measured power and energy of the FLL versus output frequency, where the output frequency was tuned by sweeping the divider value N from 2 to 16. Due to the low supply voltage, the output frequency for this design becomes supply limited for N greater than 16. Increasing the frequency causes a proportional increase in

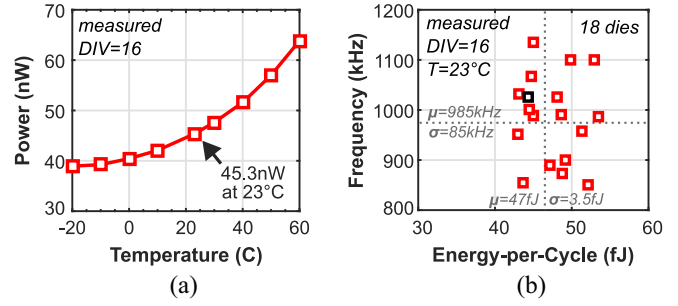


Fig. 6. (a) Measured power consumption versus temperature and (b) measured frequency and energy across 18 dies. Black marker shows the chip the rest of the measurements in this letter are taken from.

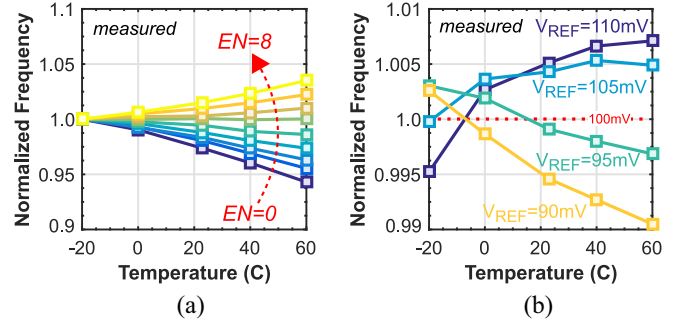


Fig. 7. (a) Output frequency deviation caused by adjusting R_N trim setting and (b) variation in V_{REF} .

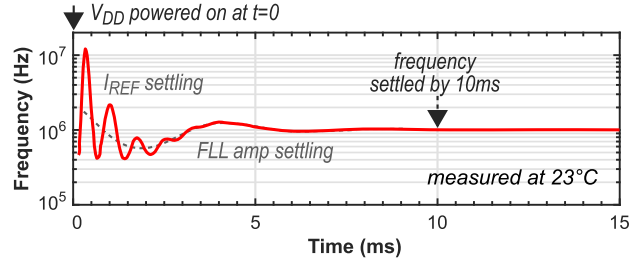


Fig. 8. Measured startup response of the FLL, showing a 10-ms settling time. Dashed line shows visualization of FLL amplifier settling without the added modulation from the I_{REF} startup.

power and an inversely proportional decrease in energy. A maximum frequency of 1.016 MHz is measured when $N = 16$ at a power consumption of 45.3 nW, yielding an energy efficiency of 44.6 fJ/cycle. The FLL can operate reliably up to this frequency from -20 °C to 60 °C while maintaining less than 50-ppm/°C temperature coefficient, reaching the peak stability of 20.3 ppm/°C at 1.016 MHz when $N = 16$. Fig. 5b shows the measured temperature stability versus output frequency, measured from -20 °C to 60 °C for each frequency point. Fig. 6(a) shows the power consumption of the FLL across temperature for $N = 16$, and Fig. 6(b) shows the measured frequency and energy-per-cycle across 18 dies. Fig. 7(a) shows the normalized output frequency versus temperature for each of the R_N trim settings, and Fig. 7(b) demonstrates the sensitivity of the output frequency to variation in V_{REF} across temperature, with less than 2% frequency variation across 20 mV of V_{REF} drift. Fig. 8 shows the measured startup response of the FLL for $N = 16$, demonstrating a 10-ms settling time. The startup behavior reveals the settling of the $V-I$ converter, which is stable within 5 ms, and the settling of the FLL loop amplifier, which takes another 5 ms to settle due to its low bandwidth. Note that [5] provides more theoretical detail on the frequency response based on a similar architecture.

TABLE I
PERFORMANCE SUMMARY AND STATE-OF-THE-ART COMPARISON

	This Work	JSSC '19 [9]	SSCL '18 [8]	JSSC '18 [7]	ISSCC '16 [6]	JSSC '16 [5]	CICC '15 [4]	JSSC '16 [3]	ISSCC '17 [2]	JSSC '15 [1]
Technology (nm)	65	65	40	180	180	180	180	65	65	180
Area (mm ²)	0.098	0.051	0.07	0.16	0.5	0.26	0.03	0.032	0.005	0.24
Operating Voltage (V)	0.6–0.8	1.0	0.65–0.8	1.0–1.8	0.85–1.4	1.2–1.8	0.6–1.8	1.0	0.9–2.0	1.2–2.2
Supply Sensitivity (%/V)	100	4.25	±0.6	0.44	0.48	0.75	6	<5	±0.49	1
Frequency (kHz)	1016	1050	417	32.7	3.0	70.4	122	18.6	1350	0.011
Temperature Range (°C)	-20–60	0–40	-20–80	-20–100	-25–85	-40–80	-20–100	-40–90	0–145	-10–90
Temperature Stability (ppm/°C)	20.3	2.5	106	13.2	13.8	34.3	327	85	96	45
Power (nW)	45.3	69000	181	35.4	4.7	110	14.4	130	920	5.8
Energy Efficiency (pJ/Cycle)	0.044	65.7	0.43	1.08	1.6	1.56	0.120	7.0	0.68	527.2

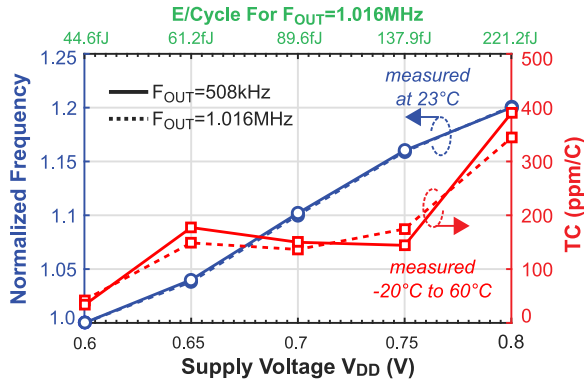


Fig. 9. Effect of supply voltage variation on output frequency, temperature stability, and energy-per-cycle.

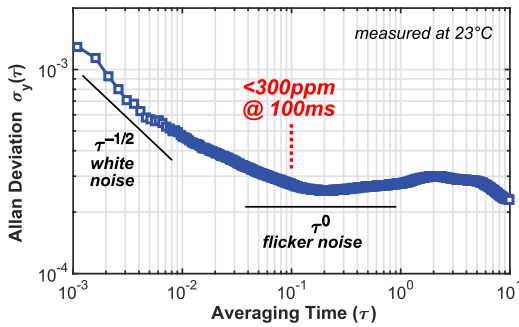


Fig. 10. Allan deviation measurement.

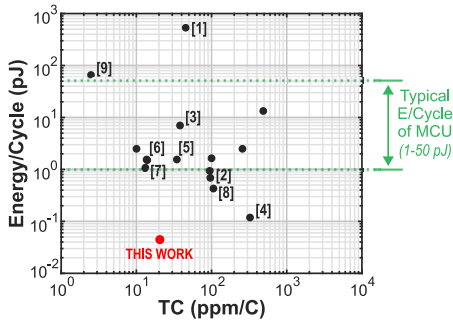


Fig. 11. Comparison of energy and temperature stability with state-of-the-art oscillators.

Fig. 9 shows the output frequency and temperature stability versus supply voltage, which both incur significant variation due to the subthreshold biasing of the FLL amplifiers (average of 111%/V frequency sensitivity across 18 dies). However, the FLL is designed

to operate from a regulated supply of 0.6 V, which is a typical supply voltage for subthreshold digital circuits targeting energy-efficient operation. Fig. 10 shows the Allan deviation of the FLL measured at room temperature, demonstrating a floor of 300 ppm after an averaging time of 100 ms. Table I summarizes the FLL performance, and Fig. 11 compares the energy efficiency and temperature stability of this letter with other state-of-the-art on-chip oscillators, showing an order of magnitude of energy reduction overworks with comparable temperature stability. To the best of our knowledge, this is the lowest energy-per-cycle for an on-chip oscillator, regardless of the architecture, operating frequency, or temperature stability.

IV. CONCLUSION

This letter presented an energy-optimized FLL architecture in 65-nm CMOS that achieves state-of-the-art energy-efficiency and high-temperature stability across a range of several hundred kHz. At 1.016 MHz, the FLL achieves 44.6-fJ/cycle and 20.3-ppm/°C temperature stability, marking over an order of magnitude of energy reduction compared to works with similar temperature coefficients.

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