

# A 0.5V 560kHz 18.8fJ/Cycle Ultra-Low Energy Oscillator in 65nm CMOS with 96.1ppm/°C Stability Using a Duty-Cycled Digital Frequency-Locked Loop

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## Abstract

This work presents an on-chip oscillator for energy-efficient IoT applications based on a duty-cycled digital frequency-locked loop (DFLL). The digital implementation allows low-voltage operation at 0.5V to reduce energy and enable voltage rail integration with low-energy digital logic, while the duty-cycled operation further improves energy efficiency to a record value of 18.8fJ/cycle (10.5nW @ 560kHz) while maintaining a high temperature stability of 96.1ppm/°C from 0°C to 100°C.

## Introduction

IoT systems require energy-efficient kHz-range clocking for functions such as data sampling, processing, and wakeup timing. This work demonstrates a fully integrated DFLL architecture that operates at ultra-low voltage and achieves a record level of energy efficiency while maintaining state-of-the-art temperature stability over a wide range. Existing on-chip architectures such as the frequency-locked loop (FLL) [1-4] and relaxation oscillator (RXO) [5,6] often suffer from poor energy efficiency since they target functionality across a wide range of analog supply voltages above 1V [3-6]. Recent works have improved on this by scaling down supply voltage [1,2], at which point the energy efficiency becomes limited by architecture. For FLLs, this limitation is due to either the dynamic power of the divider (at high output frequencies) or the power of the locking circuitry  $P_{\text{LOCK}}$  at low output frequencies (Fig. 1). The DFLL presented in this work overcomes both the existing voltage and architectural limitations on energy efficiency. First, we observe that IoT systems commonly include low-ripple voltage regulators in the 0.4V-0.6V range for low-energy digital circuits. So, the DFLL is designed to operate directly from a regulated 0.5V supply rail to save energy, facilitate integration with digital circuits, and eliminate the need to operate over a wide supply voltage range. Next, a timing controller is used to duty-cycle the frequency divider and locking circuitry to eliminate their dynamic power once the DFLL output frequency is settled, allowing it to run open-loop at significantly reduced energy regardless of the output frequency.

## Architecture

Fig. 2 shows an illustration of the DFLL during bootup, locking, and duty-cycling. The proposed DFLL (Fig. 3) generates a stable output frequency by locking a digitally-controllable oscillator (DCO) to a stable input reference voltage  $V_{\text{REF}}$ . Since the DFLL runs from a regulated 0.5V supply, a resistive divider can be used to easily obtain a stable  $V_{\text{REF}}$ . A  $V_{\text{REF}}$  of 0.2V is used for this design. To perform the lock, the DCO frequency is divided by an integer  $N$  and then transformed to a voltage  $V_{\text{CAP}}$  using a switched-capacitor frequency-to-voltage converter (FVC). The FVC uses a V-to-I reference current generator that uses  $V_{\text{REF}}$  in combination with a reference resistor  $R_{\text{REF}}$  (50.8M $\Omega$ ) to generate an  $I_{\text{REF}}$  of approximately 3.9nA with 0.6% variation from 0°C to 100°C (simulated). A comparator bank establishes a dead-zone (DZ) around  $V_{\text{REF}}$ , which is adjusted by tuning the offsets of the high (CMPH) and low-bound (CMPL) comparators. Fig. 4 shows the schematic and simulated offset tuning of the StrongARM-

based dynamic comparator. A SAR binary-search algorithm references CMPH and CMPL to adjust the DCO until  $V_{\text{CAP}}$  has settled inside the DZ, and then a linear search algorithm adjusts the DCO until  $V_{\text{CAP}}$  has settled at  $V_{\text{REF}}$ , which is indicated by a toggle on the zero-offset comparator (CMPM) output  $V_{\text{OM}}$ . The locking resolution is limited by the ripple on  $V_{\text{CAP}}$  (which is due to the FVC) that causes a theoretical worst-case error of 8kHz (143ppm/°C across temperature) when  $F_{\text{OUT}}=560\text{kHz}$ . Once the lock is complete, the DFLL is duty-cycled by freezing the DCO control word and disabling the loop divider. This breaks the feedback path so that the DFLL runs open-loop with its current frequency setting. During this time, the dynamic power of the divider and locking circuitry are eliminated, so the total energy consumption is reduced to only the dynamic power of the DCO core and leakage power of the locking circuitry. The open-loop operation causes the output frequency to be susceptible to temperature variation, so the DFLL periodically re-activates to re-lock the output frequency. An internal 160Hz leakage-based ring oscillator (Fig. 4) clocks the comparators and SAR/timing algorithm, which includes the duty-cycle timer. At the end of the duty-cycle interval (or upon bootup), the DFLL waits for  $V_{\text{CAP}}$  to settle using a bootup timer before beginning its evaluation. The re-locking process uses the linear search algorithm, which is quick and does not introduce large disruptions in the output frequency.

## Measurement Results

The DFLL was fabricated in a 65nm technology, occupying an area of 0.134mm<sup>2</sup>. Fig. 5 shows a measurement of the DFLL booting up, locking to a frequency of 560kHz (divider  $N=10$ ), duty-cycling, and waking up to re-lock. During the active locking operation, the DFLL consumes 23.7nW, which reduces to 10.4nW while duty-cycled. For a 99% duty-cycle (re-lock every 3 mins), this leads to an average of power of 10.5nW, yielding an energy-per-cycle of 18.8fJ at 20°C. Fig. 7 shows the performance measurements of the DFLL. The output frequency can be scaled over several hundred kHz by changing the divider value, which reduces average power down to 8.7nW at 55kHz (156fJ/cycle) when  $N=1$  (Fig 6). Across this output frequency range, the DFLL maintains a worst-case temperature stability of 180ppm/°C across 4 chips from 0°C to 100°C, limited by a combination of the locking resolution and variation of  $I_{\text{REF}}$ . An average stability of 96.1 ppm/°C is measured at 560kHz. The DFLL achieves an Allan deviation floor of 450ppm at 1ms, measured at 20°C. Fig. 7 shows the die micrograph and scatterplot comparison, and Fig. 8 shows a summary of the DFLL performance with full comparison to state-of-the-art low-power on-chip oscillators, demonstrating ultra-low voltage operation and a record-best energy efficiency.

## Acknowledgements

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## References

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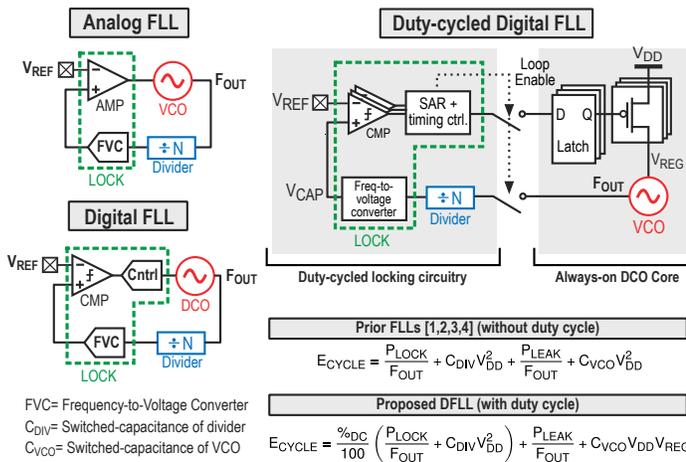


Fig. 1. Architectures of traditional FLLs and proposed DFLL design.

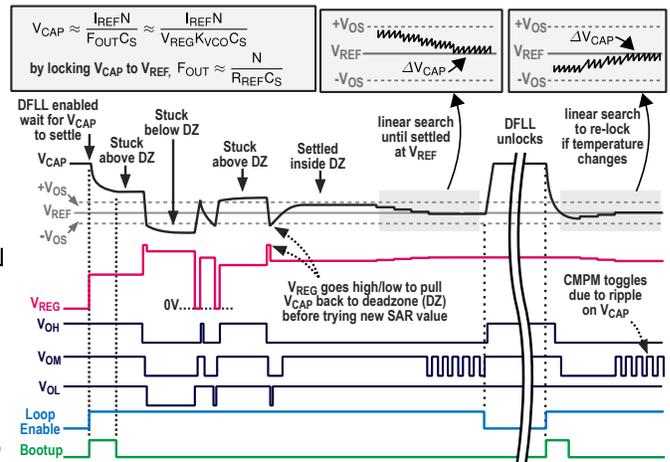


Fig. 2. Illustration of DFLL bootup, locking, and duty-cycling.

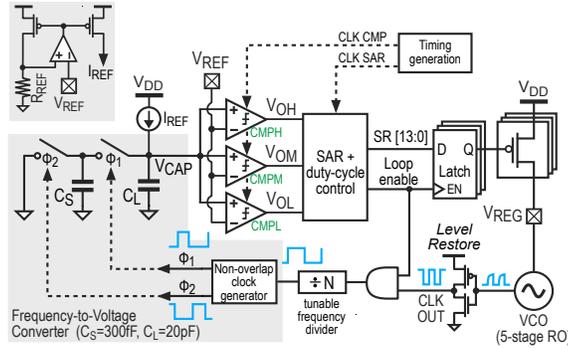


Fig. 3. Full schematic diagram of the DFLL, including V-I reference current generator and timing generation block.

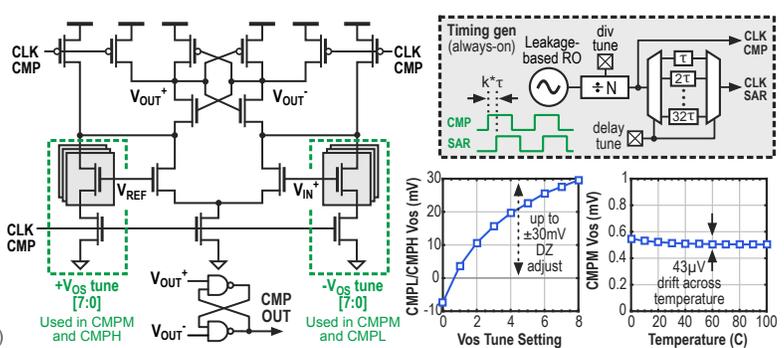


Fig. 4. Schematic of the dynamic comparator, timing generation circuit, and simulated values for comparator offset tuning and temperature drift.

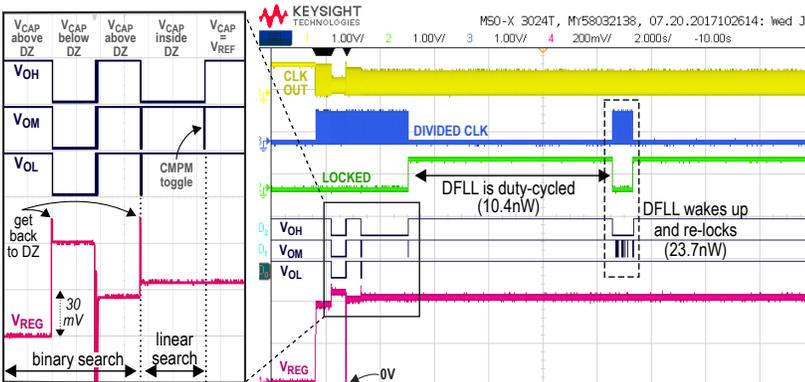


Fig. 5. Measurement of DFLL booting up, locking, duty cycling, and re-locking.

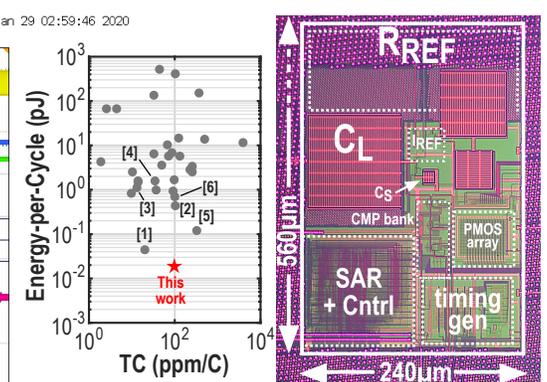


Fig. 7. Performance comparison and die micrograph.

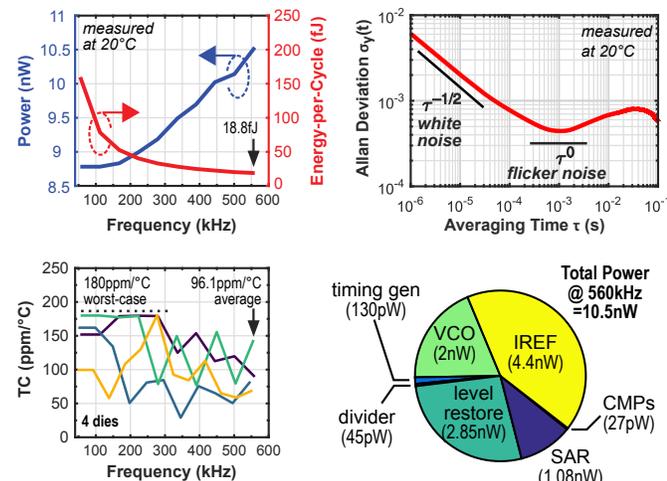


Fig. 6. Measured performance of the DFLL: power, energy, and TC versus output frequency, Allan deviation, and power breakdown.

	This Work	SSCL '19 [1]	SSCL '18 [2]	JSSC '18 [3]	JSSC '16 [4]	CICC '15 [5]	JSSC '19 [6]
Architecture	DC-DFLL	FLL	DFLL	FLL	FLL	RXO	RXO
Technology (nm)	65	65	40	180	180	180	65
Area (mm <sup>2</sup> )	0.134	0.098	0.07	0.16	0.26	0.03	0.005
Operating Voltage (V)	0.5	0.6–0.8	0.65–0.8	1.0–1.8	1.2–1.8	0.6–1.8	0.9–1.8
Frequency (kHz)	560	1016	417	32.7	70.4	122	1200
Temperature Range (°C)	0–100	-20–60	-20–80	-20–100	-40–80	-20–100	0–145
Temperature Stability (ppm/°C)	96.1	20.3	106	13.2	34.3	327	100
Power (nW)	10.5	45.3	181	35.4	110	14.4	820
Energy Efficiency (fJ/Cycle)	18.8	44.3	430	1080	1560	120	680

Fig. 8. Performance summary and comparison to state-of-the-art.