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A 0.5-V 560-kHz 18.8-fJ/Cycle On-Chip Oscillator With 96.1-ppm/°C Steady-State Stability Using a Duty-Cycled Digital Frequency-Locked Loop

Daniel S. Truesdell, *Member, IEEE*, Shuo Li, *Student Member, IEEE*, and Benton H. Calhoun, *Senior Member, IEEE*

***Abstract*— On-chip oscillators are popular clocking solutions for a wide range of circuits and systems due to their ease of integration and low form factor, but their energy efficiency is typically limited to the pJ/cycle range by a number of contributors, such as active biasing currents, frequency dividers, and comparators. This work presents an on-chip oscillator for energy-efficient Internet-of-Things (IoT) applications based on a duty-cycled digital frequency-locked loop (DFLL) that reduces energy by disabling energy-hungry components and only periodically reactivating them to keep the output frequency stabilized during temperature drifts. A test chip is implemented in 65-nm CMOS and achieves 18.8 fJ/cycle (10.5 nW at 560 kHz) while maintaining an average steady-state temperature stability of 96.1 ppm/°C from 0 °C to 100 °C.**

***Index Terms*— Clock, duty cycled, energy efficient, frequency-locked loop (FLL), low energy, oscillator.**

I. Introduction

FREQUENCY generation circuits are fundamental to the operation of many integrated components and systems. For example, radio transceivers require local oscillators (LOs), sensors, and analog front ends need sampling and chopping clocks, and digital blocks, such as processors and accelerators, depend on a clock signal to drive their synchronous logic. Depending on the application and performance targets of a component or system, the requirements of its clocking solution can vary widely and emphasize a number of metrics, such as temperature stability, noise stability, area, power/energy, and supply voltage stability. In some cases such as LO generation, off-chip quartz resonators are used as part of a crystal oscillator (XO) to deliver high-temperature stability and low noise. However, for many other components and sometimes even full systems, it is more desirable to avoid off-chip components to reduce form factor and simplify integration even at the cost of decreased performance when compared to an XO. This is often the case in system-on-chip (SoC) that integrates many components and their supporting circuits (references, passives, and so on) onto a single die and has become even more important recently with the emergence of a new subset of SoCs for the Internet of Things (IoT) that prioritize low form factor to the extent that they harvest their own energy from chip-scale solar cells to eliminate the added volume of an attached battery [1]–[3]. To maintain robust operation from harvested energy, these battery-less SoCs prioritize low-power and energy-efficient operation, which also extends to on-chip oscillators as a priority metric.

The perennial need for fully integrated frequency generation circuits has led to a proliferation of on-chip oscillator designs over many decades. Most common among these designs is the relaxation oscillator (RXO) [4]–[8], which traditionally generates an output frequency by integrating a reference current and using a comparator to detect when the accumulated charge crosses a threshold value. When implemented on chip, the reference current typically depends on a resistor R and the charge threshold depends on a capacitor C, leading the output period to be dependent on the RC time constant. A newly emerging architecture for on-chip frequency generation is based on the frequency-locked loop (FLL) that uses an amplifier to drive a voltage-controlled oscillator (VCO) to a frequency whose period is locked (via feedback to the amplifier) to an RC time constant [9]–[17].

In both architectures, energy efficiency is limited by a number of factors. Nominal supply voltages for on-chip oscillators are typically at analog-domain levels, such as 5 V in 1.2 μm [4] or 1.2–1.8 V in 180 nm [9], [10], and designs often emphasize the ability to operate across a wide range of supply voltages, which keeps dynamic power consumption high and results in energy efficiencies around 1–10 pJ/cycle. This issue has gained attention recently, and a number of designs have improved energy efficiency to sub-pJ/cycle by scaling down supply voltages to the near-/sub-threshold level [7], [11], [13]. Beyond voltage scaling, the energy is limited by architecture, as is the case in these reduced supply designs; RXOs are often limited by the dynamic power consumption of the comparator, whose switching frequency is equal to (or greater than) the output frequency of the RXO itself. Energy can be reduced by power gating the comparator within the output period, at which point the energy is limited by static dissipation of the biasing currents and RC network [6], [18].

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The authors are with the Department of Electrical and Computer Engineering, University of Virginia, Charlottesville, VA 22903 USA (e-mail: dst4b@virginia.edu).

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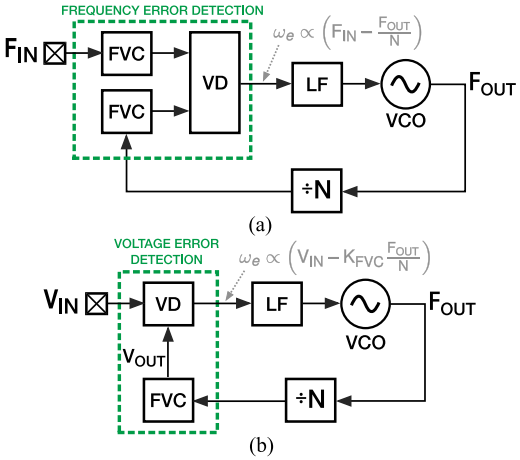

Fig. 1. Block diagram of (a) frequency synthesis using an FLL and (b) standalone frequency generation using an FLL.

FLLs replace the power-hungry comparator with an amplifier that can be biased at very low current [9], so their energy tends to be limited by either the static power of the biasing currents and locking circuitry or the dynamic power of the frequency divider, depending on the frequency the FLL is running at.

This work proposes an FLL-based on-chip oscillator (first presented in [17]) for energy-efficient IoT systems. The proposed design overcomes the existing energy limitations to achieve a high energy efficiency based on several key strategies. First, we note that energy-efficient IoT SoCs typically include integrated voltage regulators in the 0.4–0.6-V range for low-energy digital circuits. Designing the on-chip oscillator to operate directly from this type of low-voltage supply will reduce energy, facilitate integration with digital circuits, and eliminate the need to maintain stability over a wide range of supply voltages. Next, we propose a duty-cycled architecture that allows both the biasing/locking circuitry and the frequency divider to be periodically deactivated for energy reduction. Finally, we use a digital FLL (DFLL) implementation that better enables the first two techniques due to its robustness at low supply voltage and stability during the duty-cycled state. The results of these contributions are a state-of-the-art energy efficiency of 18.8 fJ/cycle without a significant sacrifice in intrinsic temperature stability (96.1 ppm/°C) compared with other on-chip oscillators. The remainder of this article is organized as follows. Section II introduces the background, operation, and performance limits of the traditional FLL architecture. Section III discusses the proposed duty-cycled DFLL implementation, and Section IV presents the measurements from a test chip fabricated in 65-nm CMOS. Then, Section V will summarize the performance and conclude this article.

II. DFLL Operation and Performance

Fig. 1(a) shows a block diagram of a generic FLL that takes an input frequency F_{IN} and synthesizes a new output frequency $F_{OUT} = N \times F_{IN}$ by using a frequency-to-voltage (FVC) converter and voltage detector (VD) to detect the frequency error between F_{IN} and the divided-down copy F_{OUT} [19]. For on-chip clock generation (where an F_{IN} does not exist), the traditional FLL architecture can be modified by replacing

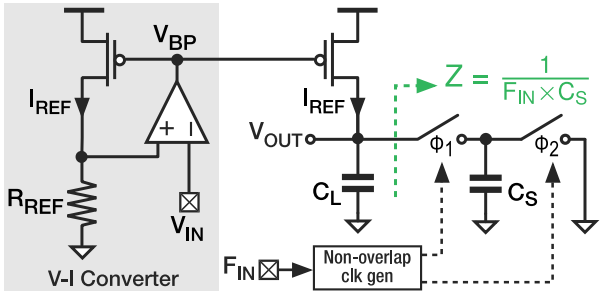

Fig. 2. Schematic of FVC with integrated V–I converter for I_{REF} generation.

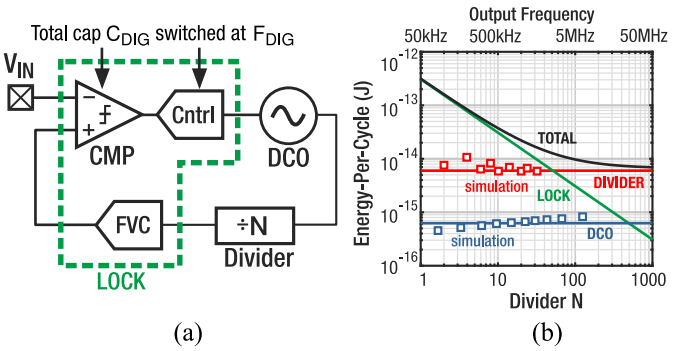

Fig. 3. (a) Block diagram and timing waveforms of a digital FLL and (b) energy per clock cycle versus divider value (proportional to output frequency) of the digital FLL at $V_{DD} = 0.5$ V. Solid lines show the model, and markers for divider and DVO/VCO are simulated values.

the input frequency and its accompanying FVC with an input voltage V_{IN} , as shown in Fig. 1(b) [12]. The FLL will then drive the VCO to a specific frequency whose reconstructed value (via the FVC) is equal and locked to V_{IN}. In this manner, the FLL behaves as a VCO, where F_{OUT} is dependent on a combination of V_{IN} and the transfer function of the FVC. However, as we will show next, the FVC and its transfer function can be designed to negate the dependence of V_{IN}, instead of replacing the dependence of F_{OUT} on an RC time constant by using a switched-capacitor-based design.

The FVC in an FLL is typically implemented using a voltage-to-current (V–I) converter, shown in Fig. 2, in combination with a reference resistor R_{REF} to transform V_{IN} into a reference current $I_{REF} = V_{IN}/R_{REF}$, which is injected into a switched-capacitor resistor C_S whose impedance can be represented as $Z = 1/(F_{IN} \times C_S)$ [9], [10], [12], [13], [16], [19]. Alternate FVC designs rely on bridge circuits [11], [14], [15]. The output V_{OUT} of the FVC can then be approximated by

$$V_{OUT} = \frac{I_{REF}}{F_{IN}C_S} = \frac{V_{IN}}{F_{IN}R_{REF}C_S} = \frac{NV_{IN}}{F_{OUT}R_{REF}C_S}. \quad (1)$$

Since the voltage error feedback of the FLL locks V_{OUT} to V_{IN}, we find that

$$F_{OUT} = \frac{N}{R_{REF}C_S}. \quad (2)$$

This simplified output frequency model will be used to calculate the energy efficiency of the FLL architecture. A more detailed model will derived later for analysis of the frequency inaccuracy.

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A. Energy Efficiency

An analysis of energy efficiency in an analog FLL implementation is given in [13], where a low-bandwidth amplifier serves as both the VD and low-pass filter of the FLL loop [9]. This section adopts a similar approach for a digital FLL, shown in Fig. 3(a), which replaces the amplifier with a comparator and digital controller that tunes a digital-controlled oscillator (DCO) instead of a VCO. The energy efficiency is easily modeled by breaking the FLL into three components: 1) the core oscillator (DCO); 2) the loop divider; and 3) the locking circuitry. The loop divider is implemented using a counter-based architecture with M bits whose power P_{DIV} can be approximated as

$$P_{\mathrm{DIV}} = F_{\mathrm{OUT}} C_{\mathrm{FF}} V_{\mathrm{DD}}^2 \sum_{i=0}^{M} \frac{1}{2^i} \approx F_{\mathrm{OUT}} 2 C_{\mathrm{FF}} V_{\mathrm{DD}}^2 \text{ for } M \gg 1 \quad (3)$$

where C_{FF} is the switched gate capacitance of a single flip-flop. Leakage power of the divider is neglected for simplicity. The DCO power is implemented with a five-state ring oscillator (RO) whose dynamic power is approximated as

$$P_{\mathrm{DCO}} = F_{\mathrm{OUT}} 5 C_{\mathrm{INV}} V_{\mathrm{DD}}^2. \quad (4)$$

The locking circuitry consists of the FVC, comparator, and digital controller. The FVC and its amplifier are biased with I_{REF}, so the total power is based on some multiple m of I_{REF}, leading to $P_{\mathrm{FVC}} = m I_{\mathrm{REF}} V_{\mathrm{DD}}$. The comparator and digital controller contain a total effective switched capacitance C_{DIG} that operates at an independent frequency $F_{\mathrm{DIG}} \ll F_{\mathrm{OUT}}$ that keeps their dynamic power low. Their leakage power P_{LEAK} can be modeled as $k I_{\mathrm{leak}} V_{\mathrm{DD}}$, where k is the number of transistors in the design and I_{leak} is the leakage current of a single transistor at V_{DD}

$$P_{\mathrm{LOCK}} = m I_{\mathrm{REF}} V_{\mathrm{DD}} + k I_{\mathrm{leak}} V_{\mathrm{DD}} + F_{\mathrm{DIG}} C_{\mathrm{DIG}} V_{\mathrm{DD}}^2. \quad (5)$$

Combining these terms and dividing by the ideal output frequency, the dependence of the total energy per cycle of the FLL on F_{OUT} is clearly reflected by (6). Since the power of the locking circuitry is independent of F_{OUT}, its energy contribution decreases inversely with F_{OUT} due to a lower integration time. The VCO and divider power consumption both scale proportionally with F_{OUT}, so their energy contributions are constant and follow the familiar CV^2 form:

$$E_{\mathrm{cycle}}(F_{\mathrm{OUT}}) = (2C_{\mathrm{FF}} + 5C_{\mathrm{INV}}) V_{\mathrm{DD}}^2 + \frac{P_{\mathrm{LOCK}}}{F_{\mathrm{OUT}}}. \quad (6)$$

The value of F_{OUT} is implicitly set by R_{REF} and C_{S} and then scaled by the integer divider value N, so we can update (6) to be a function of N

$$E_{\mathrm{cycle}}(N) = (2C_{\mathrm{FF}} + 5C_{\mathrm{INV}}) V_{\mathrm{DD}}^2 + \frac{C_S R_{\mathrm{REF}}}{N} \left(k I_{\mathrm{leak}} V_{\mathrm{DD}} + C_{\mathrm{DIG}} F_{\mathrm{DIG}} V_{\mathrm{DD}}^2 + \frac{m V_{\mathrm{DD}} V_{\mathrm{IN}}}{R_{\mathrm{REF}}} \right). \quad (7)$$

Fig. 3(b) shows the total energy per cycle versus divider N for a DFLL using (7) with $V_{\mathrm{DD}} = 0.5$ V, $C_{\mathrm{INV}} = 0.5$ fF, $C_{\mathrm{FF}} = 12$ fF, and a total locking power of approximately 18 nW, which is an optimistic approximation relative to values reported from recent designs, such as 95 nW in [9] (96% of total power), 29.4 nW in [10] (83% of total power), and 126nW in [11] (70% of total power). R_{REF} and C_{S} are sized such that $F_{\mathrm{OUT}} = 50$ kHz at $N = 1$. At low N (relatively low output frequencies), the static power contribution from the locking circuitry dominates the total energy. As N (frequency) is increased, the locking energy will eventually decrease enough that the divider begins to limit the total energy consumption instead. This frequency at which this transition occurs is particularly dependent on the supply voltage, the design of the locking circuitry, and the divider value. Designs with high bias currents or auxiliary amplifiers (large m), complex digital control algorithms (high k, C_{DIG}, or F_{DIG}), or no loop divider have relatively higher locking energy that tends to push total energy consumption to the pJ/cycle range. Decreasing V_{DD} will reduce energy but increase the relative contribution of the locking circuitry since its near-linear dependence on V_{DD} will be out-scaled by the quadratic dependence that the VCO/DCO and divider have. For example, in the current model at 0.5 V shown in Fig. 3(b), a divider value of $N = 53$ is required for the divider energy to overtake the locking energy. If V_{DD} is increased to 1.2 V, this transition occurs at $N = 20$ instead.

B. Steady-State Frequency Inaccuracy

The output frequency of the DFLL is subject to non-idealities and variation from several components. Temperature-dependent inaccuracy comes from variation in R_{REF} and the offset voltages of the amplifier in the V–I converter and the comparator in the VD. In addition, the FVC output voltage ripple ΔV_{OUT} limits the voltage error detection ability, which results in a finite steady-state (SS) frequency-locking error. Finally, the DCO gain and non-linearity can further deteriorate the locking resolution. We account for temperature-dependent inaccuracy by creating a new expression for F_{OUT} , which assumes that the voltage inputs to the amplifier and comparator are not equal

$$F_{\mathrm{OUT}} = \frac{N V_{\mathrm{IN,AMP}}}{R_{\mathrm{REF}} C_S V_{\mathrm{IN,CMP}}} \quad (8)$$

where $V_{\mathrm{IN,AMP}}$, and $V_{\mathrm{IN,CMP}}$ account for the different temperature-dependent offset voltages of the amplifier and comparator, respectively. All temperature dependencies are reflected by first-order models for simplicity

$$V_{\mathrm{IN,AMP}} = V_{\mathrm{IN0}}(1 + \alpha_{\mathrm{AMP}} \Delta T) \quad (9)$$

$$V_{\mathrm{IN,CMP}} = V_{\mathrm{IN0}}(1 + \alpha_{\mathrm{CMP}} \Delta T) \quad (10)$$

$$R_{\mathrm{REF}} = R_0(1 + \alpha_R \Delta T) \quad (11)$$

where the temperature coefficients (TCs) of the comparator (α_{CMP}), amplifier (α_{AMP}), and R_{REF} (α_R) are expressed in units of 1/°C, and ΔT is the deviation from a nominal temperature T_0. Temperature variation in V_{IN} can be accounted for in this model by adding the TC of V_{IN} to both α_{AMP} and α_{CMP}.

Fig. 4 shows how the FVC output voltage ripple ΔV_{OUT} leads to a voltage detection error that limits the SS frequency locking range. Given an initial FVC output value

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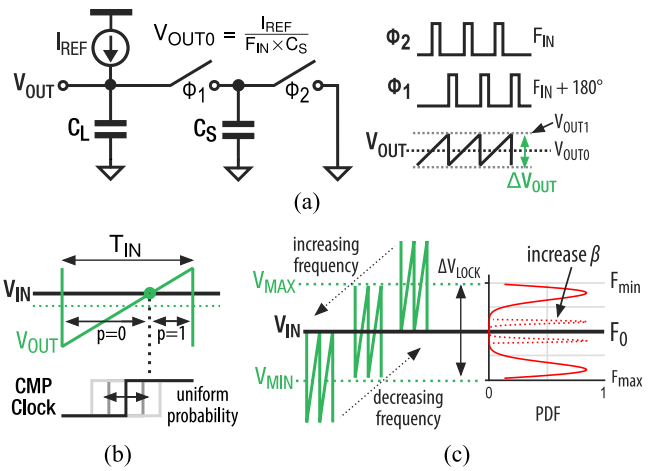

Fig. 4. (a) Simplified schematic and timing diagram of the FVC. (b) Illustration of locking probability during a decreasing frequency search. (c) Resulting voltage/frequency locking range.

V_{OUT1}, the output ripple ΔV_{OUT} can be expressed as V_{OUT1} $(C_S/(C_S + C_L))$, as shown in Fig. 4(a). In an analog FLL, the effect of the output ripple depends on the gain and bandwidth of the loop amplifier, which can filter it out. In the DFLL, the DCO frequency is adjusted (in either increasing or decreasing fashion, depending on the initial conditions) until a comparator toggle is detected, which indicates a successful lock due to V_{OUT} reaching V_{IN}. Ideally, $\Delta V_{OUT} \approx 0$ and the DCO has a fine resolution ($\Delta F_{DCO}/\text{LSB} \rightarrow 0$), so V_{OUT0} will exactly equal V_{IN} and the locking error will tend to 0. In reality, ΔV_{OUT} and the finite DCO resolution will cause the DFLL to lock to a range of voltages ΔV_{LOCK} whose corresponding frequencies ΔF_{LOCK} span above and below F_0. The voltage-locking range is represented by

$$\Delta V_{LOCK} = V_{IN,CMP} \times \frac{1+2\beta}{2\beta(1+\beta)} \approx \Delta V_{OUT}\Big|_{V_{OUT1}=V_{IN,CMP}} \quad (12)$$

where $\beta = C_L/C_S$ is the ratio of the capacitors used in the FVC. If the effects of temperature variation are ignored ($\Delta T = 0$), the (worst case) frequency inaccuracy contribution from ΔF_{LOCK} can be expressed as

$$\frac{\Delta F_{LOCK}}{F_0} = \pm\frac{1}{1+2\beta}. \quad (13)$$

Intuitively, (13) reflects that the frequency inaccuracy caused by the locking mechanism can be reduced by increasing the sizing of C_L relative to C_S, which reduces the output voltage ripple of the FVC. Locking inaccuracies of a few hundred ppm are possible by using a large β around 1000, but this can impose a large chip area for C_L. A solution for the increased area of C_L is to use some quantity N of FVC in parallel with multi-phase operation $(\phi_1, \phi_2, \ldots, \phi_{2N})$, which allows the capacitor sizes of both C_L and C_S to be reduced while maintaining a similar ΔV_{OUT} and effective FVC transfer function [20]. Practically, the frequency variation due to locking inaccuracy is lower than (13) since the final proximity of F_{OUT} to F_0 depends on the dynamic probability of the comparator toggling as V_{OUT} moves closer toward V_{IN} at each step of the locking process. An example is shown in Fig. 4(b) for a decreasing frequency search, where the probability of the DFLL detecting a lock is set by the percentage of time that V_{OUT} is above V_{IN} during one cycle of the F_{IN}. Assuming that $F_{DIG} \ll F_{OUT}/N$ and that its phase is uncorrelated with F_{OUT}, the probability of finding a lock (i.e., the comparator samples V_{OUT} when it is above V_{IN}) at a given frequency $F_{OUT} = f$ can be represented as a binomial experiment of n independent trials where n is the number of cycles of F_{DIG}

$$P(\text{lock}) = 1 - \left(\frac{fC_L R_{REF}}{N} - \frac{2\beta C_L}{C_S(1+2\beta)}\right)^n. \quad (14)$$

Then, if we consider a quantity Q of discrete and uniformly distributed frequencies $f = \{f_1, f_2, \ldots, f_Q\}$ obtainable from the DCO over the interval ΔF_{LOCK} (i.e., $\Delta F_{DCO}/\text{LSB} = f_i - f_{i-1}$), the probability of locking to a frequency f_i can be calculated as

$$P(F_{OUT} = f_i) = P(\text{lock})|_{f_i} \prod_{k=1}^{i-1}\left(1 - P(\text{lock})|_{f_k}\right). \quad (15)$$

An example of the resulting probability distribution is shown in Fig. 4(c). For a DFLL with a double-sided locking approach, the joint probability is bimodal due to the assumed equal possibility of a lock occurring from either side of V_{IN}. Increasing n or the DCO resolution will increase the likelihood that the DFLL will lock toward the boundaries of ΔV_{LOCK}, whereas increasing β toward infinity will eventually merge the two modes together to a single point at F_0 with a probability of 1. To ensure an accurate DFLL lock within the limits of (13), the DCO resolution should be high enough that V_{OUT} can be driven within ΔV_{LOCK}

$$\frac{\Delta F_{DCO}}{\text{LSB}} \leq 2|\Delta F_{LOCK}|. \quad (16)$$

This constraint can also be used to define the DCO accuracy requirements. Nonlinearity and non-monotonicity do not preclude a successful lock within ΔV_{lock}, but the differential nonlinearity (DNL) can cause V_{OUT} to jump completely across ΔV_{lock} (rather than settling within it) if its value $|\text{DNL}| \times (\Delta F_{DCO}/\text{LSB})$ violates the condition in (16).

Including the effects of temperature variation, the total SS output frequency inaccuracy can be expressed as a double-sided value

$$\frac{\Delta F_{OUT}}{F_0} = \pm\left(\frac{1+\alpha_{AMP}\Delta T}{(1+2\beta)(1+\alpha_{CMP}\Delta T)(1+\alpha_R\Delta T)} + \left|\frac{(\alpha_{CMP}-\alpha_{AMP}+\alpha_R)\Delta T + \alpha_{CMP}\alpha_R\Delta T^2}{(1+\alpha_{CMP}\Delta T)(1+\alpha_R\Delta T)}\right|\right). \quad (17)$$

Note that when $\Delta T = 0$, (17) becomes equal to (13). Fig. 5 shows how the frequency inaccuracy across $\Delta T = 100$ (converted to ppm by multiplying (17) by 1 000 000) is affected by the individual TCs of the amplifier, comparator, and reference resistor. The results for each component are obtained by sweeping its TC while holding the other TCs at 0. If the TC of any component can be decreased enough, the total frequency inaccuracy becomes limited by the locking inaccuracy in (13). When $\beta = 50$, this corresponds to

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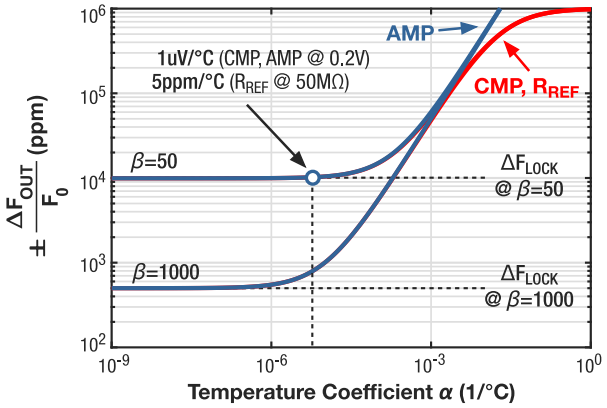

Fig. 5. Independent contributions of the amplifier, comparator, reference resistor, and locking circuitry to the total frequency inaccuracy of the DFLL, shown as a function of the TC of each component. A temperature range of 100 °C ($\Delta T = 50$) is used.

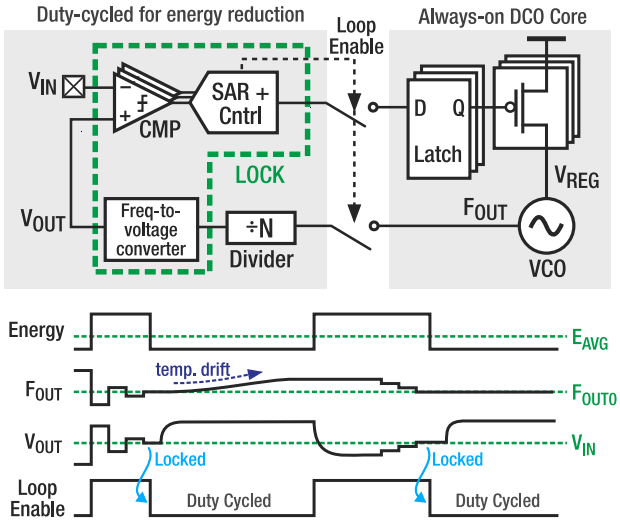

Fig. 6. Architecture and timing waveforms of the proposed duty-cycled DFLL.

a TC of approximately 10^{-5}, which translates into 5 ppm/°C for a 50-MΩ R_{REF}or an offset drift of 1 μV/°C with a 0.2-V V_{IN} for both the amplifier and the comparator. If the TCs are instead swept to infinity, the frequency inaccuracy will tend to infinity for α_{AMP} or 10^6 for α_{CMP} and α_R since they will eventually force F_{OUT} to 0 Hz.

III. Proposed Duty-Cycled DFLL

The proposed duty-cycled DFLL architecture, shown in Fig. 6, has two key mechanisms for reducing energy. First, the digital implementation improves the ability to operate robustly at low V_{DD} to take advantage of near-/sub-threshold digital supply voltage rails in the 0.4–0.6-V range that is commonly used in IoT SoCs for low-energy digital circuits. Designing the DFLL at $V_{\text{DD}} = 0.5$ V for compatibility with this regulated voltage domain will allow direct integration with low-energy digital circuits, reduce energy consumption, and eliminate the need for the DFLL to maintain stability over a wide range of supply voltages. Second, an integrated timing controller is used to duty cycle the divider and locking circuitry (shown by the "loop enable" signal) for some

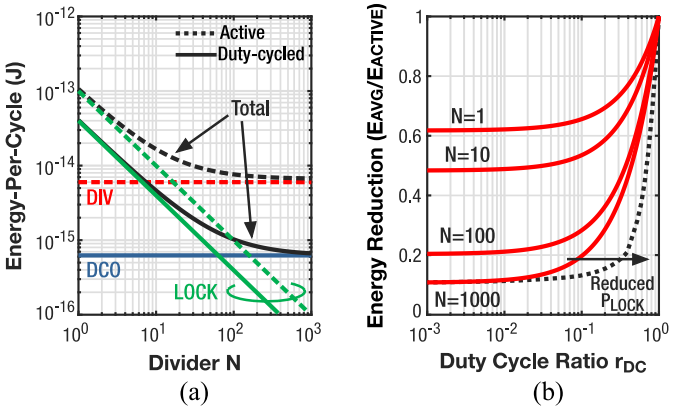

Fig. 7. (a) DFLL energy consumption during active and duty-cycled modes. DCO energy is the same for both active and duty-cycled modes, and the divider energy is only present in the active mode. (b) Total energy reduction [(18) divided by (7)] versus duty-cycle ratio, shown for different divider values.

duration t_{DC} once the frequency lock is complete. While duty-cycled, the DCO control word is frozen and the divider is disabled, which breaks the feedback path and lets the DFLL run open-loop, which leaves it susceptible to temperature variations based on the intrinsic temperature stability of the DCO. To compensate for temperature drift, the DFLL is periodically reactivated to re-lock the output frequency before returning back to the duty-cycle state. The duty-cycled divider energy can be neglected since its leakage power is very low relative to the power of other FLL components. Within the locking circuitry, the dc power consumption from bias currents [represented as mI_{REF} in (5)] will decrease since the impedance of the FVC tends to infinity when $F_{\text{IN}} = 0$, which effectively decreases m by 1. Further reduction could be achieved by power gating the remaining circuitry in the FVC, such as the V–I converter. The factor of reduction in m during the duty-cycled state is modeled as a parameter $\gamma_{\text{Iref}} = m_{\text{DC}}/m_{\text{nominal}}$. A similar effect occurs in the digital circuits (comparators and control block) since the duty-cycled state reduces their switching activity, which effectively decreases C_{DIG} by a factor γ_{dig}.

Fig. 7(a) shows the energy consumption of the same DFLL during active and duty-cycled operation. At low N, if the locking energy dominates, the amount of total energy reduction is limited by γ_{Iref} and γ_{dig}. However, if the energy of the locking circuitry is reduced by increasing N (or by reducing its power via reduced V_{DD}, C_{dig}, and so on), then the total energy can be reduced down to the power of the DCO. When a duty-cycled ratio $r_{\text{DC}} = t_{\text{on}}/(t_{\text{on}} + t_{\text{DC}})$ is used ($r_{\text{DC}} = 1$ is always active), the average energy per cycle of the DFLL can be expressed as

$$\begin{aligned} &E_{\text{cycle,AVG}}(N) \\ &= (r_{\text{DC}} 2C_{\text{FF}} + 5C_{\text{INV}})V_{\text{DD}}^2 \\ &\quad + \frac{C_S R_{\text{REF}}}{N}\Bigg(kI_{\text{leak}}V_{\text{DD}} + C_{\text{DIG}}F_{\text{DIG}}V_{\text{DD}}^2(\gamma_{\text{dig}} + r_{\text{DC}} - \gamma_{\text{dig}}r_{\text{DC}}) \\ &\qquad + \frac{mV_{\text{DD}}V_{\text{IN}}}{R_{\text{REF}}}(\gamma_{\text{Iref}} + r_{\text{DC}} - \gamma_{\text{Iref}}r_{\text{DC}})\Bigg). \end{aligned} \tag{18}$$

Fig. 7(b) shows how the average energy reduces with lower duty-cycled ratios. Note that the specific characteristics

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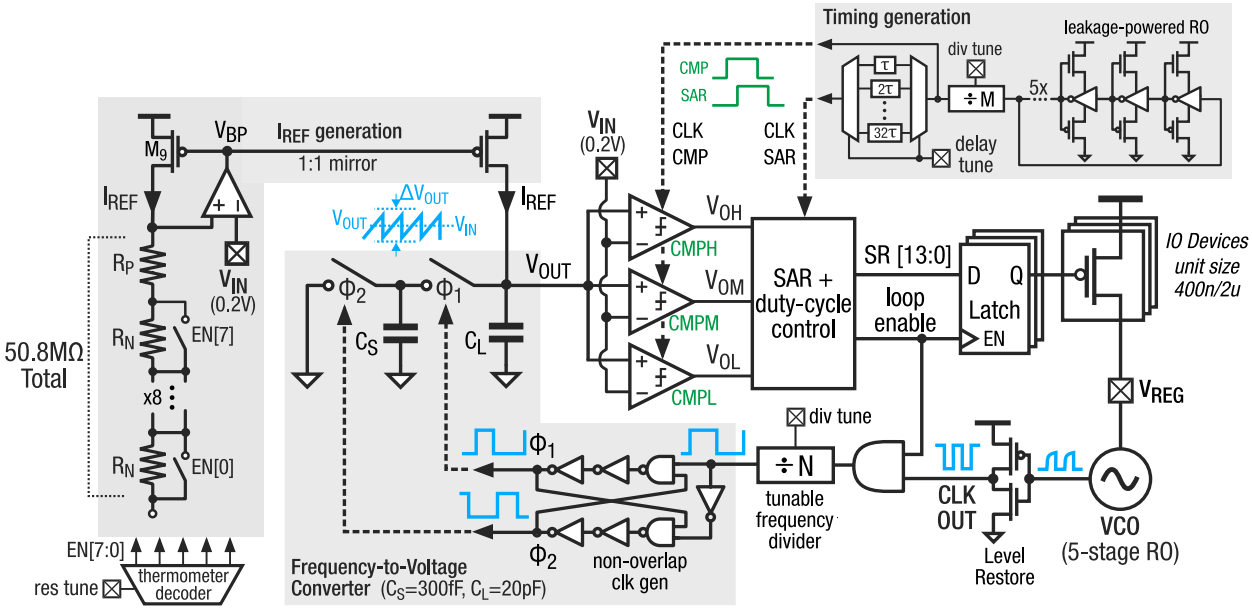

Fig. 8. Full schematic of the duty-cycled DFLL including I_{REF} generation circuit and always-ON digital timing generation block.

here are based on the relative energy of the locking circuitry in Fig. 7(a). If the locking energy is lower to begin with, the average energy will reach the same plateau at higher duty-cycle ratios (example shown by dashed line for $N = 1000$).

A. Implementation

Fig. 8 shows the full schematic of the proposed duty-cycled DFLL design, which targets a 0.5-V V_{DD} due to its popularity as a near-/sub-threshold supply voltage rail. The DCO is implemented using a tunable PMOS array that adjusts the supply voltage V_{REG} of a five-stage RO that is designed with minimum-sized devices for low energy (C_{INV}). The RO presents a very small load current, so the PMOS array uses long-channel thick-oxide devices. A skewed-sizing inverter restores the DCO output level to full swing. This level conversion approach does dissipate some short-circuit current, but also has less dynamic power than a more complex design with less short-circuit current. The level converter is switched at a high frequency, so the reduction in dynamic power is most preferable in this case. The FVC is implemented as shown in Fig. 2, with the exception that R_{REF} is broken into two different resistor types to compensate for its total TC α_R, which will be discussed later. C_L and C_S are 20 pF and 300 fF, respectively, yielding $\beta \approx 66$. Further decreasing C_S could yield a smaller β but can increase relative impacts of temperature-dependent parasitic capacitances [9]. An always-ON timing generation circuit uses a five-stage leakage-based RO and tunable frequency divider to generate F_{DIG}, which is delayed to create separate clocks for the comparators (CLK CMP) and digital control block [CLK successive-approximation register (SAR)]. The delay line simply ensures that the comparator outputs are valid at each clock cycle of the digital controller and is designed using different numbers of the same leakage-based inverters in series. To achieve both a fast initial lock and smooth subsequent re-locking, the digital algorithm replaces the single comparator approach used in existing DFLL designs (see [11] and [14]) with a bank of three comparators that enable a hybrid binary/linear searching algorithm that will be discussed next.

B. Locking and Re-Locking Behavior

The digital locking algorithm uses three comparators (CMPH, CMPM, and CMPL) to achieve a fast frequency lock by establishing a voltage deadzone (DZ) around V_{IN}. The middle comparator CMPM is designed to have a low offset to directly lock V_{IN} with V_{OUT}, whereas CMPH and CMPL are tuned for positive and negative offsets, respectively, to set the high and low bounds of the DZ. Upon bootup, an SAR binary search algorithm looks at the outputs of CMPH and CMPL and quickly adjusts the DCO control word (SR) until V_{OUT} is within the DZ, and then, a linear searching algorithm completes the locking process by adjusting the DCO one LSB at a time until it detects a toggle on the output of CMPM, indicating that V_{OUT} has reached V_{IN} (see the diagram in Fig. 4).

The frequency response of the FVC can be studied by treating its input as V_{IN} of the V–I converter while assuming that F_{IN} is constant

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{1/(R_{REF}F_{IN}C_S)}{1 + \frac{C_L}{C_S F_{IN}}s}. \tag{19}$$

Intuitively, (19) has a dc gain consistent with the result from (1) and single pole at $-C_S F_{IN}/C_L$ with a notable dependence on F_{IN}. Changes in F_{IN} during the binary searching algorithm (while V_{IN} is constant) are analogous to a step input on V_{IN} with a constant F_{IN} , which elicits a characteristic RC response. Therefore, to ensure that the FVC has time to settle after each bit trial, the algorithm's speed (F_{DIG}) should be in the passband of the FVC. Since the FVC cutoff frequency

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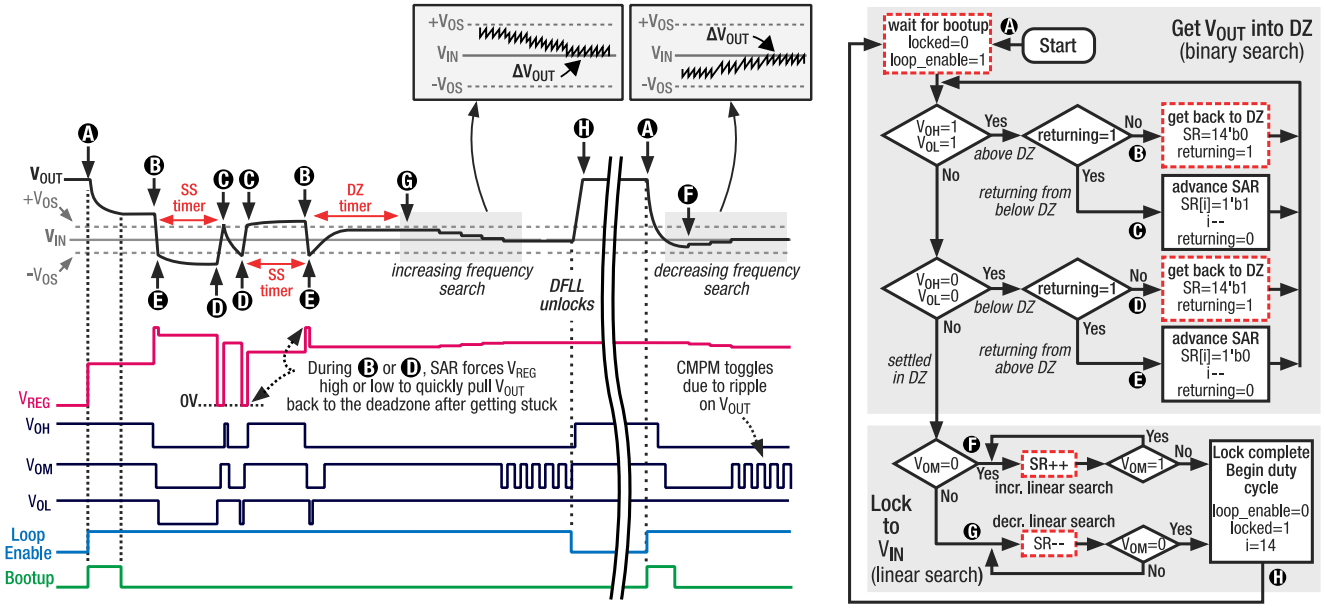

Fig. 9. Timing diagram of the DFLL booting up, locking, duty cycling, and waking up to re-lock. Diagram of locking and duty-cycling algorithm shown on right, where processes with dashed borders indicate that they only proceed after waiting for a timer.

has a dynamic dependence on F_{IN}, the locking algorithm uses several configurable timers to effectively adjust its response time based on its current stage, which is a proxy for the current range of F_{IN}.

A timing diagram and flowchart of the locking, re-locking, and duty-cycling processes are shown in Fig. 9. When the DFLL first boots up, it performs the first bit trial and waits on a bootup timer before using CMPH and CMPL to make the first decision (step A). After each bit trial of the binary search, an SS timer begins so that the FVC can settle. If V_{OUT} is outside the DZ ($V_{\text{OH}} = 1 \& V_{\text{OL}} = 1$ or $V_{\text{OH}} = 0 \& V_{\text{OL}} = 0$) when the SS timer expires, and this indicates that V_{OUT} is stuck outside the DZ and the algorithm responds by setting the DCO control to its maximum or minimum value to quickly return V_{OUT} to the DZ (steps B and D) before moving to the next bit trial (steps C and E). If V_{OUT} enters the DZ at any point, a DZ timer begins, which will trigger the linear searching algorithm if V_{OUT} has not left the DZ when the DZ timer expires. Depending on whether V_{OUT} is above or below V_{IN} when the linear searching algorithm begins (steps F and G), it will begin increasing or decreasing the DCO frequency, respectively, until it detects a toggle on the CMPM output. For each step in this phase, a linear-searching timer limits the number of times V_{OUT} is sampled by CMPM [represented by n in (14) before the algorithm increments or decrements the DCO frequency. Once the lock is complete, the DCO control word is frozen and the feedback loop is disabled so that V_{OUT} is unregulated and charges to V_{DD}, and a new duty-cycle timer starts to limit the duration of the duty-cycle interval to $t_{\text{DC}} = n_{\text{DC}} T_{\text{dig}}$, where n_{DC} is the counter threshold of the duty-cycle timer.

While duty-cycled, the temperature sensitivity and noise performance of the DFLL are based on the free-running DCO whose frequency increases exponentially with temperature but can be linearized at F_0 as

$$f_{\text{DCO}} = F_0 + \alpha_{\text{DCO}} \Delta T \tag{20}$$

where α_{DCO} is given in Hz/°C and is simulated to be around 15 000. Depending on the duty-cycle ratio and the rate of ambient temperature fluctuations, the open-loop DCO temperature sensitivity can contribute additional inaccuracy to the DFLL, which will be discussed shortly. When the DFLL wakes up to re-lock, the bootup timer allows the FVC to settle, whose output will have deviated from V_{IN} by some amount ΔV_{OUT0} based on how far the temperature has drifted since the last frequency lock

$$\Delta V_{\text{OUT0}} = \alpha_{\text{DCO}} \Delta T \left. \frac{\partial V_{\text{OUT}}}{\partial F_{\text{OUT}}} \right|_{F_{\text{OUT}}=F_0} \tag{21}$$

$$= \frac{-\alpha_{\text{DCO}} C_S R_0 \; V_{\text{IN}} \Delta T (1 + \alpha_{\text{AMP}} \Delta T)}{N(1 + \alpha_R \Delta T)} \approx 5 \text{ mV/C}. \tag{22}$$

This value plays a role in determining the amount of temperature drift that can be tolerated such that V_{OUT} will still be in the DZ when the DFLL wakes up to re-lock. Once the FVC has settled, the controller samples V_{OUT} from CMPM and then waits for the duration of the linear-searching timer for a CMPM toggle, which would indicate that V_{OUT} is still locked and no DCO adjustments are necessary. If a toggle is not detected, the linear searching process begins and can complete the re-locking process regardless of whether V_{OUT} is in the DZ or not. This approach allows the re-locking process to occur in the background without causing the large jumps or transitions in F_{OUT} as in the binary algorithm. If V_{OUT} is outside the DZ after bootup, the controller can optionally begin the binary searching algorithm instead.

The FVC output can be modeled in continuous time with the simple first-order difference equation

$$C_L \frac{dV_{\text{OUT}}(t)}{dt} + \frac{V_{\text{OUT}}(t)}{Z_{\text{FVC}}} = \frac{V_{\text{IN}}}{R_{\text{REF}}} \tag{23}$$

and the settling time t_{settle} of the FVC when waking up from the duty-cycled state can be solved with (23) knowing that the

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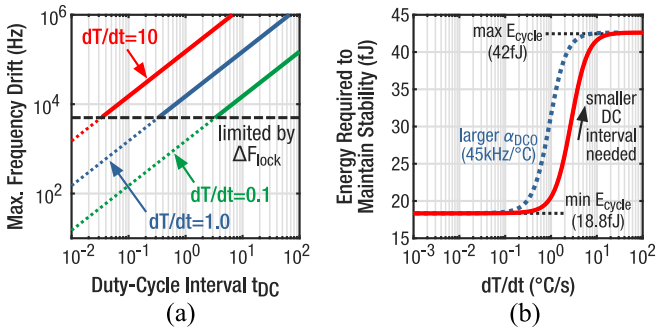

Fig. 10. (a) Modeled maximum open-loop frequency drift versus duty-cycle interval shown for temperature fluctuations of 0.1 °C/s, 1 °C/s, and 10 °C/s. (b) Average energy per cycle of the DFLL required (based on duty-cycle rate) to limit open-loop frequency drift to be within ΔF_{LOCK} versus the rate of ambient temperature drift.

initial value of V_{OUT} is V_{DD} and that V_{OUT} can be considered settled when it reaches the DZ

$$t_{\mathrm{settle}} = \frac{C_L}{C_S F_{\mathrm{IN}}} \ln\left(\frac{C_{\mathrm{SW}} F_{\mathrm{IN}} R_{\mathrm{REF}} V_{\mathrm{DD}} - V_{\mathrm{IN}}}{C_{\mathrm{SW}} F_{\mathrm{IN}} R_{\mathrm{REF}} (V_{\mathrm{IN}} + V_{\mathrm{os}}) - V_{\mathrm{IN}}}\right) \quad (24)$$

where V_{os} is the CMPH offset voltage and F_{IN} will be f_{DCO}/N which accounts for the temperature drift of the DCO frequency while duty-cycled. The overall temperature dependence of t_{settle} is low, and its value at $N = 10$ in the proposed implementation is around 5 ms. Once the FVC has settled, the linear search must complete the lock. The total re-locking time can then be approximated by

$$t_{\mathrm{relock}} = t_{\mathrm{settle}} + (n_{\mathrm{linear}} T_{\mathrm{dig}}) \frac{\alpha_{\mathrm{DCO}} \Delta T}{\Delta F_{\mathrm{DCO}}/\mathrm{LSB}} \quad (25)$$

where n_{linear} is the counter threshold used for the linear searching timer that corresponds to n used in (14). The temperature dependence of (25) is essentially linear and limited at $\Delta T = 0$ by t_{settle}. The time required by the linear searching algorithm to re-lock can be minimized by running as fast as possible within the limit of (24) due to the FVC settling time. Taking these factors together, typical locking and re-locking times on the order of several milliseconds can be expected.

C. Transient Frequency Inaccuracy

Short-term transient inaccuracy caused by frequency drift within a single duty-cycle interval can be evaluated with (20) by replacing ΔT with $\Delta T = dT/dt \times t_{\mathrm{DC}}$, where dT/dt is the instantaneous rate of temperature change expressed in °C/s and t_{DC} is the length of time spent in the duty-cycled state. Fig. 10(a) shows the resulting frequency drift versus duty-cycle interval for multiple rates of temperature change. In some cases, the frequency drift of the DCO will be lower than ΔF_{LOCK}, which will still limit the total frequency inaccuracy. To prevent transient frequency inaccuracy from exceeding ΔF_{LOCK}, the necessary t_{DC} can be computed for any dT/dt and combined with (25) to obtain the effective duty-cycle rate $r_{\mathrm{DC}} = t_{\mathrm{relock}}/(t_{\mathrm{relock}} + t_{\mathrm{DC}})$. Using the resulting r_{DC} with (7) and (18) yields the average energy per cycle of the DFLL required to maintain the intrinsic SS frequency inaccuracy by limiting the open-loop frequency drift. This result is shown in Fig. 10(b). For this DFLL design with $\alpha_{\mathrm{DCO}} = 15$ kHz/°C, low duty-cycle rates that minimize the average energy can be used until ambient temperature fluctuations exceed 1 °C/s, at which point faster duty-cycle intervals are required that will increase energy toward the fully active value. Variations that increase α_{DCO} will require shorter duty-cycle rates and therefore higher energy at lower rates of temperature change, as shown by the dashed line.

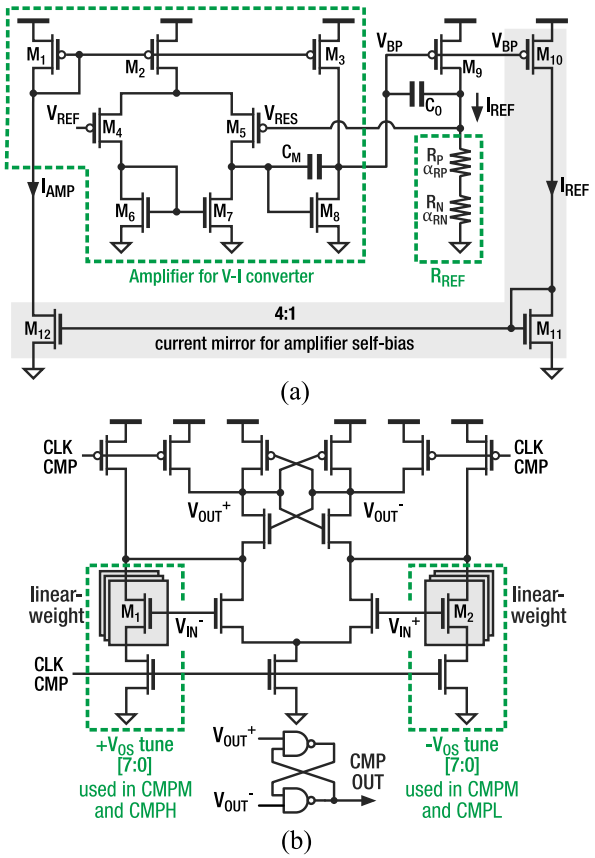

Fig. 11. Schematic of (a) V–I converter with self-biased amplifier and (b) clocked comparator based on a StrongArm latch with tunable offset.

D. Locking Circuitry and Temperature Compensation

Fig. 11(a) and (b) shows the schematics of the amplifier used in the V–I converter and the comparator design, respectively. The amplifier uses a two-stage topology that is self-biased with a copy of the reference current I_{REF} that it generates. The comparator is based on a StrongArm latch, where the offset voltage is tuned by adjusting the widths of the input pair which are implemented with 8-bit arrays of thermometer-coded minimum-sized devices. To achieve temperature compensation of the output frequency according to (17), the TCs of the amplifier offset and R_{REF} can be made equal to negate their opposite influence on the total inaccuracy. Assuming a low comparator offset drift, the frequency inaccuracy will then be limited by the locking inaccuracy.

Fig. 12 shows the simulated characteristics of the amplifier, R_{REF}, and the comparator. The amplifier experiences a positive offset drift near 1×10^{-4}/°C, so a slight positive TC near this value is needed from R_{REF}. This is accomplished by using two different resistor types in series with opposite TCs: R_P is

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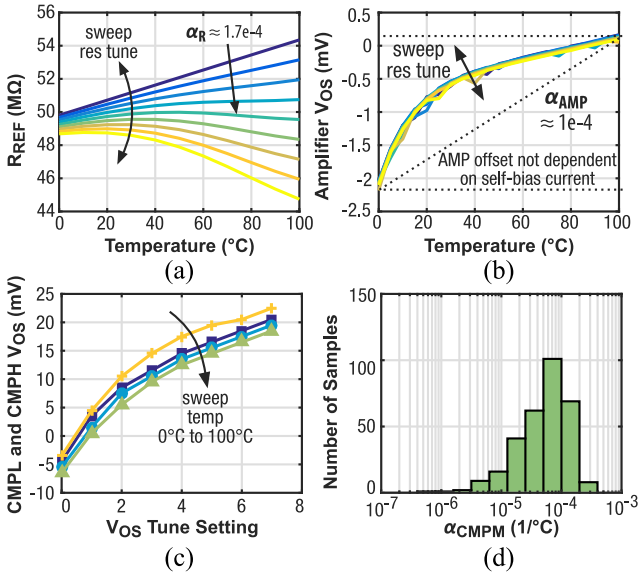

Fig. 12. (a) Simulated temperature sensitivity of the total reference resistance R_{REF} for different tuning values. (b) Temperature sensitivity of amplifier offset voltage shown for different R_{REF} tuning values. (c) CMPL and CMPH offset voltage tuning range across temperature. (d) 500-point Monte Carlo simulation of CMPM offset voltage TC.

a $P+$ diffusion resistor without salicide that has a positive TC, and R_N is a $P+$ poly resistor without salicide that has a negative TC. R_N is broken into eight thermometer-coded segments so that the overall TC of the full resistance can be tuned. Note that a high divider value is used or high energy efficiency [see (7)], which would yield MHz-range frequencies with typical on-chip resistance values in the $k\Omega$ to low-MΩ range. To keep the range of output frequencies of the DFLL at the desired kHz range, we compensate for the high N by making R_{REF} large, around 50 MΩ. The adverse effect of increasing resistor values is that temperature-dependent leakage of the R_N tuning switch becomes stronger relative to the I_{REF} that is being generated. The leakage increases exponentially with temperature, so it can be partially compensated by carefully selecting the relative sizes of R_P and R_N. The resulting tuning characteristic of R_{REF} enables a TC of 1.7×10^{-4}/°C, which is a reasonable match for the amplifier TC.

The offset tuning range for CMPL and CMPH allows a DZ width up to 20 mV, shown in Fig. 12(c), which varies across the temperature range by a maximum of around 4 mV. Note that that offset drift for these comparators will change the DZ width but not directly affect the total frequency inaccuracy of the DFLL, so the offset voltage only needs to be roughly tuned to create a reasonable DZ size. The offset drift of CMPM corresponds to α_{CMP} in the analysis from Section II, and the comparator tuning is applied symmetrically to minimize its temperature sensitivity. Fig. 12(c) shows the simulated TC of CMPM that on average is several times lower than the resistor and is low enough to render its inaccuracy contribution insignificant compared to the locking error (see Fig. 5). Based on these values, (17) predicts that across 100 °C, the DFLL will obtain a total inaccuracy of 111 ppm/°C. This value decreases to 34.7 ppm/°C if β is set to 1000, which aligns well with measured results from a similar analog FLL architecture

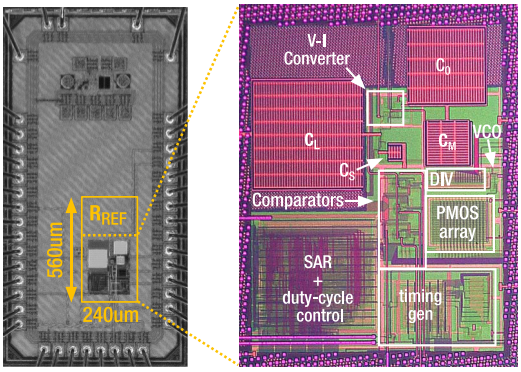

Fig. 13. Annotated chip micrograph of the proposed DFLL in 65-nm CMOS.

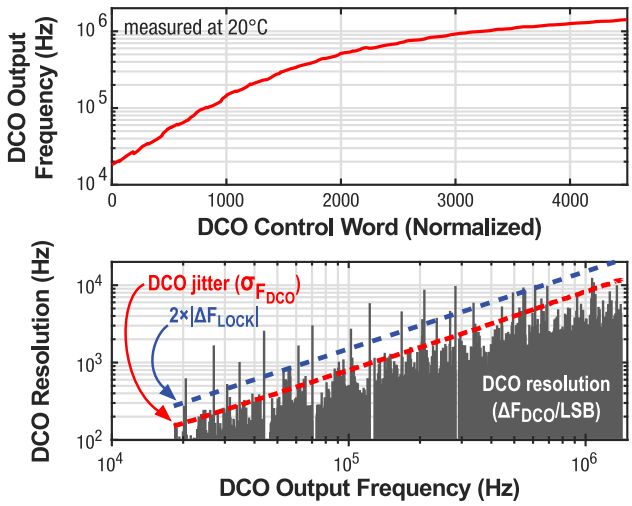

Fig. 14. Measured output frequency of the DCO across a range of 4500 tuning bit values (top) and instantaneous DCO tuning resolution (ΔF_{DCO}/LSB) versus output frequency (bottom). Dashed lines show both the measured DCO frequency jitter and theoretical calculation of locking error.

that does not suffer from a locking inaccuracy [13]. If all TCs are set to zero, the locking inaccuracy alone will lead to an overall TC of 81 ppm/°C.

IV. Measurements

The proposed duty-cycled DFLL was fabricated in a low-power 65 nm process, and Fig. 13 shows an annotated chip micrograph. The design occupies an area of 0.134 mm^2, of which roughly 60% is consumed by R_{REF}.

The performance of the DCO was individually assessed at room temperature by sweeping the control word (SR on the schematic in 8) across 4500 values. The DCO achieves a frequency tuning range of 18 kHz–1.38 MHz, which is shown in Fig. 14 along with the measured tuning resolution (ΔF_{DCO}/LSB) and measured frequency jitter ($\sigma_{F_{DCO}}$) of the DCO. The frequency range should yield an ideal DCO resolution of around 300 Hz/LSB, but the tuning approach of the DCO is inherently nonlinear, which causes ΔF_{DCO}/LSB to increase with the output frequency. With the exception of a few bit values, the DCO resolution is precise enough to allow a lock within the ΔF_{LOCK} inaccuracy limit given by (16), which is shown by a dashed line. The frequency jitter of the DCO was measured at each bit value by capturing 10 000 consecutive

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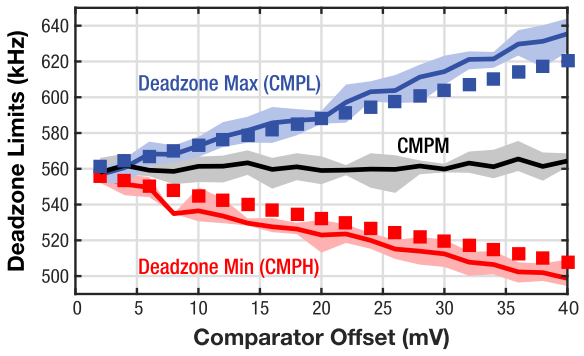

Fig. 15. Measured DZ size, expressed in terms of frequency, versus the absolute offset voltages of CMPL and CMPH. Shaded regions show the variation in DZ limits caused by the DCO frequency jitter, and square markers show the theoretical values based on (8).

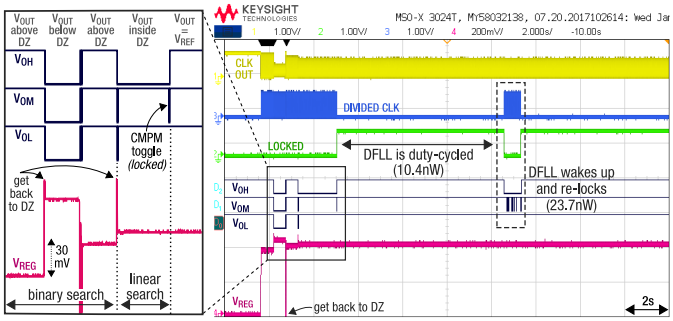

Fig. 16. Oscilloscope capture of the DFLL booting up, locking to the nominal frequency of 560 kHz, duty cycling, and waking up to re-lock.

single-period measurements from the DCO and is shown to increase linearly with the output frequency of the DCO.

Fig. 15 shows a measurement of how the DZ size changes with the offset tuning of CMPL and CMPH. This was performed by manually adjusting the comparator offsets and sweeping the DCO control word one bit at a time while measuring the outputs of the comparators. A combination of the DCO jitter and the finite probability of the comparator toggling due to the FVC output ripple ΔV_{OUT} (see Fig. 4) causes each of the comparators to toggle across a small range of frequencies that are shown by the shaded regions. The solid lines show the average values for each comparator, and the markers show the predicted DZ frequency limits based on (1).

An oscilloscope capture in Fig. 16 demonstrates the DFLL booting up, locking to the nominal frequency of 560 kHz ($N = 10$), duty cycling, and waking back up to re-lock. This waveform contains the output clock signal, the divided clock signal that is disabled during the duty cycle, the regulated DCO voltage V_{REG} that sets its frequency (V_{REG} is tuned by the PMOS array), a "locked" signal from the controller that indicates the status of the DFLL loop, and the outputs of the three comparators. The binary search is visible from both the V_{REG} signal as well as the comparator outputs, which indicate that V_{OUT} is either completely above or below the DZ for the first several bit trials. Eventually, V_{OUT} settles inside the DZ and a toggle on CMPM completes the lock. The nominal clock frequency F_{DIG} that clocks the controller and comparators is approximately 160 Hz; however, the DFLL was tested and functional with frequencies up to 10 kHz, which

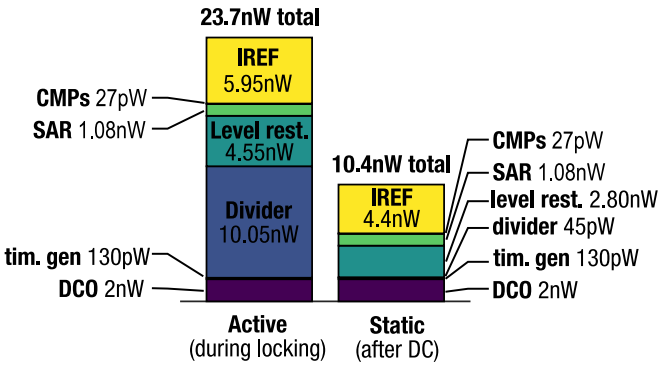

Fig. 17. Measured breakdown of power consumption in the DFLL during active and duty-cycled modes for $N = 10$ ($F_{\mathrm{OUT}} = 560$ kHz. $T = 20$ °C).

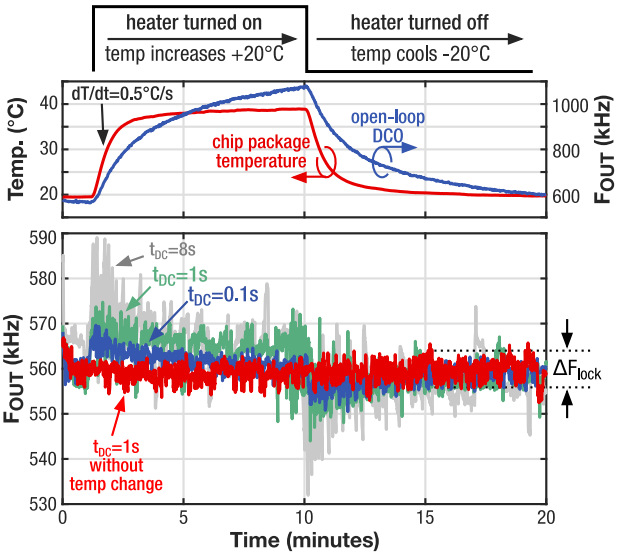

Fig. 18. Measured transient operation of the DFLL during a positive and negative 20 °C step in temperature, shown for duty-cycle rates of $t_{\mathrm{DC}} = 0.1$ s ($r_{\mathrm{DC}} = 0.36$), $t_{\mathrm{DC}} = 1$ s ($r_{\mathrm{DC}} = 0.06$), and $t_{\mathrm{DC}} = 8$ s ($r_{\mathrm{DC}} = 0.01$). For reference, the open-loop DCO response (with temp. change) and baseline closed-loop operation ($t_{\mathrm{DC}} = 1$ s without temp. change) are shown.

sets the upper bound on the allowable frequency drift of F_{DIG}. By tuning the counter values at each point in the DFLL loop, average bootup/locking times around 100 ms were obtained, and re-locking times were as short as 5 ms, which agrees well with (25).

The power breakdown of the DFLL in both the active and duty-cycled modes is shown in Fig. 17. As expected, the divider dominates the active power (the level restore circuit can be treated as an extension of the divider), followed by the locking circuitry (I_{REF}, CMPs, SAR, and timing gen), while the core DCO consumes 2 nW. Duty cycling the DFLL reduces power/energy by over 50%, from 23.7 to 10.4 nW, which is achieved primarily by eliminating the divider power. The power from the I_{REF} decreases as expected due to the FVC no longer dissipating power through C_S.

Fig. 18 shows the transient frequency inaccuracy of the DFLL when subjected to fluctuations in temperature. A heating element is attached to the chip package and cycled ON/OFF in 10-min periods that induce a ±20 °C fluctuation with a peak measured dT/dt of 0.5 °C/s. The DCO is immediately susceptible to the increasing temperature as shown by the

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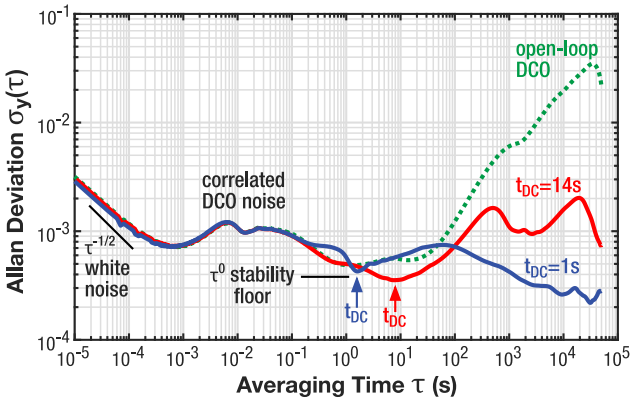

Fig. 19. Allan deviation measurement of the DFLL at $F_{OUT} = 560$ kHz ($N = 10$) in an indoor environment at room temperature (20 °C), shown for open-loop operation as well as duty-cycle intervals of 1 and 14 s.

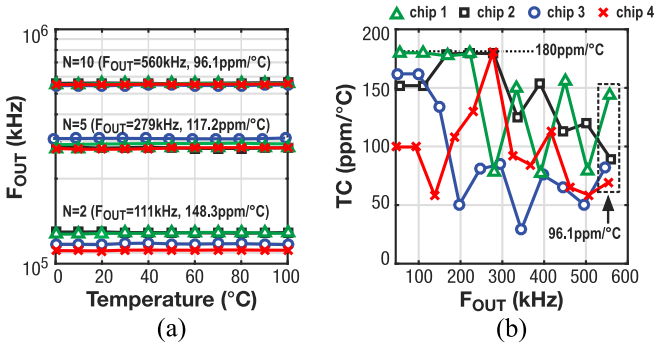

Fig. 20. Measured output frequency F_{OUT} versus temperature, shown for divider values $N = 2$, $N = 5$, and $N = 10$ on four dies (left) from 0 °C to 100 °C. TCs of the four measured dies are shown across the full range of output frequencies ($N = 1$ to $N = 10$) on the right.

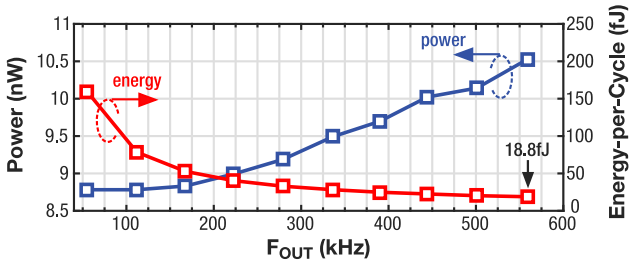

Fig. 21. Measured and power and energy consumption versus output frequency F_{OUT} measured at 20 °C.

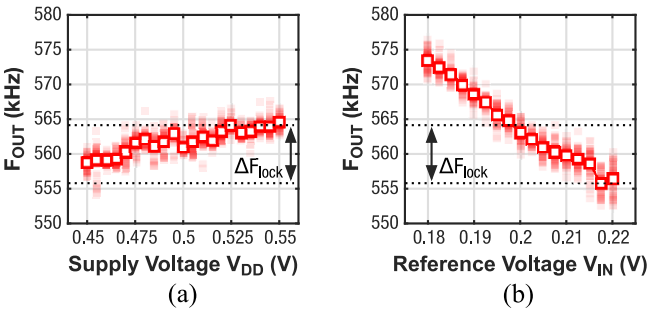

Fig. 22. (a) Measured supply voltage sensitivity for ±50 mV of deviation from the nominal supply voltage. (b) Reference voltage sensitivity for ±20 mV of deviation from the nominal reference voltage. Both measurements taken at 20 °C.

open-loop response, which increases up to 1.1 MHz. The transient closed-loop response during the same temperature change is shown for duty-cycle intervals of $t_{DC} = 0.1$ s, $t_{DC} = 1$ s, and $t_{DC} = 8$ s, which correspond with duty-cycle rates of $r_{DC} = 0.36$, $r_{DC} = 0.06$, and $r_{DC} = 0.01$, respectively, based on the measured t_{relock}. Shorter duty-cycle intervals reduce the amount of frequency drift within each duty-cycle interval that results in a lower transient inaccuracy that converges toward the SS inaccuracy defined by ΔF_{LOCK}. When the heater turns off and the chip package starts to cool, dT/dt becomes negative and the DCO frequency decreases and swings to the other side of the DZ, so the DFLL compensates during the re-locking process by increasing the DCO frequency back to the DZ. The discrepancy in F_{OUT} during the heating and cooling phases highlights the inaccuracy caused by ΔF_{LOCK}.

Frequency stability in the time domain is shown by the Allan deviation plot in Fig. 19, which was captured at room temperature over a 27-h long measurement period for duty-cycle intervals of $t_{DC} = 1$ s and $t_{DC} = 14$ s. For reference, the open-loop DCO is also shown. Correlated DCO noise limits stability at less than 1 s regardless of the duty-cycle interval, while longer term stability up to 12 h can be held to several hundred ppm by duty cycling to filter out temperature variation.

The DFLL was tested across a temperature range of 0 °C–100 °C in a Tenney Jr. environmental temperature testing chamber, and the output frequency was recorded at 10 °C increments after allowing the temperature to fully settle (no transient frequency inaccuracy). This process was repeated for divider N values ranging from 1 to 10 on four separate dies. Fig. 20(a) shows the measured frequency outputs of the four dies across the temperature range for divider values of $N = 2$, $N = 5$, and $N = 10$. The resulting SS TC for all possible divider values ($N = 1$ to $N = 10$) is shown in Fig. 20(b) and demonstrates full functionality across temperature from 55 to 560 kHz, with a worst case TC of 180 ppm/°C between all dies and divider values. This limit was separately observed in multiple dies and is likely due to a worst case combination of locking inaccuracy and TCs in the amplifier and R_{REF}. The average TC among all output frequencies is closer to the predicted value of 111 ppm/°C and is measured as 96.1 ppm/°C when $F_{OUT} = 560$ kHz. The power and energy consumption of the DFLL across the frequency range is shown in Fig. 21, with a 99% duty cycling being used. At low N, the locking power dominates, so the total power remains nearly constant, while energy changes inversely with increasing frequency. However, the DCO (and level restorer) becomes increasingly dominant as N is increased, causing a proportional increase in power that causes energy to plateau, where it reaches 18.8 fJ/cycle at $N = 10$, when $F_{OUT} = 560$ kHz. Without duty cycling, the total active energy at this point is approximately 42 fJ/cycle.

Fig. 22(a) shows the measured supply sensitivity of the DFLL across a ±50 mV range from the nominal value. The total variation across this range (1.1%) equates to a supply sensitivity of 11.01%/V. The models used in this article predict that the FLL architecture is theoretically robust to the input voltage V_{IN}, and prior works have shown that variations of ±10 mV have little effect on the output frequency across the

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR WORK

	This Work	VLSI '20 [14]	TCAS-I '20 [11]	JSSC '18 [15]	SSCL '19 [13]	JSSC '18 [10]	JSSC '16 [9]	CICC '15 [5]	JSSC '19 [6]	JSSC '18 [7]
Architecture	DC-DFLL	DFLL	DFLL	DFLL	FLL	FLL	FLL	RXO	RXO	RXO
Technology (nm)	65	40	40	180	65	180	180	180	65	180
Area (mm^2)	0.134	0.07	0.07	1.59	0.098	0.16	0.26	0.03	0.005	0.2
Operating Voltage (V)	0.45 – 0.55	1.0 – 1.4	0.65 – 0.8	1.7 – 2.0	0.6 – 0.8	1.0 – 1.8	1.2 – 1.8	0.6 – 1.8	0.9 – 2.0	0.4 – 0.65
Supply Sensitivity (%/V)	11.01	0.27	6.0	0.18	100	0.44	0.75	6.0	0.7	17.2
Frequency (kHz)	560	428	417	7000	1016	32.7	70.4	122	1350	1.22
Temperature Range (°C)	0 – 100	-40 – 80	-20 – 80	-45 – 85	-20 – 60	-20 – 100	-40 – 80	-20 – 100	0 – 145	-20 – 70
Trim Method	Resistor	Time-domain	Resistor	Resistor	Resistor	Resistor + Capacitor	Resistor	None	Resistor	Resistor
Number of Trim Points	1-point	13-point	1-point	2-point	2-point	2-point	2-point	N/A	1-point	2-point
Temperature Stability (ppm/°C)	96.1	8	135.3	2.5	20.3	13.2	34.3	327	100	94
Number of Samples	4	3	3	12	1	4	5	4	7	5
Power (nW)	10.5	380	181	775000	45.3	35.4	110	14.4	820	1.14
Energy Efficiency (fJ/Cycle)	18.8	900	430	110000	44.3	1080	1560	120	680	930

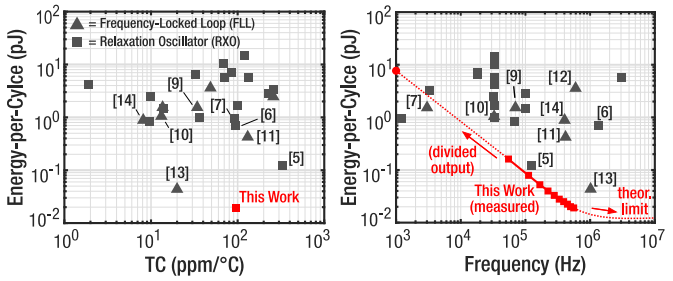

Fig. 23. Proposed DC-DFLL achieves the highest energy efficiency across a >100× frequency range. At even higher values of N, the theoretical DFLL energy floor is even lower.

temperature range [13]. We repeat this assessment at room temperature across a V_{IN} variation of ±20 mV for the DFLL by booting it up and letting it run for 50 consecutive duty-cycle intervals, measuring F_{OUT} at the end of each interval. The results, shown in Fig 22(b), demonstrate a small linear dependence of F_{OUT} on V_{IN}. Small variations within a 10-mV range have a negligible impact compared with the locking inaccuracy, which is modeled in (13) and shown in Fig. 18. For V_{IN} to remain in this range, a temperature stability of less than 475 ppm/°C is required, which can easily be achieved by a simple voltage reference design [21].

The performance summary of the duty-cycled digital FLL (DC-DFLL) and comparison with state-of-the-art on-chip oscillators is shown in Table I, and Fig. 23 shows an overview of the energy efficiency of on-chip oscillators across a wide frequency range. The DC-DFLL is the most energy-efficient architecture across the measured range (55–560 kHz), and if the output frequency is simply divided down (while keeping $N = 1$), the architecture remains the most energy efficient down to the near-Hz range, where design approaches shift to specifically target ultra-low static power consumption for wakeup timing needs [7], [22].

V. CONCLUSION

This article presented a DC-DFLL architecture that achieves high energy efficiency by mitigating the major sources of energy dissipation in traditional on-chip oscillators operating in the kHz range. We developed models for the energy efficiency and frequency stability of the DC-DFLL architecture, discussed the fundamental performance limits, and highlight design considerations for targeting low energy and high-temperature stability. Measurements from a test chip in 65-nm CMOS agree well with the modeled performance. The design achieves a state-of-art energy efficiency of 18.8 fJ/cycle at an output frequency of 560 kHz without sacrificing a large amount of temperature stability relative to other works at comparable frequencies.

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Daniel S. Truesdell (Member, IEEE) received the B.S. degree in electrical engineering from the University of Central Florida, Orlando, FL, USA, in 2016. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Virginia, Charlottesville, VA, USA.

His research interests include energy-efficient mixed-signal circuit design, on-chip oscillators and sensors, energy-harvesting and performance-scalable systems, and low-power digital circuit techniques.

Shuo Li (Student Member, IEEE) received the B.Eng. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2013, and the M.S. degree from Fudan University, Shanghai, China, in 2016, both in microelectronics. He is currently pursuing the Ph.D. degree in electrical engineering with the University of Virginia, Charlottesville, VA, USA.

His research interests include analog and mixed-signal integrated circuits and systems, energy harvesting and power management units, DC-DC converters, sensor interfaces, and system-on-chips for emerging Internet-of-Things applications.

Mr. Li was a recipient of the IEEE International Symposium on Circuits and Systems (ISCAS) Best Paper Award in 2020, and a winner of the IEEE SSCS 2019 International Student Circuit Contest.

Benton H. Calhoun (Senior Member, IEEE) received the B.S. degree in electrical engineering from the University of Virginia, Charlottesville, VA, USA, in 2000, and the M.S. degree and the Ph.D. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA, USA, in 2002 and 2006, respectively.

In January 2006, he joined the Department of Electrical and Computer Engineering, University of Virginia, where he is currently a Professor. His research has emphasized energy-efficient and sub-threshold circuit design for self-powered, batteryless wireless sensing systems. Starting from fundamental advances in sub-threshold circuits, he has expanded his work to include complete self-powered nodes for Internet-of-Things (IoT) and body-worn applications. He is the Campus Director and the Technical Thrust Leader of the NSF Nanosystems Engineering Research Center (ERC) for Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST). He co-founded and is the co-CTO at Everactive, Inc., Charlottesville, VA, USA, which is selling self-powered, energy-harvesting wireless sensing solutions in the industrial IoT market. He is a coauthor of *Sub-threshold Design for Ultra-Low-Power Systems* (Springer, 2006) and an author of *Design Principles for Digital CMOS Integrated Circuit Design* (NTS Press, 2012). He has over 200 peer-reviewed publications and 22 issued U.S. patents that contribute to the field of energy-efficient circuits and systems for self-powered and energy-constrained applications. His research interests include self-powered wireless sensors for the IoT, batteryless systems, body area sensor networks, low-power digital circuit design, system-on-chip architecture and circuits for energy-constrained applications, system-driven embedded hardware/software design, wakeup receivers, energy-harvesting-power management units, sub-threshold digital circuits, sub-threshold SRAM, energy-efficient communication, power harvesting and delivery circuits, low-power mixed-signal design, and medical applications for low-energy electronics.

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