15.1 A Self-Powered SoC with Distributed Cooperative Energy Harvesting and Multi-Chip Power Management for System-in-Fiber

Xinjian Liu¹, Daniel S. Truesdell¹, Omar Faruqe¹, Lalitha Parameswaran², Michael Rickley², Andrew Kopanski², Lauren Cantley², Austin Coon², Matthew Bernasconi², Tairan Wang², Benton H. Calhoun¹

¹University of Virginia, Charlottesville, VA ²MIT Lincoln Laboratory, Lexington, MA

Rapid reductions in power and size of SoC have paved the way for mm-scale textilebased self-powered systems capable of sensing a variety of biological and environmental data such as sodium, glucose, temperature, and neural signals [1,3-6]. SoCs built for these applications need to be fully autonomous and miniaturized, capable of continuous sensing at nW-level to operate from scarce amounts of harvested energy, and able to communicate in a distributed sensing network. A prior smart E-textile system [1] enables self-powered Na⁺ sensing but is built with cm-scale commercial-off-the-shelf (COTS) components that consume >4mW. A mm-scale system-in-fiber in [2] with COTS g components requires batteries for >10µW power. For systems using custom SoCs with nW power and mm-scale form factor [3-6], a base station is required to provide light (>3Klux [4], >60Klux [5]) to communicate and power the devices. This leads to reduced system autonomy and an inability for direct inter-SoC communication. We address these Elimitations with a fully autonomous self-powered system-on-chip (SoC) that can be distributed along a fiber strand, capable of simultaneously harvesting energy, cooperatively scaling performance, sharing power, and booting-up with other SoCs infiber. The SoC achieves 33nW power consumption for the whole chip under 92Lux light and can reduce control power down to 2.7nW for the energy harvesting and power management unit (EHPMU). With the proposed power sharing and cooperative dynamic voltage and frequency scaling (DVFS), the proposed SoC reduces the illuminance needed $\frac{1}{2}$ to stay alive by >7× down to 12Lux. We integrate the SoC into a 2.2×1mm cross-section $\stackrel{ ext{P}}{\rightarrow}$ polymer fiber with an embedded electrical bus via a 4.7×3.7mm interposer board, as Shown in Fig. 15.1.1 (bottom). The timing waveform in Fig. 15.1.1 (right) shows how the SoCs can cooperatively scale their performance based on both the local [7-9] and $\underset{=}{\text{H}}$ adjacent SoCs' conditions. This allows the energy and performance of all the in-fiber $\underset{=}{\text{H}}$ SoCs to be flexibly and jointly balanced, thereby improving the system viability and adaptability.

Figure 15.1.2 (left) shows the architecture of the proposed nanowatt system-in-fiber $\frac{1}{2}$ 8 (NanoSiF) and the SoC. The chip supports sustainable in-fiber operations by: 1) distributed energy harvesting: instead of powering the system from an aggregated energy source, the proposed architecture distributes SoCs along the fiber, which enables each SoC to harvest energy simultaneously and significantly relieves the dependence on $\overset{e}{\ominus}$ environment; 2) power sharing: the EHPMU harvests from a PV cell and provides four $\overset{e}{\ominus}$ outputs: $V_{\text{DIG}}(\sim 0.58V), V_{\text{LDO}}(0.95V), V_{\text{LOCAL}}(1-1.2V), and V_{\text{SHARE}}(1-1.2V).$ The V_{SHARE} rail is shared by all the SoCs in-fiber. The output of the 2^{md} stage (buck-boost) converter can be connected to either V_{LOCAL} or V_{SHARE} or both rails, which allows a flexible set of power $\frac{1}{2}$ management options, including a) sharing power with V_{SHARE} rail when the harvested $\overset{\infty}{B}$ energy is surplus; b) pulling power from V_{SHARE} rail when local energy is scarce; c) isolating V_{LOCAL} and V_{SHARE} rails to allow the SoC to act as an isolated power island if V_{SHARE} Bis collapsing. In this way, all the energy harvested along the fiber can be redistributed and reused, and local regions of the fiber can stay active even when other regions are without power; 3) ultra-low-power (ULP) digital core and sensor: for ULP sensing and processing, a digital core [7] comprising a dynamic-leakage-suppression (DLS) logic based SRAM and a scalable DLS RISC-V processor, along with a pW temperature sensor 5[10] are implemented; 4) ripple boot-up (RB): instead of programming each SoC َيْ individually [3-6], a power-gateable on-chip 492B flip-flop-based RB RAM (RBR) enables Eautonomous instruction memory programming via a RB procedure. Each SoC can ក្ខ customize the boot code provided to the next SoC along the fiber. Therefore, only one 2NVM is needed for all the SoCs in-fiber, achieving a minimal number of discrete components; 5) cooperative DVFS: with the proposed RBR, an SoC can read the energy ± conditions of adjacent SoCs and perform DVFS accordingly to share more power with SoCs in poor conditions, allowing the entire fiber system to remain operational. Figure 15.1.2 (bottom-right) shows the flow chart for the cooperative DVFS.

Figure 15.1.3 shows the architecture and block diagram of the proposed EHPMU. Prior designs suffer from cascade efficiency loss [11], demand off-chip maximum power point tracking (MPPT) and an excessive number of converters [12], or do not have cold start circuits for deployability [13]. Our two-stage topology directly powers the load components with minimum stages of converters, which avoids cascade loss [11]. The sub-nW power-gateable two-dimensional MPPT [7], including a fractional-open-circuitvoltage based pulse frequency modulation (PFM) and a conversion ratio modulation

(CRM), maximizes the energy extracted from the PV cell. And at low V_{PV} , the MPPT is automatically power gated with retention cells to improve the efficiency in poor

conditions. To achieve low area and ULP, the 2nd stage converter is only triggered when V_{DIG} is above V_{REFH} or below V_{REFL} A local asynchronous loop is then activated to overclock the 2nd stage converter and the mode controller to quickly regulate the V_{DIG} rail back to V_{REFM}. Compared to previous work, where the extra harvested power is discarded [7] or a 10MHz high-frequency clock is needed [13], this design shares the surplus energy with other SoCs without any extra high-frequency clocks. The sharing controller keeps monitoring the V_{LOCAL} and V_{SHARE} rails to decide 2^{nd} stage EHPMU output connection. To avoid sinking the V_{SHARE} rail before the chip cold starts, a back-to-back switch is implemented with a default-output-high level shifter to isolate the V_{SHARE} and V_{LOCAL} rails, as shown in Fig. 15.1.3 (top-right). Combining all these techniques, the EHPMU achieves a 2.7nW minimum control power, >60% peak efficiency for each stage, and full autonomy with a 0.516mm² area. The RBR includes two SPI slaves and a 492B register. The SPI slave enters NVM mode once it receives a specific command to imitate the COTS NVM, allowing SoCs to boot-up from either an NVM or RBR. The fiber integration process is shown in Fig. 15.1.3 (bottom-right). The polymer fiber is thermally drawn from a Polyetherimide (PEI) perform with six embedded copper wires. The integration technique includes: 1) the top layer of the PEI material is removed to create pockets and expose the copper wires; 2) the wires are cut in the middle; 3) the SoC is wire-bonded onto an interposer which is then soldered onto the exposed wires, followed by encapsulation with UV-cure epoxy.

The SoC is fabricated in 65nm CMOS. A benchtop testing setup is shown in Fig. 15.1.4 (top), where two SoCs are connected over V_{SHARE} and SPI ports. The measured waveform shows that the SoCs can share power with each other and isolate V_{LOCAL} from the V_{SHARE} rail when it droops. The measured ripple boot-up waveform (Fig. 15.1.4 bottom) shows that SoC1 can cold start, boot-up from the NVM, and execute the program to turn on its RBR, followed by SoC2 booting-up from SoC1. The measured cooperative DVFS waveform shows that once SoC1 gets into a dark condition, it changes its RBR value to indicate a help request. SoC2 keeps reading SoC1's RBR value, and when it detects the request, it scales itself down to share more power with the V_{SHARF} rail. Figure 15.1.5 shows the measured efficiency for the EHPMU across V_{PV} and P_{OUT} . The EHPMU achieves a 62.7%, 74.8%, 72.6% peak efficiency for the boost converter and buck-boost converter in boost and buck mode, respectively, with a 2.7nW minimum control power. The system power breakdown for the full chip is measured (Fig. 15.1.5 bottom-left) at its poorest harvesting point. The measured minimum voltage/Lux required to keep an SoC alive is 180mV/90Lux (across 11 dies). When adjacent SoCs can share 50nW power with V_{SHARF} rail, the required Lux for an SoC to stay alive can be decreased by >7×.

Figure 15.1.6 presents the comparison with the state-of-the-art fiber systems and microsystems. The SoC achieves 33nW full chip power from the harvesting input and can maintain continuous sensing under the poorest of lighting conditions. With the EHPMU, the SoC achieves distributed energy harvesting and multi-chip power sharing, enabling an SoC to survive in a $>7 \times$ darker environment. Thanks to the proposed ripple boot-up function, the SoCs in-fiber can boot-up and communicate with each other, which is not supported by previous work. Figure 15.1.7 shows the die micrograph of the SoC and comparison with state-of-the-art switched capacitor based multi-output EHPMU. The proposed EHPMU achieves the lowest control power of 2.7nW with high efficiency and a small area of 0.516mm². With a 2.2×1mm² cross-section fiber, the SoC is shown to be fully compatible with the post-draw integration technique for fiber integration. All these results and features make this SoC well-suited for ULP SiF applications.

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References:

[1] L. Yin et al., "A Self-Sustainable Wearable Multi-Modular E-Textile Bioenergy Microgrid System," *Nature Comm.*, vol 12, no. 1542, Mar. 2021.

[2] G. Loke et al., "Digital Electronics in Fibres Enable Fabric-Based Machine-Learning Inference," *Nature Comm.*, vol 12, no. 3317, June 2021.

[3] S. O'Driscoll et al., "A 200µm × 200µm × 100µm, 63nW, 2.4GHz Injectable Fully-Monolithic Wireless Bio-Sensing System," *IEEE RFIC*, pp. 256-259, June 2017.

[4] X. Wu et al., "A 0.04mm³ 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement," *IEEE Symp. VLSI Circuits*, pp. 191-192, June 2018.

[5] L. Xu et al., "A 210 × 340 × 50 μ m Integrated CMOS System for Micro-Robots with Energy Harvesting, Sensing, Processing, Communication and Actuation," *ISSCC*, pp. 194-195, Feb. 2022.

[6] J. Lim et al., "A Light-Tolerant Wireless Neural Recording IC for Motor Prediction with Near-Infrared-Based Power and Data Telemetry," *IEEE JSSC*, vol. 57, no. 4, pp. 1061-1074, April 2022.

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Figure 15.1.1: The proposed NanoSiF with distributed cooperative energy harvesting cooperative DVFS (bottom-right).





power sharing, and ripple boot-up (top); comparison of the state-of-the-art vs. the Figure 15.1.2: Architecture of the proposed NanoSiF and system block diagram of proposed NanoSiF (bottom-left); principle of the proposed power sharing and the proposed SoC (left); power sharing control scheme (right-top); flow chart of the cooperative DVFS control algorithm (right-bottom).



Figure 15.1.3: Block diagram of the EHPMU (top), ripple boot-up, and asynchronous Figure 15.1.4: Testing setups (top-left); measured power sharing waveforms (topcommunication (bottom-left); buck-boost mode control, back-to-back switch, and right); measured ripple boot-up waveform (top-left); measured local DVFS and cooperative DVFS waveform (top-right). fiber integration (bottom-right).



Figure 15.1.5: Measured EHPMU efficiency across V_{PV} and output power (top); measured full chip power breakdown at 0.183V V_{PV} under 92Lux light, 1.2Hz, 0.5V V_{CN}, 0.1V_{CP} (bottom-left); measured minimal voltage/Lux for the SoC to cold startup Figure 15.1.6: Comparison of the NanoSiF SoC with prior self-powered miniaturized and stay alive with/without power sharing (bottom-right).

	[1] Nature Commu.'21	[3] RFIC`17	[4] VLSI'18	[5] ISSCC`22	[6] JSSC'22	This Work
Technology	N/R	65nm	55nm DDC	55nm triple-well	180nm	65nm
Sensor	Na [*] Concentration	Glucose Concentration	Temperature	Temperature + Electric Field	Neural Recording	Temperature
Processor and Memory	ATtiny441**	No	Arm Cortex M0+ +4Kb SRAM	MCU+480b Mem.	No	RISCV+6KB SRAM
Self-Powered	Yes, TEG/BFC	Yes, PV	Yes, PV	Yes, PV	Yes, PV	Yes, PV
Distributed Energy Harvesting	No	No	No	No	No	Yes
Power Sharing	No	No	No	No	No	Yes
Cold Startup	Yes	Yes	Yes	Yes	Yes	Yes
Boot-up Function	No, preprogram	No	Yes	Yes	No	Yes, Ripple Boot-up
Communication	Yes	Yes, RF/Optical	Yes, Optical	Yes, Optical/Move	Yes, Optical	Yes, Wireline
Cooperative DVFS	No	No	No	No	No	Yes
Minimal System Power	4mW@2V	63nW	16nW	75nW@60Klux	570nW (38°C)	33nW@0.183V V _{PV} (92Lux)
Components included in System Power	MCU** +PMU**+sensor+ ECD+IO	CLK+Current Reference+PMU	MCU+SRAM+ ROM+CLK+PMU+ sensor+TRx	MCU+SRAM+ROM +Sensor+CLK+Rx	AFE+Rx+CLK+ Bias	Full Chip: Sensor+MCU+ SRAM+ROM+CLK+EHPMU +ESD+IO+V _{CN} ,V _{CP} Gen.
PMU Topology	Inductor	SC	SC	No, EH only	No, EH only	SC+LDO
PMU Peak Efficiency (%)	N/R	46%@100nA I _{load}	N/R	N/R	N/R	62.7%@1st stage 74.8%@2nd stage-Boost 72.6%@2nd stage-Buck
System Integration	E-texile with films	TSV to back side of IC	Stacked with bond wire	Monolithic Fabricated Robot	Stacked with flip chip	Embedded in fiber with interposer and bond wires
Device Size	>1cm ³ *	200x200x100µm	360x400x280µm	210×340×50µm	190x280µm	4.7×3.7mm interposer on a 2.2×1mm cross-section fiber
Minimal V _{IN} /Lux for system survival	0.33V	N/R	3Klux	60Klux	N/R	180mV(90Lux)@Single SoC 145mV(12Lux)@Power Share

*Calculated from the paper **Commercial off-the-shelf products

SiF and microsystems.

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Additional References:

[7] D. Truesdell et al., "NanoWattch: A Self-Powered 3-nW RISC-V SoC Operable from 160mV Photovoltaic Input with Integrated Temperature Sensing and Adaptive Performance Scaling," *IEEE Symp. VLSI Circuits*, pp. 210-211, June 2022.

[8] X. Liu et al., "A 194nW Energy-Performance-Aware IoT SoC Employing a 5.2nW 92.6% Peak Efficiency Power Management Unit for System Performance Scaling, Fast DVFS and Energy Minimization," *ISSCC*, pp. 224-225, Feb. 2022.

[9] L. Lin et al., "Sub-nW Microcontroller With Dual-Mode Logic and Self-Startup for Battery-Indifferent Sensor Nodes," *IEEE JSSC*, vol. 56, no. 5, pp. 1618-1629, May 2021.
[10] D. Truesdell and B. H. Calhoun, "A 640 pW 22 pJ/sample Gate Leakage-Based Digital CMOS Temperature Sensor with 0.25°C Resolution," *IEEE CICC*, pp. 1-4, Apr. 2019.

[11] S. Carreon-Bautista et al., "An Autonomous Energy Harvesting Power Management Unit with Digital Regulation for IoT Applications," *IEEE JSSC*, vol. 51, no. 6, pp. 1457-1474, June 2016.

[12] J. Li, et al., "Triple-Mode, Hybrid-Storage, Energy Harvesting Power Management Unit: Achieving High Efficiency Against Harvesting and Load Power Variabilities," *IEEE JSSC*, vol. 52, no. 10, pp. 2550-2562, Oct. 2017.

[13] H. Kim et al., "A Dual-Mode Continuously Scalable-Conversion-Ratio SC Energy Harvesting Interface With SC-Based PFM MPPT and Flying Capacitor Sharing Scheme," *IEEE JSSC*, vol. 56, no. 9, pp. 2724-2735, Sept. 2021.