Analyzing Static and Dynamic Write Margin for Nanometer SRAMs

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ABSTRACT
This paper analyzes write ability for SRAM cells in deeply scaled technologies, focusing on the relationship between static and dynamic write margin metrics. Reliability has become a major concern for SRAM designs in modern technologies. Both local mismatch and scaled V_{DD} degrade read stability and write ability. Several static approaches, including traditional SNM, BL margin, and the N-curve method, can be used to measure static write margin. However, static approaches cannot indicate the impact of dynamic dependencies on cell stability. We propose to analyze dynamic write ability by considering the write operation as a noise event that we analyze using dynamic stability criteria. We also define dynamic write ability as the critical pulse width for a write. By using this dynamic criterion, we evaluate the existing static write margin metrics at normal and scaled supply voltages and assess their limitations. The dynamic write time metric can also be used to improve the accuracy of VCC_{min} estimation for active V_{DD} scaling designs.

Categories and Subject Descriptors
B.3.1 [**Memory Structures**]: Semiconductor Memories – *Static memory (SRAM);* B.8.2 [**Performance and Reliability**]: Performance Analysis and Design Aids

General Terms
Design, Performance, Reliability

Keywords
SRAM, Write margin, Dynamic noise margin, Reliability, VCCmin, Static Noise Margin, Variation

1. INTRODUCTION
With increased device variability in nanometer scale technologies, SRAM becomes increasingly vulnerable to noise sources. The wider spread of local mismatch leads to reduced SRAM reliability. For the demand of minimizing power consumption during active operation, supply voltage scaling is often used. However, SRAM reliability is even more suspect at lower voltages. VCC_{min} is the minimum supply voltage for an SRAM array to read and write safely under the required frequency constraint. Therefore, the analysis of SRAM read/write margin is essential for low-power SRAMs. In recent years, research on sub-threshold SRAMs has shown the promise of SRAM design for energy-efficient and ultra-low-power applications. The most challenging issue for sub-threshold SRAM is increasing reliability during read/write. A good metric for read/write margin is critically important to all kinds of SRAM designs. In this paper, we will emphasize SRAM write margin analysis, although our approach to this analysis is readily applicable to dynamic read margin.

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Static noise margins (SNMs) are widely used as the criteria of stability. The traditional butterfly SNM approach is the most popular one, although recent studies on the N-curve have demonstrated its benefit as an alternative metric for SRAM cell stability. For static write margin, there also exist several other static metrics, such as BL and WL margin. Some of them have shown some advantage over the SNM approach, but no work has given a thorough comparison of all of these metrics. It is also unclear whether these static approaches remain valid for scaled supply voltages and future technologies. Therefore, it is necessary to examine all the existing static write margin approaches and find the best one for scaled supply voltages. In this paper, we evaluate the static approaches by comparing them with dynamic write margin. While static margin is often easier to simulate and measure, it has the drawback of disregarding time dependencies. In fact, a real write operation is a time-dependent event. The dynamic write ability is the true indicator of how easily the cell can be written within a time constraint.

A key insight of this paper is that we can analyze the write operation as an injection of current noise into the cross-coupled inverters in the bitcell, which allows us to use concepts of dynamic stability to analyze the write ability of the cell. We propose to quantify the dynamic write ability as the minimum WL pulse width required to flip the cell's state. We evaluate the static metrics against this dynamic metric and find that some of them have a very poor correlation with dynamic write ability, and one even shows fake write failures at lower V_{DD}.

VCC_{min} is a critical parameter for low-power SRAM designs. For a given frequency constraint, lower VCC_{min} increases power savings, but write and read ability must be ensured at VCC_{min}. Our paper shows that the proposed dynamic write time definition improves the accuracy of VCC_{min} prediction and thus allows a better tradeoff among frequency, power and reliability.

We use a commercial 45nm CMOS bulk process for all of the simulations in this paper. We first review existing approaches for SRAM static write margin in Section 2. Section 3 analyzes write ability in the context of dynamic noise margin and proposes a definition of the critical time (T_{CRIT}) as the dynamic write ability criterion. Section 4 examines the static approaches in terms of the correlation with the dynamic criterion T_{CRIT}. In Section 5, we discuss how write ability limits VCC_{min} and show that the use of T_{CRIT} can help to estimate VCC_{min} more precisely. The conclusions are drawn in Section 6.

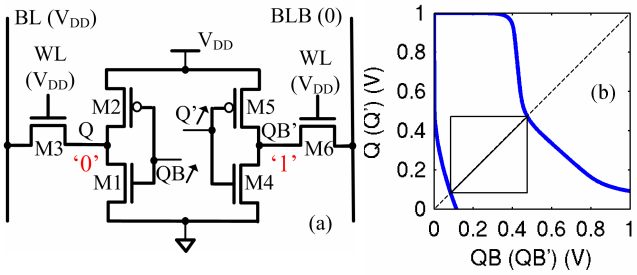

Figure 1: (a) Circuit for WSNM of writing '1'. (b) WSNM of writing '1' is the width of the smallest embedded square at the lower-right side. Here the WSNM is 0.390V.

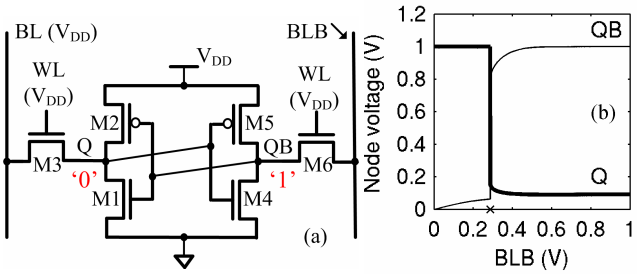

Figure 2: (a) Circuit for sweeping BL to get write margin. (b) Write margin is the BLB value when Q and QB flip. Here the write margin is 0.287V.

2. STATIC WRITE MARGINS

In this section, we introduce five existing static approaches for measuring write margin. The most common static approach uses SNM as a criterion (e.g. [1]). The cell is set in the write operation. Figure 1a shows the circuit for writing a '1' into the cell. Write SNM (WSNM) is measured using butterfly (or VTC) curves (Figure 1b), which are obtained from a dc simulation sweeping the input of the inverters (QB and Q'). For a successful write, only one cross-point should be found on the butterfly curves, indicating that the cell is monostable. WSNM for writing '1' is the width of the smallest square that can be embedded between the lower-right half of the curves. WSNM for writing '0' can be obtained from a similar simulation. The final WSNM for the cell is the minimum of the margin for writing '0' and writing '1'. A cell with lower WSNM has poorer write ability.

The BL voltage can also be used as a measure of write margin [2]. The 6T cell is configured as in Figure 2a for a write '1' case. The voltage of BLB (the bitline connected to the node holding '1' initially) is swept downward during simulation. The write margin is defined as the BLB value at the point when Q and QB flip (Figure 2b), which we will call VBL. The lower that value is, the harder it is to write the cell, implying a smaller write margin.

A third definition of write margin measures the WL voltage on the half-cell holding '1' [3], which we call VWL_R. The authors showed that VWL_R is inversely proportional to the access transistor mismatch over a wide PVT range. Figure 3a shows the circuit setup. The WL (WL_L) and the input of the left half-cell are always V_{DD} so Q remains at its lowest dc value due to a read and connects to the input of the right half-cell. The voltage of WL_R, the WL at the right half-cell, is swept from 0 to V_{DD} during dc simulation. The write margin is defined as the margin between V_{DD} and the critical WL_R value at which QB reaches the switching point of the left half-cell, VM_L. We can get the VM_L value, which is 0.474V, from previous

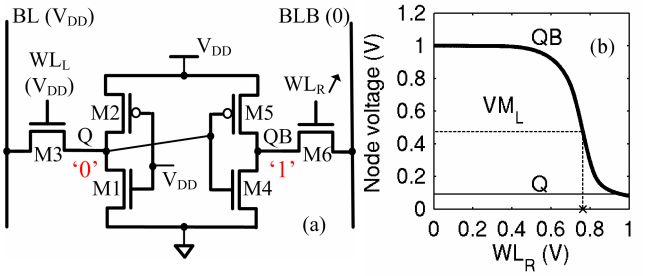

Figure 3: (a) Circuit for sweeping WL_R to get write margin. (b) Write margin is the margin between V_{DD} and the WL_R value at which QB reaches the switching voltage of the left half-cell. Here the margin is 0.237V.

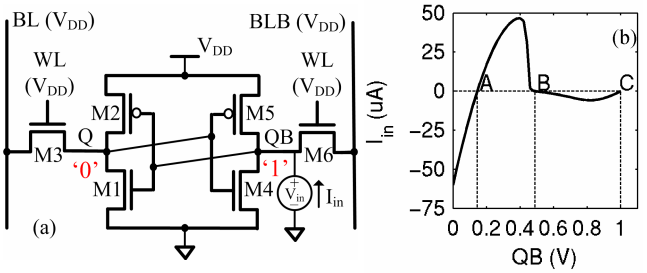

Figure 4: (a) Circuit for N-curve. (b) WTV is the voltage difference between C and B; WTI is the negative current peak between C and B. Here WTV is 0.511V and WTI is 5.86uA.

VTC curve. Figure 3b shows that the VWL_R write margin for this cell is 0.237V.

Another static method uses an N-curve, which was first proposed by [4] for read stability. [5] extended the use of the N-curve to be a measure of write ability. The unique feature of the N-curve is the use of the current information. In Figure 4a, the cell initially holds '0' and both the two bitlines are clamped to V_{DD}. A dc sweep on node '1' (QB) is performed to get the current curve through the dc source (I_{in}). Figure 4b shows the I_{in} curve for the example cell. The current curve crosses over zero at three points A, B and C from left to right. The curve between C and B is the relevant part for write ability. [5] defined the voltage difference between C and B as the write trip voltage (WTV), defined the negative current peak between C and B as the write-trip current (WTI), and stated that a higher WTV or WTI implies a smaller write margin. It should be noted that WTI actually is the current when VBL reaches the trip point as using the BL method. But these two metrics are not equal. Because of different access transistor strength, cells with the same VBL value might have different WTI values and vice versa. Authors in [5] suggested both WTV and WTI should be evaluated for more accurate write ability analysis, while we find that WTV and WTI are both poorly correlated with write ability, as we will explain in Section 4.

The final static method is an improvement over the previous WL method [6]. Instead of only sweeping the WL at the side holding '1', this approach sweeps the WL at both sides simultaneously to replicate a real write operation, where a WL pulse drives both of the access transistors. The write margin is defined as the difference between V_{DD} and the WL voltage when the nodes Q and QB flip (see Figure 5). We call this metric VWL.

All the static approaches assume the WL pulse width is infinite in duration because they only account for its amplitude. However, in a real write operation, the WL pulse width is finite and proportional to

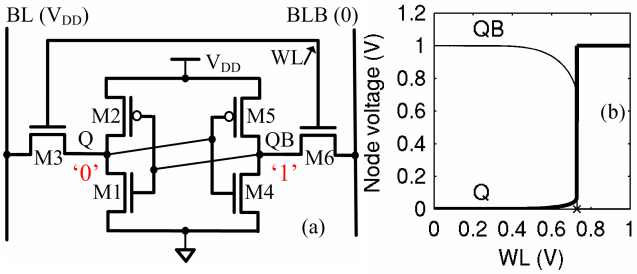

Figure 5: (a) Circuit for write margin from WL sweeping. (b) Write margin (VWL) is defined as the difference between V_{DD} and the WL voltage when the nodes Q and QB flip. For this case, the write margin is 0.272V.

the cycle time. Therefore, it is necessary to investigate dynamic write margin metrics and evaluate the validity of the static ones by comparing them with the dynamic alternatives. But first, we need to clarify the criterion for a write failure so we can select a proper definition of dynamic margin. It should be noted that besides the finite pulsed WL, other timing dependencies, such as power supply noise [7], are excluded by static methods but contribute to dynamic stability. In our paper, we will mainly focus on the impact of the pulsed WL on dynamic stability. However, similar dynamic write failure criterion can be used to examine other dynamic write dependencies.

3. DYNAMIC WRITE MARGIN

To define the dynamic write margin, we should first clarify the criterion for a write failure. A write failure is usually considered to occur when the write time (T_{wr}) is larger than the WL pulse width (T_{WL}). T_{WL} depends on a number of factors, such as the number of BLs and the WL driver, but we are only interested in the final pulse for this paper. T_{wr} is often defined as the time when the node storing '1' is pulled down from V_{DD} to a critical low value. However, the proper definition of this critical low value is not so clear. In [8], the trip voltage of the inverter initially holding '0' is considered as the critical low value, while [9] uses zero as the critical low value. The former is too optimistic and leads to an underestimation of the write failure probability, while the latter is too pessimistic and leads to an overestimation of the write failure probability. Authors in [7] define a write failure to occur when the voltage of the node initially holding '1' is not lower than the other node voltage by the end of the cycle (not the WL pulse). This write failure definition is valid for most reasonable write cycles that last longer than the WL pulse, however it obscures the actual cause of a write failure, which is closely related to the WL pulse. As we will show later, if the time between the end of the WL pulse and the end of the cycle is small, it is possible for a write to succeed by this definition while ultimately failing. In this paper, we will reveal the mechanism of the write event and examine dynamic write margin in the context of dynamic noise margin. We will also propose a new definition of the critical write time.

3.1 Dynamic Noise Margin

Analysis of the dynamic noise margins for logic gates has shown that both the noise amplitude and the noise duration are critical for dynamic stability [10][11]. Dynamic noise margins are larger than the static ones [10] because larger amplitude noise events can be tolerated if they persist for a sufficiently short time. Dynamic stability analysis was applied to an SRAM cell that resulted in an analytical model for evaluating its dynamic noise margin while in

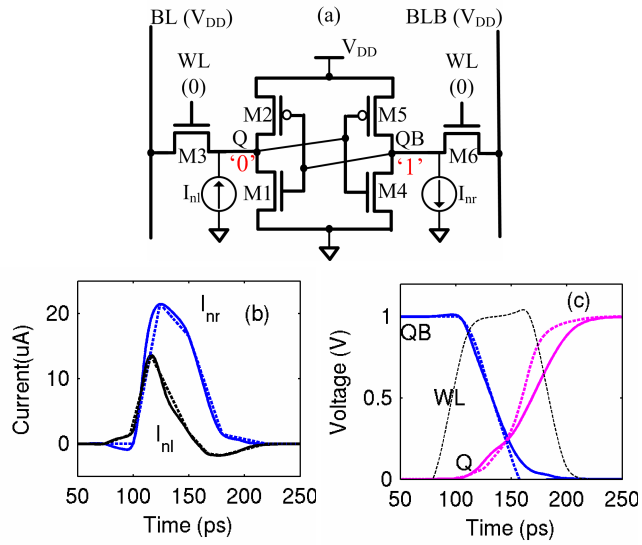

Figure 6: (a) SRAM cell schematic with two transient current noises being injected. (b) I_{nr} and I_{nl} from a write simulation are approximated with PWL waveforms. (c) The waveforms of Q and QB from a write simulation (solid curves) and from the current noise circuit (dashed curves).

the standby mode [12]. This model assumes that the noise source is a current noise pulse injected into the node storing '0'. For a given noise amplitude, the model estimates the critical pulse width, i.e., the minimum pulse duration for the noise to flip the cell's state. A dynamic instability occurs when the injected noise causes the cell's state to follow a trajectory that crosses the boundary of attraction regions (e.g. regions that will settle to different stable points). However, [12] assumed that the boundary between attraction regions, also called the separatrix, is always the line where Q=QB, so they used the final condition that the two nodes reach the same voltage. In fact, this assumption about the location of the separatrix is only true for a balanced nominal cell (i.e. without mismatch). Recent analysis in [13] has shown that the separatrix relocates off of the line Q=QB due to device variation and has proposed a technique to identify the separatrix while taking into account device mismatch.

3.2 Modeling an SRAM Write as a Dynamic Noise Event

In this paper, we propose to view an SRAM write event as a dynamic noise disturbance. Taking this view of the write will allow us to analyze the SRAM dynamic write margin in the presence of variation by using knowledge of the bitcell's dynamic stability and the location of its separatrix.

During a write operation, we can model the current sinking or injecting through the access transistors as current noise sources. When the WL rises up on the side of the half-cell holding '1', the current through the access transistor is equivalent to a current noise source I_{nr} that will sink current from node QB. On the other side of the cell, the current through the access transistor is equivalent to a current noise source I_{nl} that will inject current into node Q. Figure 6a shows the proposed equivalent noise model for a write operation. There are two major differences between the noise source for cell hold stability and the one for cell write ability. For hold stability analysis, as in [12], a single current noise source is added to the cell; while here we have two noise sources that perturb opposite sides of the cell. Second, in the write scenario, the current sources I_{nr} and I_{nl}

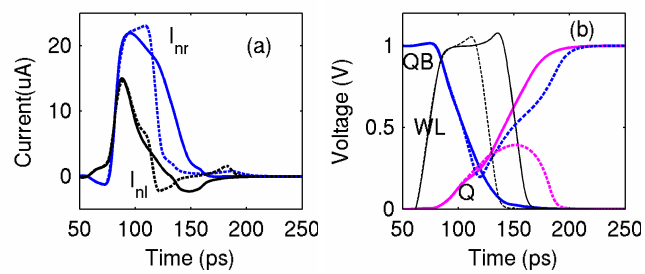

Figure 7: (a) Simulation of I_{nr} and I_{nl} and (b) of Q and QB. Solid and dashed lines correspond to a WL pulse width of 78ps and 53ps, respectively.

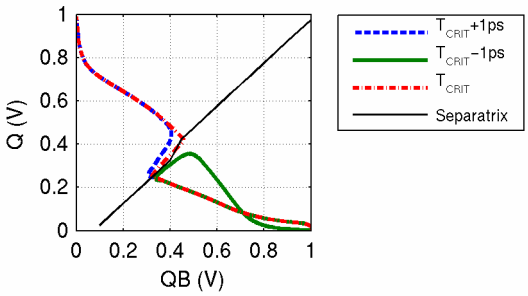

Figure 8: Trajectories for writing '1' (starting point (QB,Q)=(1,0)) when T_{WL} is equal to T_{CRIT} and T_{CRIT}±1ps.

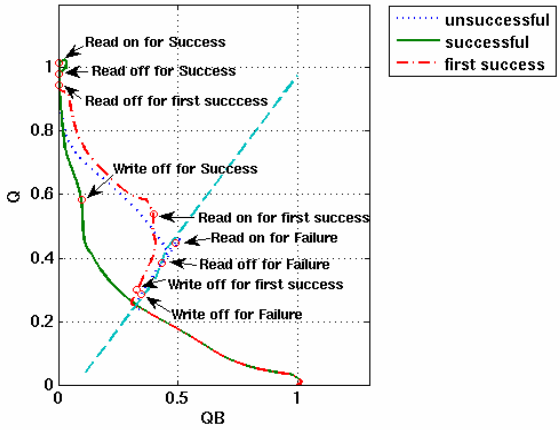

Figure 9: Trajectories for a writing '1' when taking count of a successful RAW.

do not inject ideal current pulses with constant amplitude. In Figure 6b, the solid curves show the real currents through the access transistors from a transient simulation of a write operation. We can approximate the two currents with a simple piece-wise-linear (PWL) waveform model as shown in Figure 6b with the dashed curves. With these two current noise sources modeled as I_{nr} and I_{nl}, we re-simulated the circuit in Figure 6a. Figure 6c shows that the Q and QB values from the current noise circuit (dashed curves) are quite close to the real Q and QB waveforms (solid curves) from a write simulation. Therefore, the current noise circuit can be considered as a good approximation of the write circuit. The peak of the noise current is determined by the strength of the access transistor. The duration of the current source is determined by the width of the WL pulse. Figure 7 shows the simulated waveforms from two different WL pulse widths. Both WL pulses generate the same peak current value, but the current waveform for the narrower WL pulse is truncated at the falling edge of the WL pulse, leading to a write failure. To ensure a successful write, the amplitude of the current noises should be large enough *and* the duration of the current pulse should be long enough to enable the cell's state (e.g. (QB,Q)) to cross over the separatrix.

3.3 Critical Time for Write

In order to evaluate the write ability of a cell more precisely, a metric which takes into account the dynamic write behavior must be used. On a successful write, Q and QB cross over and eventually settle at V_{DD} and 0V, respectively. The WL pulse width (T_{WL}) determines whether or not the two waveforms cross and the write is successful. We propose to use the minimum WL pulse width (T_{CRIT}) for the cell to flip ultimately to the correct new state as a metric for dynamic write margin. In order to understand T_{CRIT} as a useful metric, we will relate it back to the dynamic stability analysis that we described in Section 3.1.

Figure 8 shows the trajectories of Q and QB for writing '1' when T_{WL} is equal to T_{CRIT}−1ps, T_{CRIT}, and T_{CRIT}+1ps. The thinner solid line is the separatrix for this cell, which is the cell with the largest T_{CRIT} out of 1000 M-C simulations. The trajectories all overlap each other as they approach the separatrix, but they diverge at that point because the WL pulses end at slightly different times. The two trajectories for $T_{WL} \geq T_{CRIT}$ then overlap again as they converge to the newly written value, but the trajectory for $T_{WL} < T_{CRIT}$ falls back to the starting state. This simulation clearly shows that T_{CRIT} is the WL pulse width that causes the state of the cell (QB,Q) to cross over the separatrix when the WL drops to 50% of V_{DD}. Notice that variation has pushed the separatrix off of the line Q=QB. As in this cell, when we write '0' instead (trajectory starts from (QB,Q)=(0,1)), the voltages at Q and QB can actually cross, but, if the trajectory does not cross the separatrix, the write can still eventually fail.

Process variations will make T_{CRIT} difficult to predict since both the trajectory of the cell state during the WL pulse and the separatrix of the cell will vary with the device parameters, but we can make a few observations. First, the intersection of the separatrix with the trajectory curve is the value of Q and QB when $T=T_{CRIT}$. Since write accesses to an SRAM bitcell depend on pulling the '1' node low, this intersection point will generally lie in the bottom left quadrant of the state space. Second, our definition of T_{CRIT} gives the minimum T_{WL} in order to write the cell eventually, but in practice a write operation must complete before the next operation begins. In other words, if a read operation at the same address follows the write operation, it should return the correct value.

Simulation of a read after write (RAW) scenario can reveal how this extra constraint impacts our write margin definition. We consider the read to be correct if a BL differential of at least 100 mV (BL precharge voltage is 1.0V) develops by the end of the WL pulse in the Read operation. Otherwise, the write cannot be considered successful, even if the cell eventually writes. Figure 9 shows the trajectories traversed by the worst case cell in a 1Kb SRAM for an RAW in a write '1' scenario. The dashed line denotes the separatrix for this cell. In all three cases, the cell eventually writes. However, when T_{WL} is much larger than the T_{CRIT}, as in the solid line, the disturbance caused by the Read operation does not affect the write and there are no bends in the path. In fact, we can see that when the WL pulse turns on for the Read operation, the cell has already reached the stable state. For a T_{WL} which is slightly less than T_{CRIT}, the trajectory has just reached the separatrix, as indicated by the

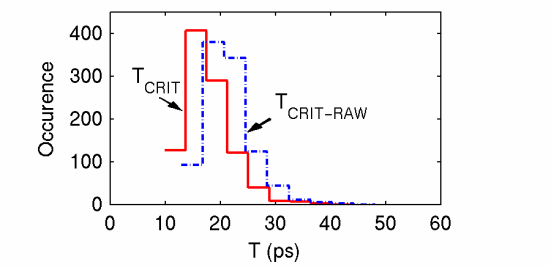

Figure 10: T_{CRIT} & $T_{CRIT-RAW}$ distribution at V_{DD}=1.0 V

dotted line. But, when the Read WL pulse arrives at that instant, it perturbs the cell so that the wrong value is read. Thus, the write operation is not truly successful in this case. We define $T_{CRIT-RAW}$ as the critical WL pulse for a successful RAW. When T_{WL} is equal to $T_{CRIT-RAW}$, the state of the cell is such that the Read operation is successful. This is denoted by the dash-dot line in Figure 9. In this case, the state trajectory is sufficiently far away from the separatrix when the Read commences. Towards the end of the Read cycle, the cell has nearly reached its final stable state.

$T_{CRIT-RAW}$ depends on the time available before the next WL pulse occurs (e.g. including BL precharge time, etc.), since the cell being written will settle toward its final value during that time. With device mismatch, T_{CRIT} or $T_{CRIT-RAW}$ of the cells within the same chip will vary. Figure 10 shows the distribution of T_{CRIT} and $T_{CRIT-RAW}$ over 1000 Monte Carlo iterations at a V_{DD} of 1.0 V. The $T_{CRIT-RAW}$ distribution has a higher mean than T_{CRIT} but with a similar standard deviation, and both distributions have large tails. For high performance SRAMs with short times for the written cells to settle prior to a following read, designers need to analyze both read and write operations together to assess $T_{CRIT-RAW}$ for the array. The T_{CRIT} time provides us with a means of quantifying the ability of a cell to be written successfully in a dynamic fashion. We can use this metric to assess circuit level changes aimed at improving write ability.

4. USING STATIC METRICS FOR DYNAMIC STABILITY

Static measures of write margin are convenient and fast for simulation and testing. If they accurately reflect the dynamic behavior of the write operation, then we can use them to identify cells that will limit write ability in the presence of variation and at lower operating voltages. In this section, we will examine the relationship of the standard static metrics to T_{CRIT}.

Figure 11 shows the correlation between T_{CRIT} and each static metric at V_{DD}=0.6V. The correlation plots reveal that the N-curve metrics, WTV and WTI, have a poor correlation with T_{CRIT}. A higher WTI or WTV value is supposed to imply a weaker write ability, which should indicate a higher T_{CRIT}. However, in Figure 11e and 11f, those points with highest T_{CRIT} correspond to a wide range of WTI and WTV values. WTI and WTV are measured in the context of a read operation, so they should be considered as metrics for read stability instead of write ability. Write ability has a strong dependence on V_{T-X1}, the threshold voltage of the access transistor for node '1', because the corresponding BL is 0 during write and a

Table 1: Correlation coefficient (CC) between each write margin and ΔV_{T-X1} at V_{DD}=0.6V

	T_{CRIT}	SNM	VBL	VWL_R	VWL	WTV	WTI
CC	0.60	-0.54	-0.61	-0.60	-0.65	-0.15	-0.03

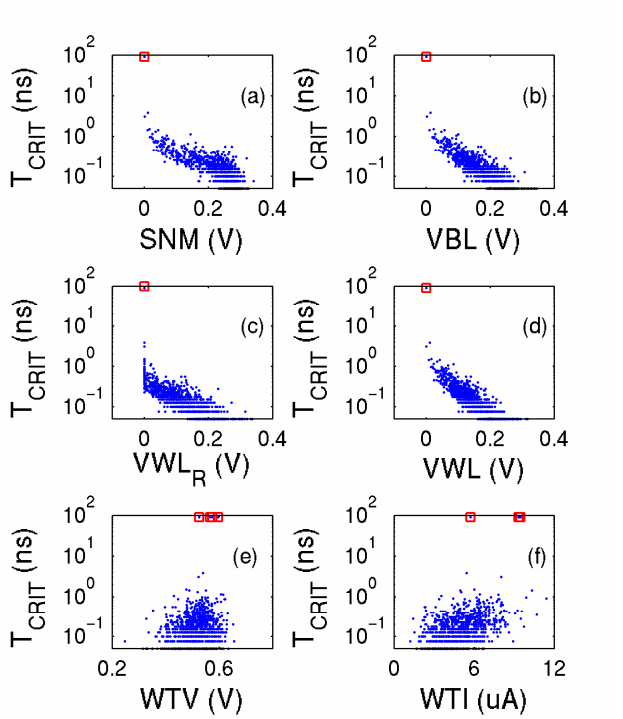

Figure 11: Correlation between each static metric and T_{CRIT} at V_{DD}=0.6V. Points highlighted with square actually never flip ($T_{CRIT}=\infty$); their values are assumed to 90ns for display.

large amount of current would flow through it to discharge the node '1'. Table 1 shows the correlation coefficient between static/dynamic write margin metrics and V_{T-X1} variation (ΔV_{T-X1}). Most of them have a correlation coefficient with large magnitude (e.g. 0.60 for T_{CRIT}), which verifies that V_{T-X1} has a strong impact on write ability. WTI and WTV have the least correlation with V_{T-X1} because both bitlines are clamped at V_{DD} in the simulation for these metrics. Therefore, WTI and WTV are not good metrics for write ability.

The VWL, VWL_R, VBL, and SNM metrics all show a good match for the never-flipped case (those points highlighted with square), and a good correlation to T_{CRIT}, especially at the worst case tail. However, VWL_R metric also develops some fake zero-write-margin errors. In Figure 11c, a significant set of points with VWL_R=0 exhibit low T_{CRIT} values. This means that the VWL_R metric cannot uniquely identify cells that have poor dynamic write ability. This type of error occurs because the half-cell holding '1' in the VWL_R simulation has its input always connected to V_{OL} (the lowest output of the other half-cell). In reality, this condition only happens at the onset of the write transition. As the transition continues, Q and QB will enter the positive feed-back region of the state space, which accelerates the flipping process and explains why VWL_R mis-categorizes some write-able cells as having zero write margin.

For the VBL metric, it should be noted that setting WL to V_{DD} before sweeping down BL is similar to a read operation, which might be capable of flipping the cell if the variation causes such a strong write ability that a read could change the cell's state. For this special case of write success, since the storage nodes already flip before BL sweeping, no voltage or current change on nodes will happen during the BL voltage sweep process. Therefore, the

designer must pay attention to the absolute voltage of nodes in this case; otherwise it might be mis-categorized as a write failure.

The limitation of VWL_R approach and the special care needed for VBL approach leave the SNM and VWL static metrics as having the best correlation with T_{CRIT} at the tails. However, SNM has less correlation with T_{CRIT} across the full range of values. In addition, it is actually harder to measure SNM directly from silicon. And as Table 1 shows, VWL metric has the highest correlation with the access transistor mismatch. These considerations indicate that the VWL method is the best among these static metrics for assessing the dynamic write ability of SRAM cells for lower V_{DD} and future nanometer technologies.

5. WRITE MARGIN & VCC_{min}

The need to reduce power in systems with embedded SRAMs makes lowering the supply voltage an appealing option, but the minimum voltage, VCC_{min}, is limited by the failure rate of read and write operations. The longest T_{CRIT} for the cells in the SRAM array will limit the VCC_{min} value. Figure 12 shows, for different definitions of write failure, the change in the critical WL pulse width with V_{DD} scaling, for the worst cell within a 1-Kb SRAM. The dotted line represents the critical T_{WL} when a successful write is defined as in [8] (node storing 1 pulled down to trip voltage of the other inverter), the solid line represents the T_{CRIT} as defined in this work (cell eventually writes), and the dash-dot line represents the critical T_{WL} as defined in [9] (node storing 1 pulled down to 0). We can observe that for all the definitions, the critical T_{WL} increases rapidly below 0.75V. This curve will shift upwards for larger SRAMs since the larger number of cells will include cases with worse variation, leading to higher T_{CRIT} values. The size of the SRAM array and the frequency constraint for the application will determine the VCC_{min} value. An important observation is that earlier definitions in [8] and [9] underestimate or overestimate the critical WL pulse width for a write. This leads to an underestimation or overestimation of the write failure probability and the VCC_{min} value for a given SRAM.

6. CONCLUSIONS

In this paper, we analyzed both static margin and dynamic margin for SRAM write ability. We proposed to analyze a write operation as the current pulse noises that are injected purposely to defeat the cell's dynamic stability. Our proposed way of viewing a write operation as an intentional noise event allows us to use analysis of dynamic noise margin for modeling an SRAM's dynamic write ability. A new definition of the dynamic write ability, T_{CRIT}, was proposed. It gives the critical time for write, which is the minimum duration of the WL pulse that can eventually move the cell from one stable state to the other. With this dynamic critical write time, we are able to examine the static write margin metrics fairly. The correlation between the dynamic margin and each static metric reveals that none of the static ones is a strong indicator of dynamic write ability, especially the N-curve metrics. In addition, the WL approach proposed by [3] is unreliable under certain conditions, especially at scaled V_{DD}. The improved WL approach [6] is the best candidate for static write margin because it exhibits the best correlation with dynamic write margin as well as the access transistor mismatch, and maintains this at a lower V_{DD}. T_{CRIT} is also used to determine VCC_{min} for dynamic voltage scaling. Although our paper only focused on the write ability, the similar dynamic analysis method can be used for cell read stability. Ultimately, with the aid of dynamic read/write margin analysis, SRAM designers can discover new techniques for improving SRAM reliability at lowered supply voltages.

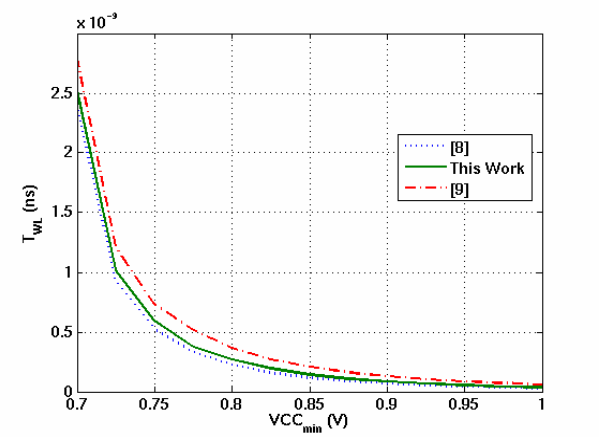

Figure 12: VCC_{min} vs. the critical WL pulse width (T_{WL}) for writing the worst cell within a 1-Kb SRAM.

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