Minimizing Offset for Latching Voltage-Mode Sense Amplifiers for Sub-threshold Operation

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ABSTRACT

This paper examines latch style voltage mode sense amplifiers for operation in the sub-threshold region, where $V_{DD}<V_T$. We show that the offset gets worse relative to strong inversion as technology scales. Furthermore, increasing the sizes of devices in the sense amplifier does not yield the reduction of input referred offset according to $1/(WL)^{0.5}$ that is achieved for strong inversion operation. We analyze the source of the offset and propose circuit level operating principles for minimizing its impact in sub-threshold SAs. This design methodology will optimize sub-V_T SAs for more robust ultra low power operation.

1. INTRODUCTION

Sense amplifiers (SAs) are used widely in digital circuits for a number of different important applications including SRAM [1], DRAM [2], I/O [3], and A/D conversion [4]. Since the purpose of a sense amplifier is to detect and to amplify a small input signal (either a voltage or current), one of the most important metrics for a sense amp is the input referred offset [6]. Without loss of generality, we will use a differential voltage mode latch-style sense amplifier to discuss the offset. Figure 1 shows an example schematic of a common latch-style sense amp topology. Although the transistors in the SA are non-ideal, it can be cumbersome to treat the non-idealities of each device separately. Instead, the cumulative mismatch in the sense amp is lumped together and modeled as an offset (voltage source in this case) at the input to an ideal sense amp. This modeling approach makes it clear that the differential input voltage must exceed this input referred offset in order to cause the sense amp to amplify the input to the correct large swing value at the outputs.

Many previous works focus on the problem of offset in sense amplifiers. For example, [6] found that offset can be reduced by slowing the rise time of the enable signal, while [7] found that it can be reduced by lowering the DC voltage at the input. As the previous works make clear, continued process scaling tends to cause increases in the input referred offset of sense amp topologies. This is largely due to the overall increase in local (e.g. within-die) process variation due to mechanisms such as lithographic variation and random doping fluctuation (RDF). These local variations cause the threshold voltage (V_T) of transistors with identical layout to be distributed normally, and the standard deviation of the V_T distribution is proportional to $1/(WL)^{1/2}$ [8]. Clearly, differences in the threshold voltage will lead to increased input referred offset for the SA.

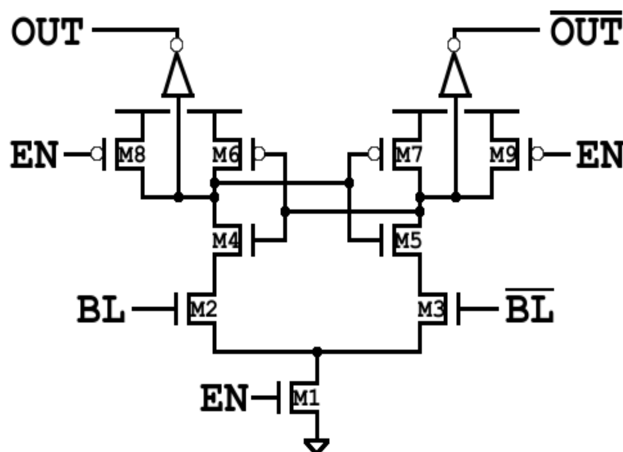

Figure 1: Schematic of a typical latch-type sense amplifier. The sense-amplifier resolves when EN goes high and resets when EN goes low.

Sense amplifiers, along with most other digital circuits, are traditionally operated with a supply voltage (V_{DD}) above the V_T of the transistors. Recent interest in extremely energy-limited applications such as microsensor nodes or medical implants has led to investigate of sub-threshold operation, where $V_{DD}<V_T$. For applications where energy is the most important metric, sub-threshold operation minimizes the energy per operation for digital circuits [13]. The performance and optimization of digital gates [14][15] and SRAM [9][10][11][12] have been explored for sub-threshold operation.

Despite this activity in sub-threshold circuits research, there are very few implementations of sense amps in sub-threshold. The sub-threshold SRAMs demonstrated in [9][10][12] use full swing read circuits in lieu of SAs. Sense amps in [11] are pseudo-differential latch style, but the offset is so large the implementation uses two SAs per column to provide redundancy against variations. This sort of drastic measure is necessary because of the additional difficulty of using SAs in sub-threshold.

This paper will analyze the specific impact of variations on a sense amp operating in sub-threshold and will propose simple changes to the circuit operation to help reduce this impact without significantly altering the topology.

2. Sense Amplifier Offset in Sub-threshold

Sense amplifiers traditionally have two primary metrics of interest: resolution speed and intrinsic input offset [5]. Delay is usually a lesser concern for energy constrained circuits operating at a sub-threshold voltage, so we will assume that the offset is the primary metric for a sub-threshold SA. There are two reasons that justify this

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assumption. The first is that the resolution speed of a sense-amp is relatively fast in the sub-threshold region, approximately as fast as a single static gate (e.g. NAND). Since energy-constrained circuits are less concerned with maximizing throughput than with reducing active and leakage energy, it is therefore worth spending more design time improving the reliability of the device rather than trying to squeeze out an extra performance increase.

The second reason that offset is more important than resolution speed is that SA offset is relatively larger in sub-V_T than at the nominal V_{DD}, and scaling makes this even worse. Figure 2 shows a 1000 point Monte Carlo distribution of the input referred offset voltage divided by the operating voltage (V_{OS}/V_{DD}) for the same SA operating at V_{DD}=1V and V_{DD}=0.4V in two commercial technologies. Although V_{OS}/V_{DD} increases for both V_{DD}s in the 45nm process relative to the 90nm process, the worst-case V_{OS}/V_{DD} becomes relatively worse at V_{DD}=0.4V by nearly 50% in the 45nm process. This indicates that scaling will hinder SA design in sub-V_T more than for strong inversion. These two considerations lead to the conclusion that the standard deviation of the intrinsic input offset voltage (σ_{OS}) must be decreased in order to provide a sense amplifier that is suitably reliable for sub-V_T operation.

In order to explain why V_{OS}/V_{DD} is relatively worse in sub-V_T, we will derive a formula relating mismatch in the SA to V_{OS}. The two major sources of mismatch in the SA are the input pair and the cross-coupled output inverters.

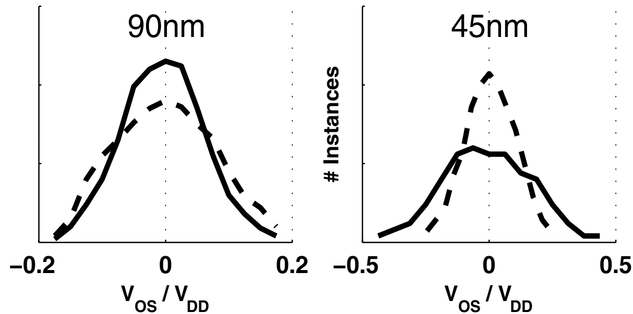

Figure 2: Plots of V_{OS}/V_{DD} vs Number of Instances for a 1000 item Monte Carlo run for V_{DD}=1V (dotted line) and V_{DD}=0.4V (solid line) for the sense amp in Figure 1. V_{OS} was found using a binary search of the voltage at the input.

2.1 Offset-Voltage due to the Input-Pair

We will first consider a derivation of the input-offset arising from V_T variation in the input transistors. By assuming that one side is stronger than the other (i.e. that M_2 is stronger than M_3), we can solve for the offset voltage (V_{OS}) needed at the gate of the weaker device to ensure that I_2=I_3. If each V_T is offset by the same amount from its nominal value: $V_{T2} = V_T + \Delta V_T$, $V_{T3} = V_T - \Delta V_T$, then we can equate the current in M_2 and M_3 and solve for V_{OS}:

$$10^{(V_{GS}-V_T+\Delta V_T)/S} = 10^{(V_{GS}-V_T-\Delta V_T+V_{os})/S}$$

$$10^{\Delta V_T/S} = 10^{(-\Delta V_T+V_{OS}/S)}$$

$$V_{OS} = 2\Delta V_T = V_{T2} - V_{T3} \quad (1)$$

The input-offset of the sense amplifier is equal to the difference in V_T of the two input devices, just as it is in strong-inversion, despite the sub-threshold exponential dependence on V_T. This explains why the maximum value of V_{OS}/V_{DD} is higher in sub-threshold as V_{DD} decreases. If ΔV_T remains constant then $\Delta V_T/V_{DD}$ will increase. If ΔV_T is normally distributed around 0V, then V_{OS} itself will have a Gaussian distribution with a mean of 0V. The yield of the SA for a given minimum difference in the input voltage (ΔV_{IN}) can then be found using a normal distribution; or more commonly, the minimum ΔV_{IN} is set to be 3 or 4 times the standard deviation (σ_{OS}) of the offset voltage to ensure robust SA operation. Figure 3 shows a sweep of V_{DD} vs. σ_{OS}/V_{DD} as V_{DD} is lowered into the sub-threshold region.

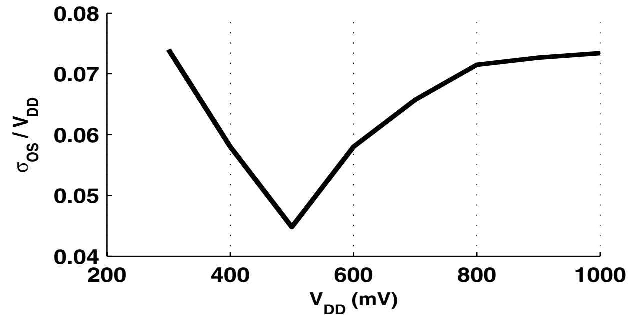

Figure 3: Plot of V_{DD} vs. σ_{OS}/V_{DD} in a 90nm technology.

2.2 Offset-Voltage due to the Cross-Coupled Inverters

This section will show that mismatch in the cross-coupled inverters is as significant as mismatch in the input-pair. To explain this, we will first derive the DC transfer characteristics of a pass-transistor operating in sub-V_T.

The DC transfer curves of a pass-transistor (NMOS, for example) operating in strong-inversion are very easy to describe: the output at the source will equal the input at the drain until the drain voltage exceeds V_{DD}-V_T. At this point, V_{GS} of the transistor equals 0, and it turns off. The same pass-transistor operating in sub-V_T behaves differently. A DC-sweep of an isolated (e.g. unloaded) pass transistor in sub-V_T will show that the input always equals the output. Unfortunately, this will not be the case in realistic circuit situations. The final-value DC value will actually depend on parasitic leakage currents at the source. Figure 4 shows a single pass transistor with a load modeled by an off transistor (e.g. modeling other passgates).

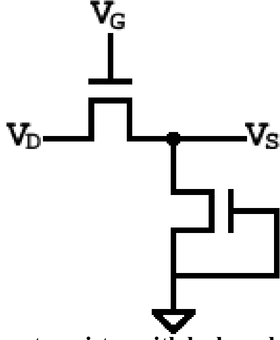

Figure 4: Pass transistor with leakage load.

Using this circuit model and assuming DC voltages for V_G and V_D, the final DC value for V_S can be found by equating the two currents at V_S (through the passgate and through the load):

$$I_O\left(\frac{W}{L}\right)_{PG} 10^{(V_{GS}-V_T+\Delta V_T+\eta V_{DS})/S}(1-10^{-nV_{DS}/S})$$

$$= N * I_O\left(\frac{W}{L}\right)_{LD} 10^{(-V_T+\eta V_S)/S}$$

Where η is the DIBL coefficient, S is the sub-threshold slope, and n is the sub-threshold slope factor. N is the number of leaking transistors in parallel. We ignore the body-effect since at this stage its effect will be quite small. If we assume that n is approximately equal to (1+2η) then we can derive a closed form solution for the final DC value at the source. Although this assumption may not be valid for every technology, the following solution is accurate to within 2% for our simulations:

$$V_S = \frac{1}{\beta}(K - S * \log_{10}(1+10^{(K-nV_D)/S})) \qquad (2)$$

$$K = V_G + \eta V_D + S * \log_{10}(W_P / N * W_L) + \Delta V_T)$$

$$\beta = (1+n+2\eta)/2$$

Equation (2) shows that V_S will vary linearly with ΔV_T. Next, if the drain voltage is close to (or greater-than) the gate voltage (for instance, if both gate and drain are driven to V_{DD}), then the roll-off term will disappear as V_{DS} will be greater than $2V_{th}$. This means that, except for the case of very small load current, the value of V_S when V_D=V_G is given by K/β. Figure 5 shows a simulation of a passgate that displays the dependence of the output voltage on the amount of leakage current in the load. Equation (2) predicts these curves with less than 2% error.

Now we will show the pass transistor's effect on the input-offset of a SA by considering a ΔV_T in one of the NMOS transistors of the cross-coupled pair, M_4 and M_5. Notice that during the reset phase (EN=0) the NMOS transistors of the cross-coupled inverters (M_4 & M_5) will act as passgates because both their gate and drain will be pre-charged to V_{DD}. Therefore, the DC final-value at the source of M_4 (and M_5) will equal K_{MAX}/β, where K_{MAX} is:

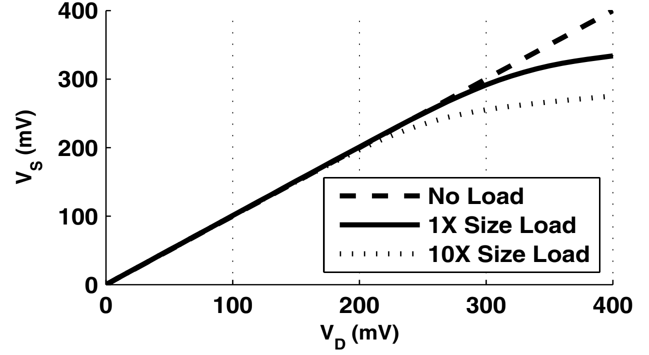

Figure 5: DC transfer curves of a pass transistor operating in sub-threshold from Equation (2); V_G=0.4V.

$$K_{MAX} = (1+\eta)V_{DD} + S * \log_{10}(W_4/W_2) + \Delta V_{T4} \qquad (3)$$

Since the source of M_4 is the drain of M_2, we can use K_{MAX}/β instead of V_{DD} to find V_{DS2}:

$$V_{DS2} = \frac{1}{\beta}K_{MAX} - \frac{1}{\beta}(K_{CASC} - F)) \qquad (4)$$

$$K_{CASC} = V_{INDC} + \frac{\eta}{\beta}K_{MAX} + S * \log_{10}(W_4/W_1)$$

$$F = S\log_{10}(1+10^{(K_{CASC}-nK_{MAX}/\beta)/S})$$

V_{INDC} is defined as the DC voltage at the inputs if ΔV_{IN} were ignored; V_{INDC} will be equal to the input closest to the power rail in most applications. V_{INDC} is nominally at V_{DD} unless lowered by other sources. Notice that in K_{CASC} we must consider the leakage through M_4 rather than M_2 since M_2 cannot have more leakage flowing through it than M_4 no matter how large it is made. Figure 6 plots V_{DS2} as ΔV_{T4} is varied. When ΔV_{T4} is less than 0, the pre-charged value of V_{DS2} is driven deeper into the region where roll-off becomes significant. Therefore, when EN transitions high, it will take a much longer time for M_2 to exit the roll-off region, by which time M_3 will become dominant. Likewise, when ΔV_{T4} is greater than 0, V_{DS2} during

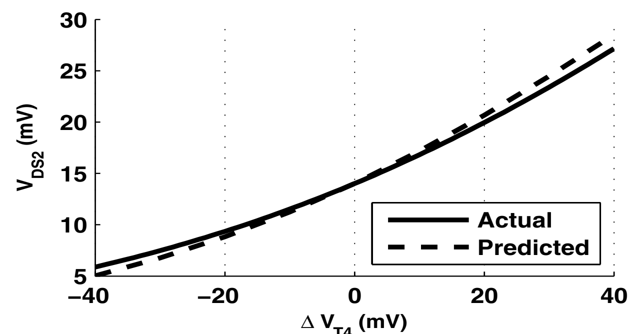

Figure 6: ΔV_{T4} vs. V_{DS2} by Equation (4). V_{DD}=V_{INDC}=0.4V.

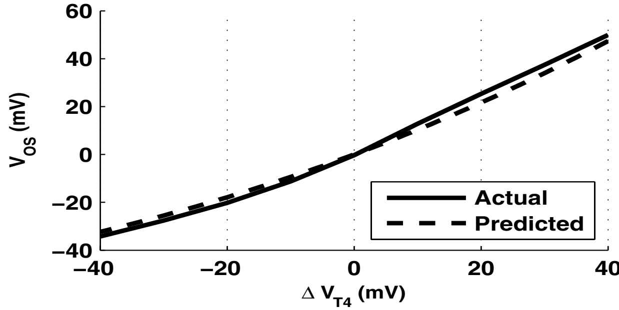

Figure 7: ΔV_{T4} vs. V_{OS} predicted by plugging (3) and (4) back into I_{DS2}. V_{DD}=V_{INDC}=0.4V.

precharge will cause M_2 to move out of the roll-off region and become dominant over M_3. Figure 6 shows how variation on one side of the cross-coupled NMOS pair affects V_{OS} of the SA, but does not directly show how much. By adding together the terms containing ΔV_{T4} from expressions derived in (2) and (3) we can plot the input referred offset. Figure 7 shows ΔV_{T4} vs. V_{OS}. It is easy to see that the difference in ΔV_T gives approximately a linear relationship with respect to V_{OS}, similarly to the input pair, when V_{INDC}=V_{DD}. Therefore, the contribution of the cross-coupled NMOS can be approximated as:

$$V_{OS} \approx \Delta V_{T4} - \Delta V_{T5} \tag{5}$$

Since the cross-coupled PMOS do not influence the pre-charged value of V_{DS2} (and V_{DS3}) they play a very small role in the overall offset of the SA. Simulations show that variation in ΔV_{T6} and ΔV_{T7} by +- 40mV results in less than a +- 5mV change in the offset at 3σ, and therefore the effects from variation on V_{OS} from M_6 and M_7 may be safely ignored.

3. Reducing SA Input-Offset in Sub-V_T

Since the most crucial metric of a sense amplifier operating in sub-threshold is the intrinsic input-offset, V_{OS}, it is desirable to lower this voltage in any way possible. Traditionally, the simplest way to lower the offset of a SA is to increase the size of the devices. The standard-deviation of the variation in V_T of a single transistor is proportional to $1/\sqrt{WL}$ [17], and therefore increasing W or L should decrease the variability of that transistor. Since the offset of the sense amplifier is equal to the difference in V_Ts of the input devices (M_2 and M_3 in Figure 1), increasing their size should decrease the offset of the SA at the cost of area. However, simulation results in Figure 8, a plot of W_{IN} vs. σ_{OS} at V_{DD}=0.4V, reveal that increasing the size of W_{IN} does not appreciably decrease the offset. Increasing W_{IN} initially lowers the standard deviation of the offset, although by less than the predicted $1/\sqrt{WL}$. In fact, the offset begins to increase again as W_{IN} becomes larger.

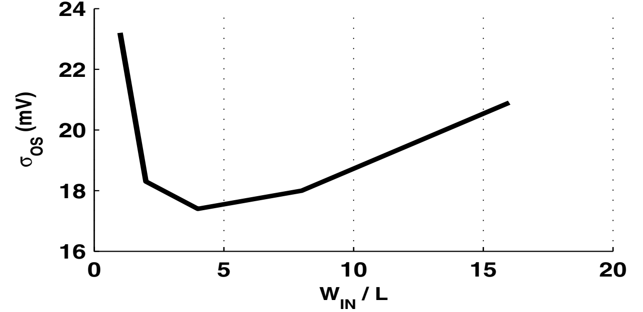

Figure 8: Plot of W_{IN} vs. σ_{OS}. V_{DD}=0.4V.

This phenomenon can be explained by more closely examining the equation describing the current through the input transistors:

$$I_{DS} = I_O \frac{W_{IN}}{L} 10^{(V_{INDC} + \Delta V_{IN} - V_T)/S}$$

As noted in [7], decreasing the value of V_{INDC} relative to V_{DD} will decrease the offset of the sense amplifier because it decreases the absolute imbalance of the starting voltages at the intermediate nodes between M_2 and M_4 (and thus V_{DS2}) and between M_3 and M_5 (and thus V_{DS2}). In Section 2.2 we have shown why this imbalance in V_{DS} will have a direct near-linear effect on the offset of the SA. Figure 9 uses (4) to explicitly show the effect of V_{INDC} on the offset. As V_{INDC} decreases, the contribution to V_{OS} from the cross-coupled inverters decreases to almost nothing. Based on this result, (5) can be redefined with a scaling factor as:

$$V_{OS} \approx (\Delta V_{T4} - \Delta V_{T5}) * 10^{-(V_{DD} - V_{INDC})/2S} \tag{6}$$

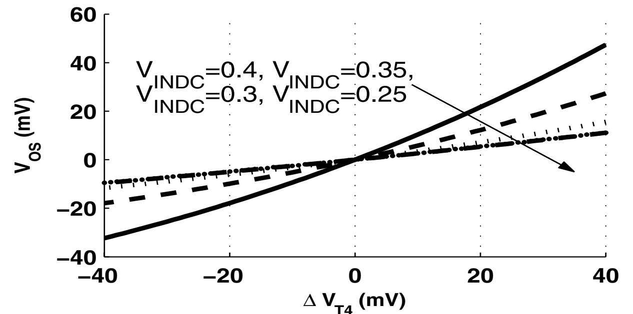

Figure 9: ΔV_{T4} vs. V_{OS} for different V_{INDC}. W_{IN}=4.

For a differential SA, the current through the input transistors also depends on the current through the enable transistor, M_1, which has a width of W_{EN}. W_{EN} is ideally small since all leakage current must sink through it. Since the SA is differential, approximately half of the current flowing through M_1 will go through each of M_2 and M_3. For analysis we can then treat one side of the differential structure as an input device with equivalent width W_{IN}'=W_{IN}/2. Therefore, for this equivalent circuit,

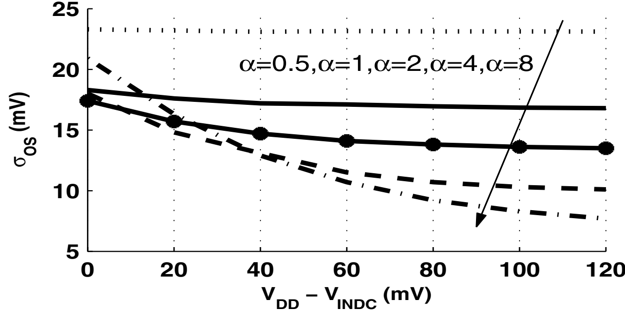

Figure 10: Plot of V_{DD} -V_{INDC} vs. σ_{OS} for different α from simulation. V_{DD}=0.4V.

W_{IN}'=W_{EN}*α/2; where α is equal to W_{IN}/W_{EN}. The current through M_{IN} is thus given by:

$$I_{DS} = I_O \frac{W_{EN} * \alpha/2}{L} 10^{(V_{INDC}+\Delta V_{IN}-V_T)/S}$$

$$I_{DS} = I_O \frac{W_{EN}}{L} 10^{(V_{INDC}+\Delta V_{IN}+S*\log_{10}(\alpha/2)-V_T)/S}$$

By algebraically moving the sizing factor into the exponent, we can see that increasing W_{IN} is equivalent to increasing V_{INDC}. Likewise, the body effect will decrease V_{INDC} by $V_{BE}=\gamma(\sqrt{2\phi_F-V_S}-\sqrt{2\phi_F})$; the nominal V_S can be used here since the effect of variation on V_{BE} is small. Therefore we will redefine V_{INDC} in (6) as $V_{INDC-EFF}$:

$$V_{INDC-EFF} = V_{INDC} - S * \log_{10}(W_{IN}/2 * W_{EN}) + V_{BE} \quad (7)$$

Figure 10 shows a plot of V_{INDC} vs. the standard deviation of the offset voltage for different α. It shows that as V_{INDC} is lowered, the offset of a sense-amp also decreases. The plot also shows that when α increases and V_{INDC} decreases (thus lowering $V_{INDC-EFF}$), the offset of the sense-amp decreases dramatically. Finally, it shows that when V_{INDC} is decreased, there becomes a point where σ_{OS} levels off and stops decreasing due to changes in V_{INDC}. Figure 11 plots the nominal value for V_{DS2} as V_{INDC} is varied to show why this is the case. As V_{INDC} is decreased, the mean value for V_{DS2} is pushed out of the region where roll-off occurs, which is around $2V_{th}$ (~52mV at room temperature). It is at this point that V_{DS} stops having as a large effect on I_{DS}, and the curves flatten in Figure 10.

Although the simulation results clearly show a relationship between $V_{INDC-EFF}$ and V_{OS}, the relationship requires clarification. Therefore, it will be useful to develop a model for the standard deviation of the offset. Equations (1) and (6) give a starting point for V_{OS} based on ΔV_T:

$$V_{OS} \approx (\Delta V_{T2} - \Delta V_{T3}) + (\Delta V_{T4} - \Delta V_{T5}) * T \quad (8)$$

$$T = 10^{-(V_{DD}-V_{INDC})/S}$$

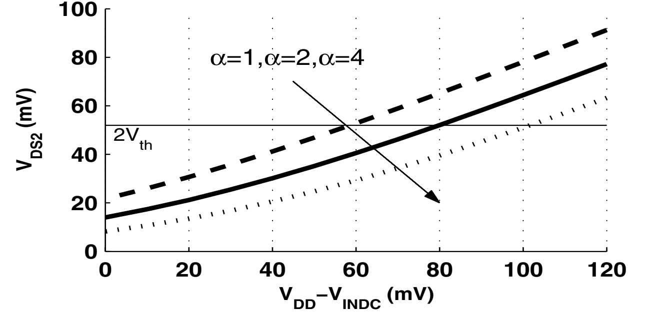

Figure 11: Plot of V_{INDC} vs. V_{DS2} for different α; based on Equation (3).

Equation (8) gives the value for V_{OS} based on the actual difference in V_Ts for the 4 transistors. In practice, these values will be unknown, but the standard deviation in V_T for a minimum-size NMOS transistor (σ_N) will be available. Therefore, by noting that the difference in standard distributions for two I.I.D. normal distributions can be found as $\sigma_{X-Y}=\sigma_X{}^2+\sigma_Y{}^2$, the standard deviation of V_{OS} can be based on (8) and found as:

$$\sigma_{OS} \approx \sqrt{\frac{2\sigma_N{}^2}{W_{IN} * L} + \frac{2\sigma_N{}^2}{W_{EN} * L} * T^2}$$

$$= \frac{\sigma_N}{\sqrt{W_{IN} * L/2}} \sqrt{1 + \alpha * 10^{-(V_{DD}-V_{INDC-EFF})/S}} \quad (9)$$

Here we assume that the size of the the NMOS in the cross-coupled inverter is the same as the size of the enable-transistor. Equation (9) shows that a properly selected V_{INDC} causes the expression for σ_{OS} to collapse to:

$$\sigma_{OS} \approx \sigma_N / \sqrt{L*W_{IN}/2} \quad (10)$$

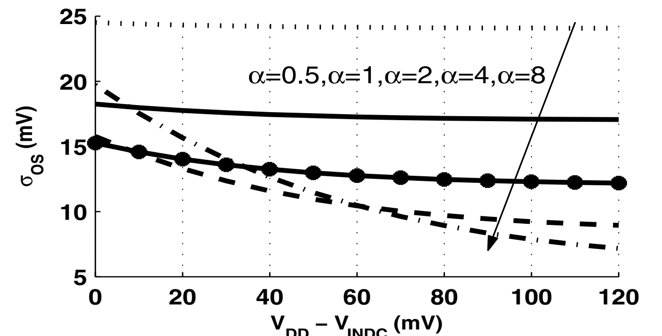

Figure 12: Plot of V_{DD} -V_{INDC} vs. σ_{OS} for different α using Equation (9). V_{DD}=0.4V.

Figure 12 uses (9) to plot V_{DD} -V_{INDC} vs. σ_{OS} for a few α. Although the model shown in Figure 12 is less precise than the one in Figure 10, it does accurately show the impact of $V_{INDC-EFF}$ on σ_{OS}. Figure 13 shows the minimum σ_{OS} at each α from simulation and by selecting V_{INDC} from (10).

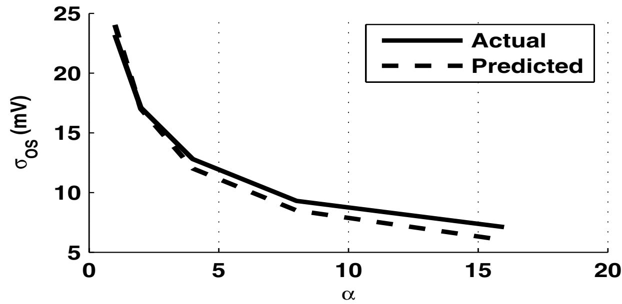

Figure 13: Plot of α vs. σ_{OS} near the optimal V_{INDC} predicted by Equation (10). V_{DD}=0.4V.

4. Sense-Amp Design Methodology

Based on the equations derived in this paper, we propose a methodology for SA design in sub-threshold. In order to minimize the input-offset of the SA there are two options available to the designer: change the sizing of the transistors and/or V_{INDC}. Sizing the transistors is the more flexible option. The cross-coupled inverters should be sized so their V_M is near $V_{DD}/2$ using the method described in [16]. The reset transistors (M_8 and M_9) should be as small as possible to prevent their parasitic capacitances from loading the output. Next, the enable transistor M_1 should be sized the same as the NMOS in the inverters to minimize active and leakage energy in the SA. Increasing the size of M_1, M_4, and M_5 will decrease α and thus lower σ_{OS} at the cost of extra area and energy; however, the same effect can be had by lowering V_{INDC} (e.g. see (9)) at no area cost, and thus this method is preferred. Finally, W_{IN} should be sized for the V_{INDC} of the circuit using (7) so that $\log_{10}(\alpha/2)$ is equal to V_{INDC} and $V_{INDC-EFF}$ is roughly equal to zero.

Two examples will show how V_{INDC} can be designed (or designed around) to achieve minimum offset. First, consider a SA used in a sub-V_T SRAM. In [11], leakage from the cells significantly reduced V_{INDC} by causing both BLs to droop away from V_{DD}. For leaky technologies, this effect can be exploited to decrease V_{INDC}. The drooping '1' bitline will lower V_{INDC} and provide decreased SA offset for a properly sized SA, as shown in Figure 10.

Another example is a low-swing interconnect scheme (e.g. 0 to $V_{DD}/2$ swing) that uses a pseudo-differential p-input sense-amplifier with a reference voltage as the receiver. Designing the reference-voltage to be equal to $V_{DD}/4$ at first seems obvious, but notice that in the case of a "1" the voltages on the bitlines will equal $V_{DD}/4$ and $V_{DD}/2$. Therefore, V_{DD}-V_{INDC} will equal $V_{DD}/4$, which will reduce the offset. However, for a "0", V_{DD}-V_{INDC} will be equal to 0, and the offset for the sense-amp will be much larger. Therefore it makes more sense to increase the value of the reference voltage closer to $V_{DD}/2$ to equalize the effective offset for both input values.

5. Conclusions

In this paper, we analyzed the sources of the input referred offset for a SA in sub-V_T. We showed the impact of sizing and of V_{INDC} for the differential inputs and provided models for understanding how they affect V_{OS}. Based on this analysis, we have proposed a methodology for sizing sub-V_T SAs to minimize offset that will improve the robustness of circuits using SAs in deeply scaled technologies.

6. Acknowledgements

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