SRAM Sense Amplifier Offset Cancellation Using BTI Stress

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Device variability in modern processes has become a major concern in SRAM design leading to degradation of both performance and yield. Variation induced offset in the sense amplifiers requires a larger bitline differential, which slows down SRAM access times. In this paper, we propose a post fabrication technique that takes advantage of the typically detrimental bias temperature instability (BTI) aging effect to improve SRAM sense amplifier offset.

Offset Compensation, SRAM Sense Amplifier, BTI Stress.

I. Introduction

Sense amplifier (SA) input referred offset directly slows the access times of SRAMs and limits the amount of integration of cells on a column. As variability increases with scaling, the offset increases along with other damaging variability effects. Several attempts have been made before to tackle the problem of offset voltage in sense amps including redundancy [4], transistor upsizing [3], and digital compensation [2][5]. Unlike all of the former methods, our approach is not a design time method. Instead, it can be applied after fabrication (e.g. during burnin, power up, or built-in-self-test) and used in addition to other compensation techniques as an initial step to reduce the offset variations.

Bias temperature instability (BTI) is one of the major aging issues that weaken transistors over time. Many studies have examined the impact of BTI on offset voltage and proposed techniques to reduce BTI effects [6][7]. In lieu of only considering BTI as a variation source, it can instead be used as a mechanism for variation compensation. More interestingly, due to its dependence on the stress condition, we can exploit BTI to combat random variation (i.e. mismatch) by applying different stress conditions for different transistors. Our approach is adapted from [1], which applied BTI to SRAM cells that were first reset into a given condition in which BTI stress acted to improve the data retention voltage. We apply a similar concept to reduce the offset voltage in SAs. For a sense amp with mismatch, when we only stress transistors with higher variation induced strength, the BTI induced change can compensate for mismatch and thus contribute to balancing the sense amp. Therefore we propose to exploit BTI to compensate sense amp offset.

We illustrate how the scheme can be applied to a latch based sense amp shown in Figure 1. The main contribution of the sense amplifier offset comes from the NMOS transistors as they are responsible to drive the output nodes to the trigger point while both the PMOSs are still off, so stressing the PMOS transistors will have negligible impact on the offset voltage compared to stressing the NMOS. Variations in the NMOS access transistors M2 and M3 are more dominant in determining the offset than M4 and M5 [2]. Consider a case where M2 has higher threshold voltage than M3 as shown in Figure 2. If a zero-differential input is applied to the sense amp, the output node "OUT" will be driven to 0. M1, M2, M3, M5 and M6 will be in strong inversion indicated by the red circles and will be affected by the BTI stress during compensation. M4 and M7 will be off.

To avoid stressing both the access transistors, the output is fed back to the input as shown in Figure 3 to turn off M2 during

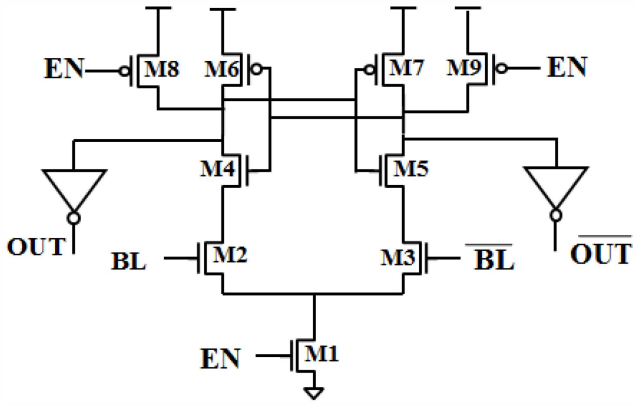

Figure 1. Latch-based sense amp

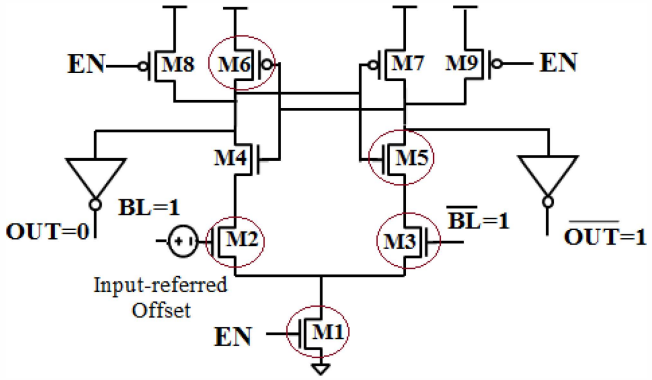

Figure 2. Sense amp condition after it latches according to the input-referred offset, when M2 has higher V_T than M3.

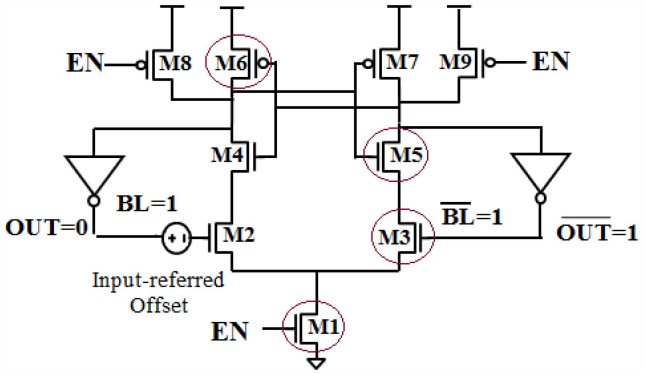

Figure 3. Feeding the output back to the input during stress to avoid stressing the weaker input device.

stress. The feedback saturates the sense amp in the offset direction leaving only M1, M3, M5 and M6 in strong inversion to be affected by the stress as indicated by the red circles. This acts to weaken the stronger side of the SA, reducing the offset.

The scheme has negligible power overhead. It can be easily integrated into burn-in test and use burn-in stress to offset mismatch, or it can be periodically used through the life time of the chip to partially mitigate offset variation from real-time aging. Finally, it can easily be integrated with other compensation techniques as an initial step to reduce the offset.

II. Overstress Avoidance

Applying the stress only one time might cause an extra increase in the threshold voltage that might move sense amplifier offset to the other polarity rather than canceling it. One solution to avoid this is to repeatedly rest the SAs during stress. Each reset event will set each SA into a new state based on its new offset value, the stress will act on the correct devices to reduce the offset toward 0.

Figure 4 shows the effect of applying stress that results in a total of 80mV of shift in the transistor V_T values compared with a reset scheme in which four stress events separated by resets each result in 20mV V_T shifts. The sense amp initial offset was 50mV. Applying stress once overstressed the sense amp in the opposite direction of the initial offset, causing the offset to shift to the other polarity. Repeated stress allows fine tuning of the offset and tends to drive each cell closer to 0 offset. Clearly, more frequent resets can theoretically result in smaller final values of the offset.

III. Simulation Results

We performed 80 Monte Carlo simulations of a SA undergoing a stress event with resets after each effective 20mV change in V_T. Variations within ±40 mV range are included in the threshold voltage of M2, M3, M4 and M5.

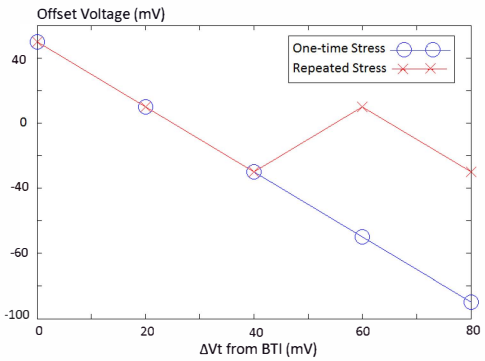

Figure 4. Effect of One-time and repeated BTI stress on the offset voltage

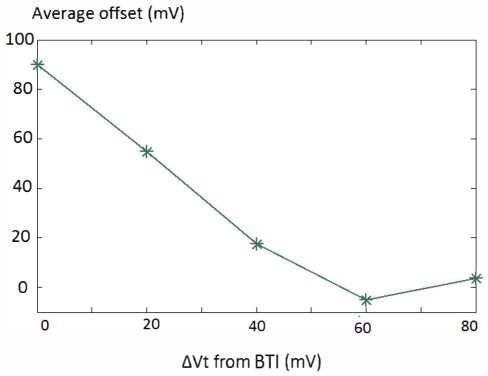

Figure 5. Average value of the offset voltage after each stress step

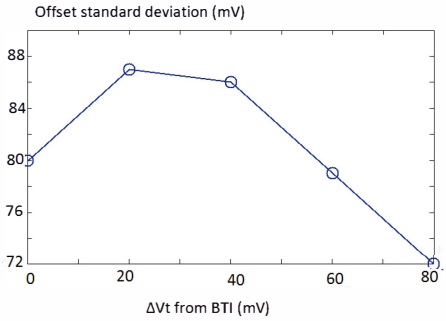

Figure 6. Standard deviation of the offset voltage after each stress step

Figure 5 and Figure 6 show the mean and standard deviation of the offset voltage distribution after each stress step, respectively. Both the average and the standard deviation change non-linearly with the induced threshold shift and might not be monotonic because, while the BTI stress decreases the offset for some sense amps, it increases it for those with offset voltage close to zero. This effect can be minimized by decreasing the period of stress to avoid overstressing the sense amp whose offset is close to zero if this is a concern. Usually, however, the SAs with offset on the worst case tail are the primary concern, and slight degradation of the offset on near-best case SAs is tolerable.

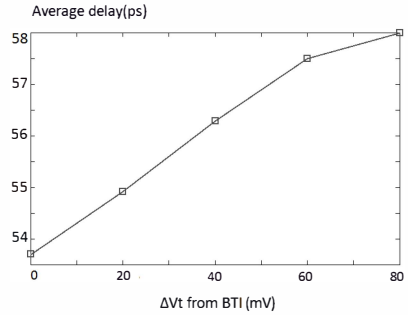

Figure 7 Average delay after each stress step

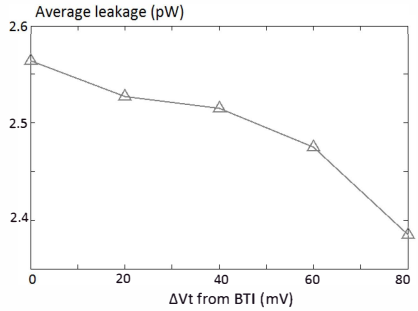

Figure 8 Average leakage after each stress step

Increasing the threshold voltage of the stressed devices has a few other effects to consider beyond simply reducing offset. Specifically, the BTI effect lowers V_T, so it decreases the leakage power but has the downside of degrading the sense amp speed. Figure 7 shows the average delay after each stress step for the same Monte Carlo simulation scenario as before. The average delay increases slightly due to the higher threshold voltage on one side of the SA, although this delay may be easily compensated by the speedup that is enabled by a reduction in offset of the worst cells. Figure 8 shows the average of the total leakage power after each stress step, which decreases due to higher V_Ts in the stressed devices.

IV. 120nm Test Chip Measurements

We applied the proposed scheme to a test chip that contains an array of SAs to demonstrate how BTI can improve offset. The chip is fabricated in 120nm technology and contains 15,360 sense amplifiers arranged in an array to simplify testing. To verify the scheme, the chip was stressed at 1.7× of the nominal V_{DD} and 45°C for 12 hours, and measurement of the offset voltage was performed every 4 hours. Due to the structure of the test chip, all SAs had to receive stress in the same direction. This means that the offset should improve for roughly half of the SAs and degrade for the other half. Another way to say this is that the offset distribution of all the cells will shift in one direction. Figure 9 shows the initial and final distribution of the offset voltage. Figure 10 shows the average offset voltage after each stress step. The stress has the expected effect of reducing offset in the anticipated direction. By applying the feedback and reset scheme proposed above, we can reduce the offset of all of the SAs. The absolute amount of offset improvement was not large, but the PBTI

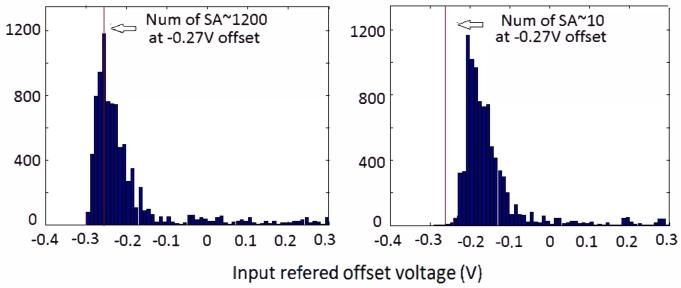

Figure 9. a. Initial distribution of the measured offset voltage b. Final distribution of the measured offset voltage after stress.

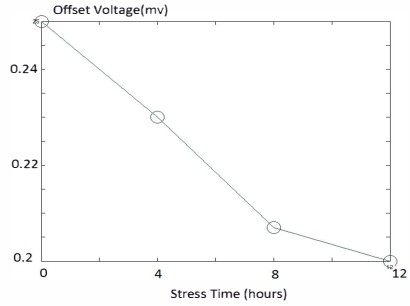

Figure 10. Average measured offset voltage after each stress time.

effect (in NMOS) is not large in 120nm. For newer technologies, both NBTI and PBTI are much more pronounced, so shorter stress events would produce more substantial improvements.

V. Conclusion

We presented a scheme that uses the typically detrimental aging effect to improve the SRAM sense amplifier offset. Offset compensation of 50mv was achieved using stress of 1.7× of the nominal VDD and 45°C for 12 hours. It can be periodically used through the life time of the chip to offset variation from real-time aging and could be easily integrated with other compensation techniques as an initial step to reduce the offset variations.

VI. References

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