A 10 mV-Input Boost Converter With Inductor Peak Current Control and Zero Detection for Thermoelectric and Solar Energy Harvesting With 220 mV Cold-Start and −14.5 dBm, 915 MHz RF Kick-Start

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***Abstract*—A boost converter for thermoelectric energy harvesting in 130 nm CMOS achieves energy harvesting from a 10 mV input, which allows wearable body sensors to continue operation with low thermal gradients. The design uses a peak inductor current control scheme and duty cycled, offset compensated comparators to maintain high efficiency across a broad range of input and output voltages. The measured efficiency ranges from 53% at $V_I = 20$ mV to a peak efficiency of 83% at $V_I = 300$ mV. A cold-start circuit starts the operation of the boost converter from 220 mV, and an RF kick-start circuits starts it from −14.5 dBm at 915 MHz RF power.**

***Index Terms*—Boost converter, DC-DC converter, energy harvesting, low voltage, solar energy harvesting, thermal-electric, ultra-low power.**

I. Introduction

ULTRA-LOW-POWER (ULP) wireless sensors for the emerging internet of things (IoT) often rely on harvested energy from ambient sources with small output voltages [1] and lower power. The power from a solar cell in indoor lighting can be only a few μW [2]. For wearable applications the thermal gradient between skin and air, especially under clothing, may only be a few °C, and the challenge of matching thermal impedances in the harvester packaging may leave thermoelectric generators (TEGs) with <1°C, which results in open circuit TEG outputs voltage of less than 30 mV. Recently several energy harvesting boost converters have been presented to harvest energy from lower voltage, lower power sources for ULP applications. A boost converter circuit that can harvest with allowable input voltage (V_I) down to 20 mV [3] achieves a maximum efficiency of 46% at 20 mV. It also needs an initial pre-charge voltage from an external source (for example, a battery) to kick-start the boost converter. Further, the design does not employ a maximum power point (MPP) tracking scheme to match the impedance of the energy harvester. A boost converter that can startup at 35 mV [4] with the help of a mechanical switch can harvest from 25 mV V_I. It achieves a peak end-to-end efficiency of 58%. A self-starting battery-charger IC [5] can startup from 330 mV and achieves an efficiency of 80% at 0.5 V V_I. To reduce the startup voltage of the boost converter, a transformer based startup mechanism is presented in [6]. It achieves a minimum startup voltage of 40 mV. However, use of the transformer increases the size of the system. Further, the re-use of the transformer as an inductor for boost conversion adversely affects the maximum achievable efficiency, which is 61% [6]. This paper focuses on the challenge of harvesting from lower V_I. Harvesting from low V_I faces several key challenges; low input power demands ultra-low power circuits for good efficiency. The inductor peak current (I_P) needs to be controlled properly for maximizing efficiency. The control circuits for the boost converter need to be controlled for mismatch which makes the small V_I hard to detect and use accurately. Mismatch can also cause significant variation in the peak inductor current (I_P), and accurate zero detection typically requires high current comparators. Further, the system needs a lower startup voltage.

This paper presents a boost converter capable of harvesting from V_I down to below 10 mV at efficiencies that are 7% higher than prior work [10]. A voltage-insensitive constant I_P control circuit, maximum power point (MPP) tracking, an integrated CMOS cold-start circuit from 220 mV, a parallel RF kick-start circuit that enables operation from a −14.5 dBm, 915 MHz RF signal, and the combination of offset compensation with duty cycled comparators enable these results and give efficiencies from 53% at a 20 mV V_I to 83% at 0.3 V V_I.

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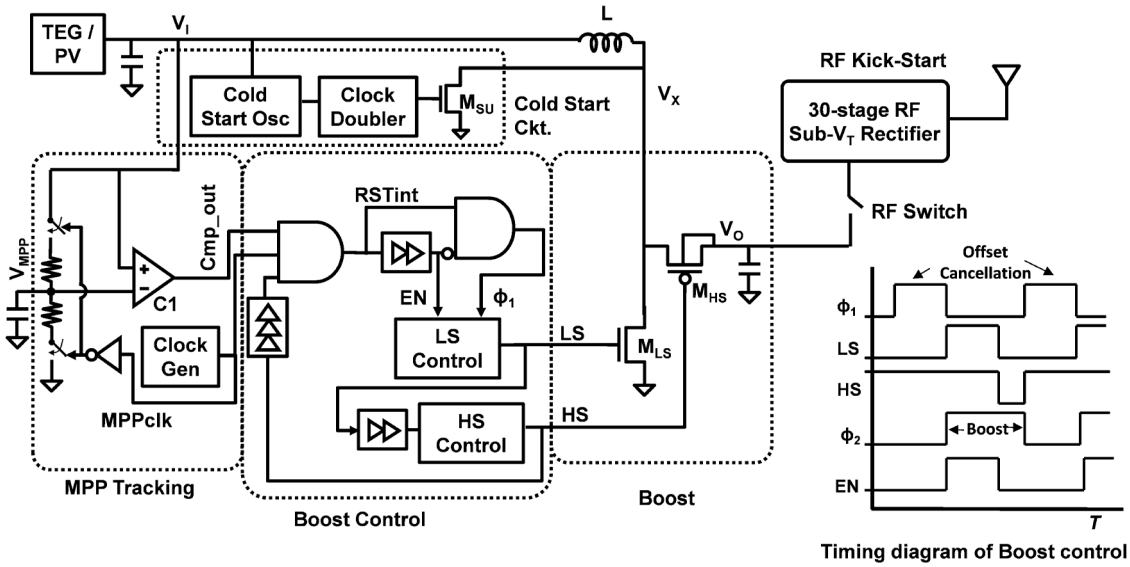


Fig. 1. Complete architecture and timing diagram of the boost converter.

II. Architecture of the Boost Converter

Fig. 1 shows the architecture and the timing diagram of the boost converter. It comprises a MPP tracking circuit, a cold-start circuit, a circuit to generate three phases of timing control, the conventional High Side (HS) and Low Side (LS) boost converter switches, and an RF kick-start circuit to startup from RF power. The boost converter can startup alternatively from the cold-start circuit which uses an oscillator and a voltage doubler circuit to cold-start from 220 mV. After startup, the boost converter operates in the normal mode where the boost converter makes use of a MPP tracking circuit to operate the converter at MPP. The boost control circuit generates three non-overlapping phases, ϕ_1, LS, and HS. In a conventional boost converter the switching cycle consists of LS and HS phases only. We add the extra phase, ϕ_1, for LS control and for offset compensation throughout the design. The ϕ_1 pulse width is set by a delay line. A peak inductor current control circuit is used to set the peak current, which maximizes the efficiency of the converter. The pulse width of the LS switch is set by the LS controller. A HS controller is used to control the HS switch to turn it off once the inductor current crosses zero during the high side charge transfer of the converter.

A. MPP Tracking and Control of the Boost Converter

The MPP of ambient harvesters such as solar cells and TEGs exists at fixed ratio (MPP coefficient, K) of the harvester's open circuit voltage. The MPP of a solar cell exists at 73% to 80% of PV's open circuit voltage [12], while for a TEG the MPP is at 50% of its open circuit voltage [11]. Since, the MPP varies with ambient conditions such as change in insolation levels or change in temperature, MPP tracking circuits are used to continuously track the MPP. In this work, we implement a constant voltage MPP tracking scheme [13] because of its suitability for low power applications. Fig. 2 shows the maximum power point tracking circuit for the energy harvester connecting to the boost converter. It consists of an MPP sampling circuit, a comparator C1, and a clock generator. The MPP sampling circuit samples the ratio of open circuit voltage at $\mathrm{V_I}$ and stores it on the cap. The clock generator generates a clock with a typical period of $\sim$2.4 s, which is fast enough to track the slow changing ambient condition, and the leakage of the MPP capacitor $\mathrm{C_M}$. Fig. 3(a) shows simulation of MPPT circuit with a fast MPP clock of 150 ms and a sampling pulse of 10 ms. When this pulse goes low, the boost converter is disabled, disabling the load at the output of the harvester which goes to its open circuit voltage. The MPP pulse is also used to close the switches $\mathrm{S_1}$ and $\mathrm{S_2}$, as shown in Fig. 2. The two resistors, $\mathrm{R_1}$ and $\mathrm{R_2}$ get connected to $\mathrm{V_I}$, and the $\mathrm{V_{MPP}}$ node goes to the voltage $\mathrm{R_1/(R_1+R_2)^*V_I}$, where $\mathrm{R_1}$ and $\mathrm{R_2}$ can be selected based on the MPP coefficient.

Fig. 3 shows the simulation result of the MPP tracking circuit. A comparator is used in a feedback loop to regulate $\mathrm{V_I}$ and maintain it close to the MPP. This way the output voltage of the harvester is maintained at its MPP with a small ripple. The amount of ripple is a function of the capacitor $\mathrm{C_I}$ connected at the output of the harvester. The ripple is made small by using a 5 μF capacitor at $\mathrm{V_I}$. Further, the comparator regulates the input voltage $\mathrm{V_I}$ and it needs to be continuous time and low power. We use a comparator with a quiescent current of 5 nA. Fig. 3(b) shows the simulation of the MPP tracking scheme with a fast MPP clock with the open circuit voltage of the harvester varying from 300 mV to 200 mV in 100 ms.

III. LS Timing Control

Owing to the low output power of the ambient sources, it is more efficient to operate the boost converter in discontinuous conduction mode (DCM). Fig. 4 shows the circuit operation of LS and HS switching in a boost converter operating in DCM. In the LS switching, the inductor current rises from zero to a peak value $(\mathrm{I_P})$, which is discharged onto $\mathrm{C_L}$ in the HS phase. The efficiency of the boost converter is limited by the switching loss energy $(\mathrm{E_{SW}})$ in the switches and control circuit, static

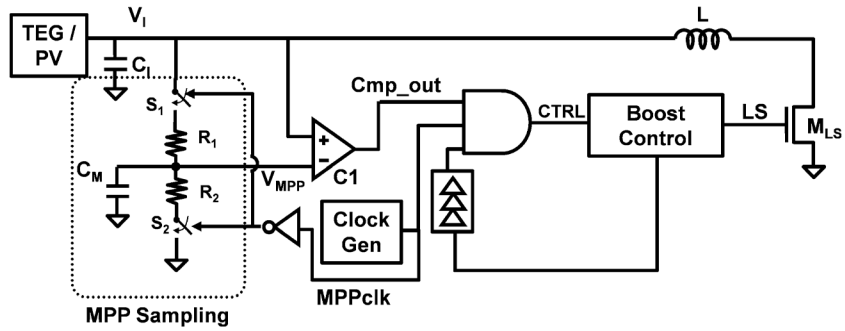


Fig. 2. Maximum power point tracking and control implementation of the boost converter.

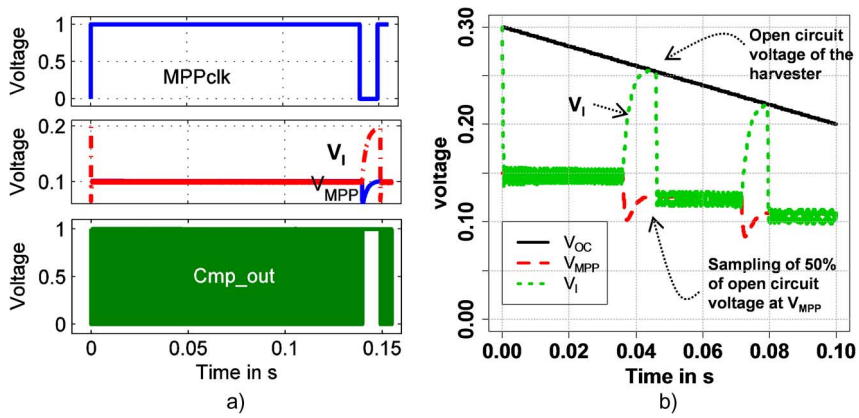


Fig. 3. Simulation result of MPP tracking scheme showing tracking at 300–200 mV input voltage. (a) Simulation result of MPP tracking. (b) Simulation MPP tracking w/ changing MPP point.

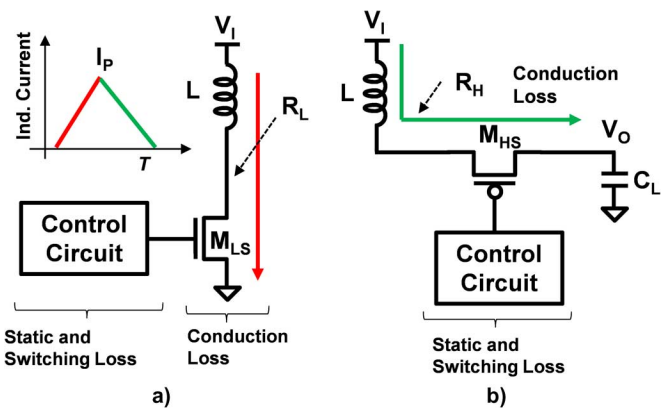


Fig. 4. LS and HS switching operation of the boost converter. (a) Low Side switching. (b) High Side switching.

loss (E_{ST}) due to bias currents, and conduction loss (E_{CN}) in the resistance of the switches. The E_{ST} and E_{SW} are generally constants for a given architecture and fixed switch sizes, while the conduction loss depends on I_P. The efficiency depends on I_P as the following analysis describes.

A. Efficiency Dependence on Peak Inductor Current

The total energy loss in a boost converter can be given as

$$E_L = E_{ST} + E_{SW} + E_{CN}. \tag{1}$$

E_{CN} has two components, $E_{CN,L}$ and $E_{CN,H}$ for LS and HS conduction loss. For the LS switching, assuming that the switch resistance is small, we can write inductor current as

$$L\frac{di}{dt} = V_I. \tag{2}$$

For LS switching time T_{LS}, the heat loss can be written as (assuming LS resistance is R_L)

$$E_{CN,L} = \int_0^{T_{LS}} i^2 R_L dt. \tag{3}$$

Changing (3) to a current integral using (2),

$$E_{CN,L} = \int_0^{I_P} i^2 R_L \frac{L}{V_I} di = \frac{L R_L I_P^3}{3V_I} \tag{4}$$

where I_P is the peak inductor current at $t = T_{LS}$. Similarly, the HS conduction loss is obtained as

$$E_{CN,H} = \frac{L R_H I_P^3}{3(V_O - V_I)}. \tag{5}$$

The total conduction loss is given by

$$E_{CN} = E_{CN,H} + E_{CN,L} = \frac{L}{3}\left(\frac{R_H}{V_O - V_I} + \frac{R_L}{V_I}\right) I_P^3. \tag{6}$$

Since V_I can be small for this design, R_L should also be small to minimize E_{CN}. Further, for $V_O \gg V_I$, E_{CN} can be given

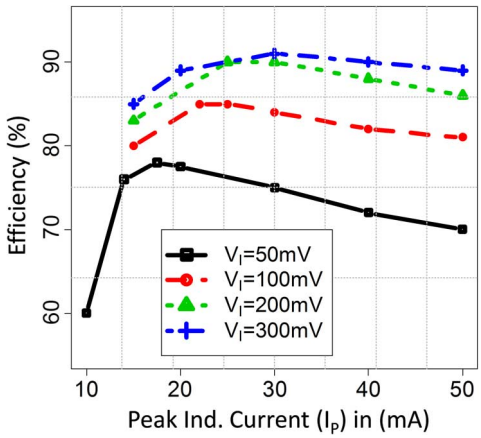


Fig. 5. Efficiency variation of the peak inductor current (I_P) with V_I shows that I_P for maximum efficiency increases with V_I.

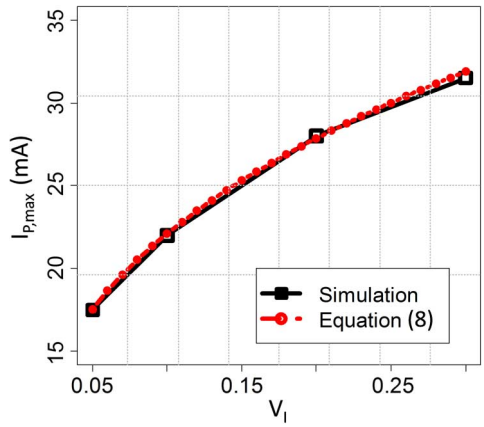


Fig. 6. Comparison of variation of $I_{P,max}$ with V_I in simulation and as proposed in (8).

by (4). Since $0.5LI_P^2$ is the energy transferred in each cycle (assuming low losses), the efficiency losses (η_L) as a percent can be written as

$$\eta_L = \frac{E_L}{0.5LI_p^2} = \frac{E_{ST}+E_{SW}}{0.5LI_p^2} + \frac{R_L I_P}{1.5V_I}. \quad (7)$$

η_L represents the losses in the converter as a percent which needs to be minimized to maximize the efficiency (η) of the converter. η_L has a minimum which can be obtained by differentiating (7) with respect to I_P and the corresponding I_P which maximizes efficiency is given by

$$I_{P,max} = \left[\frac{6(E_{ST}+E_{SW})V_I}{LR_L}\right]^{\frac{1}{3}}. \quad (8)$$

Equation (8) also shows that $I_{P,max}$ decreases with V_I. The value of I_P needs to be controlled as given by (8) with respect to V_I to achieve the maximum efficiency in the converter. Fig. 5 shows the simulation result where the I_P was varied for different V_I. The values for E_{ST}, E_{SW}, and R_L are found from simulation to be 1.5 pJ, 99 pJ, and 0.269 Ω (with estimated layout parasitic including the inductor's DCR). A 20 μH inductor is used for the simulation set-up. Fig. 5 shows that at higher values of I_P, η decreases linearly, and at lower values of I_P, it rolls off quickly due to the quadratic dependence as shown in (7). Further, the maximum efficiency peak inductor current ($I_{P,max}$) was plotted as a function of V_I and compared with the proposed equation (8). Fig. 6 shows that (8) predicts the optimized $I_{P,max}$ with less than 3% error.

B. LS Timing Control Circuit for I_P

In the preceding section, we showed that by controlling the peak inductor current, the efficiency of the boost converter can be maximized. In the conventional approach, the resistance of the switch (MOS transistor) is used to measure the I_P. The drop across the LS transistor M_{LS}, when the low-side is turned on, is the representation of I_P and is used to control I_P. However, this method is sensitive to mismatch and can result in ±20%–40% error in the peak inductor current [15]. Another approach is to keep LS on for a fixed time [3], [4] to control the peak inductor current. This method is not expensive in terms of power. However, the efficiency can be reduced because the inductor current is not very well controlled with varying V_I or V_O. Also, the process variation can result in a variation of the peak current, further impacting the efficiency of the converter. In this section we propose a low power control scheme to control the peak inductor current for the boost converter. We also propose digital control bits to control the process variation.

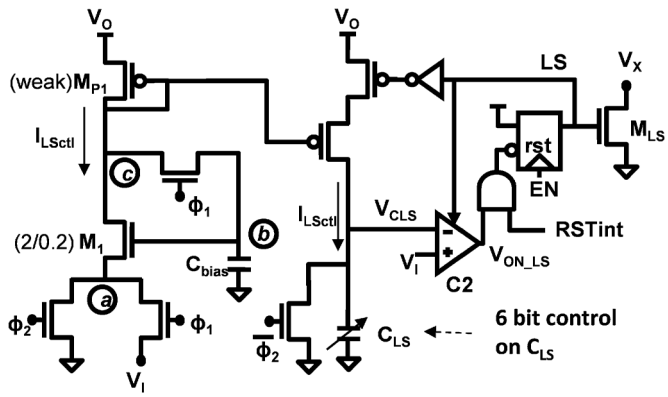


Fig. 7. The Low Side (LS) timing control circuit sets I_P independently from V_I or V_O to maximize efficiency.

TABLE I
OPERATION OF LS CONTROL CIRCUIT IN PHASE ϕ_1 AND ϕ_2

Phase	Node-*a*	Node-*b*	I_{LSctl}
φ_1	V_I	V_I+V_{TM1}	-
φ_1	-	V_I+V_{TM1}	$\propto(V_I+V_{TM1}-V_{TM1})^2$ $\propto(V_I)^2$

Fig. 7 shows the circuit that is used for generating peak inductor current for LS timing. Table I shows the configuration of the circuit in phase ϕ_1 and ϕ_2. The functioning of this circuit is explained with the help of the timing diagram shown in Fig. 8(a). During phase ϕ_1, node a is connected to V_I, the output

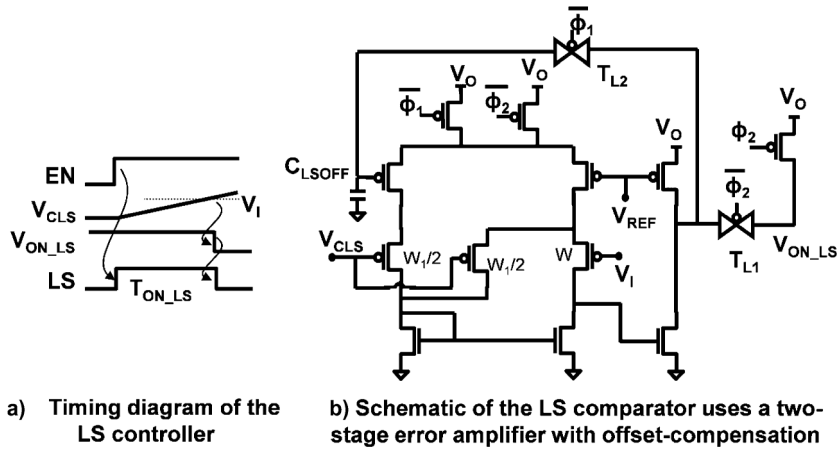


Fig. 8. (a) Timing diagram of the LS control circuit. (b) Schematic of the LS comparator C2.

of the energy harvester, V_{CLS} is held to ground, and comparator C2 is disabled. The output of LS is set to ground. The transistor M_{P1} is made weak, which sets the output voltage of node b and is given by $V_I + V_{TM1}$, where V_{TM1} is the threshold voltage of the transistor M_1. Weak M_{P1} drives M_1 very close to its threshold voltage. In phase ϕ_2, node a is connected to ground, while the connections between b and c are removed. The transistor M_1 is designed to be in saturation and sets the current I_{LSctl} which is given by

$$I_{LSctl} = k * (V_I + V_{TM1} - V_{TM1})^2$$
$$I_{LSctl} = k * (V_I)^2. \quad (9)$$

The current generated for LS control is made proportional to the square of the input voltage V_I. This current is mirrored to charge the capacitor C_{LS}. Once ϕ_2 goes high, LS goes high, and the capacitor starts charging. Once the capacitor C_{LS} crosses V_I, output of the comparator C1 goes low, which resets the D-flip-flop and brings LS to ground. Fig. 8(a) shows the timing diagram for the generation of LS. The timing of LS is given by

$$I_{LSctl} = C_{LS}\frac{dv}{dt}$$

as the capacitor charges from 0 to V_I and using (9), we get

$$T_{ON_LS} = C_{LS}\frac{V_I}{I_{LSctl}} = \frac{C_{LS}}{kV_I}. \quad (10)$$

This is the time for which the inductor is kept on. It increases as V_I decreases. Now, let us find out how the peak inductor current is obtained. Assuming negligible drop across M_{LS}, we can write the basic equation for inductor as

$$L\frac{di}{dt} = V_I.$$

The inductor current charges from 0 to I_P during the time LS is on.

$$So, \quad I_p = \frac{V_I T_{ON_LS}}{L}.$$

Using (10), we get

$$I_P = \frac{C_{LS}}{kL}. \quad (11)$$

Equation (11) gives the formula for peak inductor current. The expression shows that the I_P is independent of V_I and V_O voltages. It depends on the value of the capacitance C_{LS} and the inductor value L. By controlling the value of C_{LS}, peak inductor current can be set to a constant value, which targets the maximum efficiency, given by (8) and Fig. 5. The constant k in the expression is a function of process and temperature. As a result, the peak inductor becomes a function of variation in process. The value of I_P varies by 16% (21 mA to 25 mA) over a temperature range of 20°C to 60°C. Further, we also propose to address the variation using the capacitor C_{LS}. We use 6 bit binary control on the capacitor to address process variation. We perform the calibration of I_P by observing T_{ON_LS}. The value of T_{ON_LS} for a given V_I is compared with a look-up table (LUT) for T_{ON_LS} obtained for the $I_{P,max}$ of that V_I given by (8). C_{LS} is changed to set the T_{ON_LS} given by the LUT to set I_P for maximum efficiency. Fig. 8(b) shows the circuit diagram of the LS comparator C2 utilizing a two-stage error amplifier with offset compensation. In phase ϕ_1, the offset of the comparator is compensated and stored on capacitor C_{LOFF}. The offset compensation technique is similar to the offset compensation in the HS comparator, which is discussed in the following section. In phase ϕ_2, the comparison between V_I and V_{CLS} is performed. Fig. 9 shows the simulation result of I_P in a 1000 point Monte-Carlo simulation with process and mismatch variation at 250 mV V_I. Simulation result shows a mean

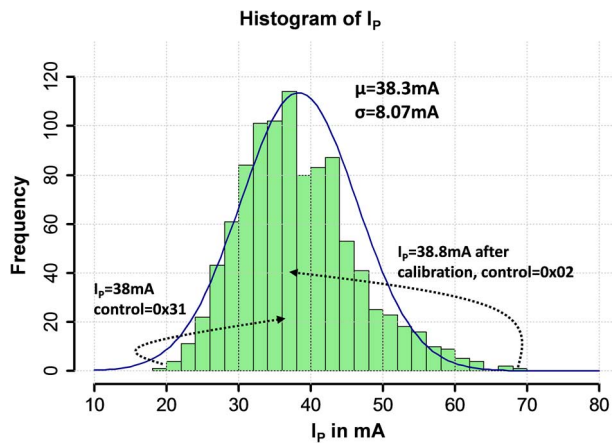


Fig. 9. Statistical distribution of I_P in a 1000 Monte-Carlo (process and mismatch variation) simulation with $V_I = 250$ mV.

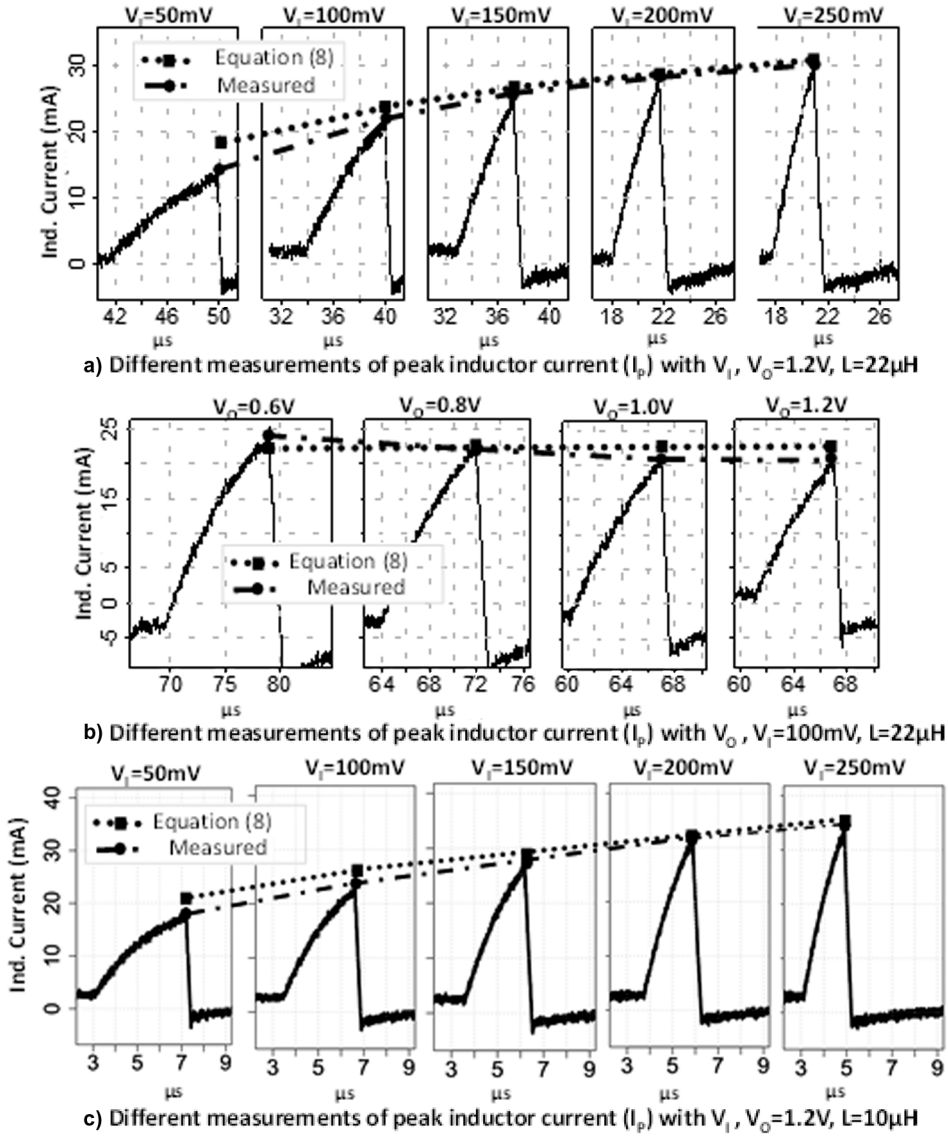


Fig. 10. Measurement results of peak inductor current: (a) variation with V_I with $L = 22\ \mu$H, (b) variation with V_O with $L = 22\ \mu$H, and (c) variation with V_I with $L = 10\ \mu$H shows that the LS control circuit tracks I_P based on (8) for maximum efficiency.

of 38.3 mA with a maximum of 70 mA and a minimum of 20 mA. Fig. 9 also shows that both the maximum and the minimum can be brought closer to the mean value of 38 mA by applying control bit of 0×31 for the minimum and 0×02 for the maximum I_P condition.

Equation (11) shows that I_P is independent of V_I. This is a first order derivation based on assumptions that the drop across LS switch M_{LS} is negligible compared to V_I. However, this assumption does not hold for lower values of V_I. Further, based on the derivation of (8), the value of I_P should decrease with V_I for lower values of V_I. In our proposed circuit, I_P does decrease with V_I due to the small voltage drop across M_{LS}, which we ignored initially to derive (2). This dependence is not the dependence required by (8). However, it does help to increase efficiency at lower values of V_I. We measured the peak inductor current for different inductor values and their corresponding $I_{P,max}$ (by programming C_{LS}). Fig. 10 shows the measurement of I_P at different V_I and V_O. Fig. 10(a) shows the measurement of I_P with V_I while V_O is held constant at 1 V, using a 22 μH inductor with a DCR of 70 mΩ. The total LS resistance including board parasitic is close to 0.25 Ω. The inductor current will rise to 16 mA at 50 mV V_I if the switch and inductor are ideal. Fig. 10(a) shows that inductor current rises to 14.5 mA at 50 mV V_I. Fig. 10(a) also shows that I_P is within 15% of the value proposed by (8) at $V_I = 50$ mV and $<1\%$ at $V_I = 150$ mV or higher. Fig. 10(b) shows the measurement of I_P with V_O and V_I is constant at 100 mV. The value of I_P varies by $\sim$10% with the variation of V_O. Fig. 10(c) shows the measurement of I_P at different V_I with $L = 10\ \mu$H. The measurement shows less than 10% error at $V_I = 50$ mV when compared to equation (8). The variation of I_P across process is addressed by digitally tuning C_{LS} as described in the preceding section. C_{LS} can also be tuned for lower V_I operation as well to improve efficiency.

Further, the timing of LS is controlled by the comparator C2. The timing is given by capacitor C_{LS} charging from 0 to V_I

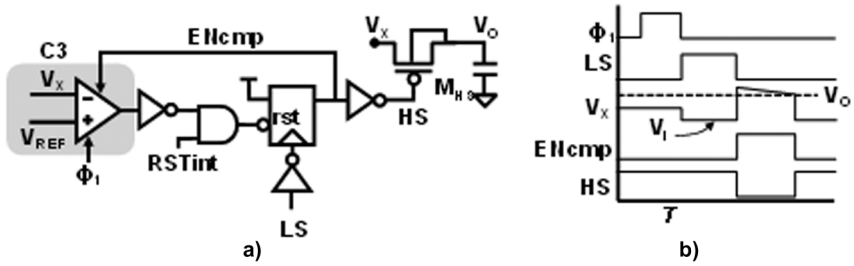


Fig. 11. Circuit to generate the HS timing using zero inductor current crossing. (a) Circuit diagram of HS control. (b) Timing diagram of HS control.

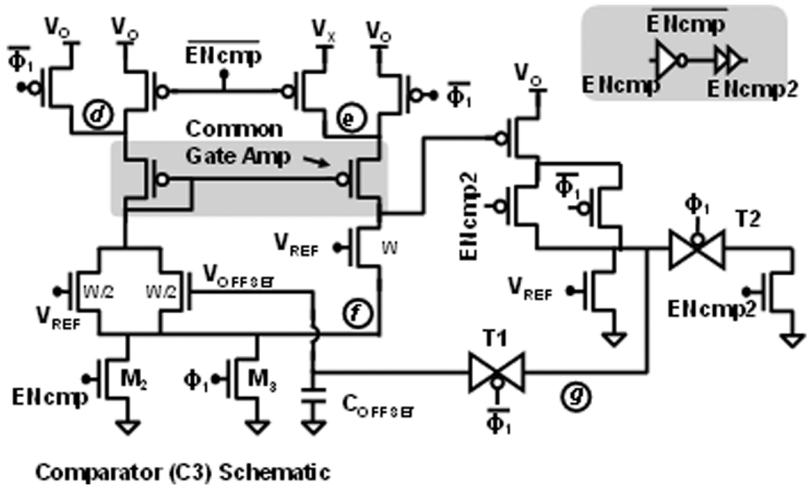


Fig. 12. High Side (HS) timing circuit with an offset-compensated (for offset $<$1 mV) and duty cycled (for low power) comparator.

using I_{LSctl}. When the comparator detects that $V_{CLS} > V_I$, it turns off the LS pulse. The offset in the comparator can introduce error in our required I_P value and can impact the performance of the converter significantly, particularly at low V_I values such as 10 mV. We compensate the offset of the comparator C2 in phase ϕ_2 which helps enable charging at voltages measured down to 10 mV. Fig. 8(b) shows the schematic of the comparator C2. The details of the offset compensation technique are covered in Section IV. The delay of the comparator C2 can also affect the LS timing, so its performance needs to be high. We use a 3 μA comparator to achieve the required performance and it is turned on only during the switching cycle. This circuit consumes no static power since the comparator is on only during times of high power transfer and high I_L, making its power a component of the switching loss.

IV. HS Timing Control

Fig. 11 shows the circuit for generating the HS timing using the zero detection. Comparator C3 is used to compare the V_X node with V_O. Once V_X crosses V_O and goes below it, the comparator output goes low and turns off the switch M_{HS}. Previous works on micro-power converters have considered comparator-based zero detection very high power [3], [4] and instead use a correction technique for zero crossing. In this work, we present the comparator based zero detection scheme as shown in Fig. 11. There are several challenges involved in designing zero detection comparator for a micro-power converters. First, the performance of the comparator needs to be very good. If the delay of the comparator is high, the exact timing of the HS control cannot be met. Second, the power consumption of the comparator needs to be small, as it will add to the loss in the boost converter. Finally, the mismatch between the devices in the comparator can result in high offset, which can alter the zero detection. This is particularly critical for harvesting from very low input voltage, as offset itself can be much higher than the input voltage V_I. Therefore, the offset due to mismatch needs to be cancelled. This work proposes a comparator that addresses these issues.

Fig. 12 shows the circuit diagram of the zero detection comparator. It uses a common gate amplifier, which is biased at $\sim$ 10 μA of quiescent current. The use of a common gate amplifier provides very good performance. However, this comparator cannot be always on as the static power consumption will degrade the efficiency of the boost converter. The comparator is duty-cycled and is turned on only when the switching happens. Fig. 11 shows that every time LS goes low, the output of D-flip-flop goes high, which powers up the comparator. The comparator detects the zero crossing and signals high which is used to reset the flip-flop, which powers off the comparator after zero detection is performed. Comparator C3 is on only during the switching cycle, making its power consumption a component of the switching loss. The power overhead because of the zero-detect comparator is greatly reduced. It reduces efficiency by only 4% at $V_I = 20$ mV and 0.4% at $V_I = 0.3$ V, but its high on-current ($\sim$ 10 μA) gives a fast response. While the performance and power issues are addressed as explained above, the circuit also addresses the offset issues. The offset in the

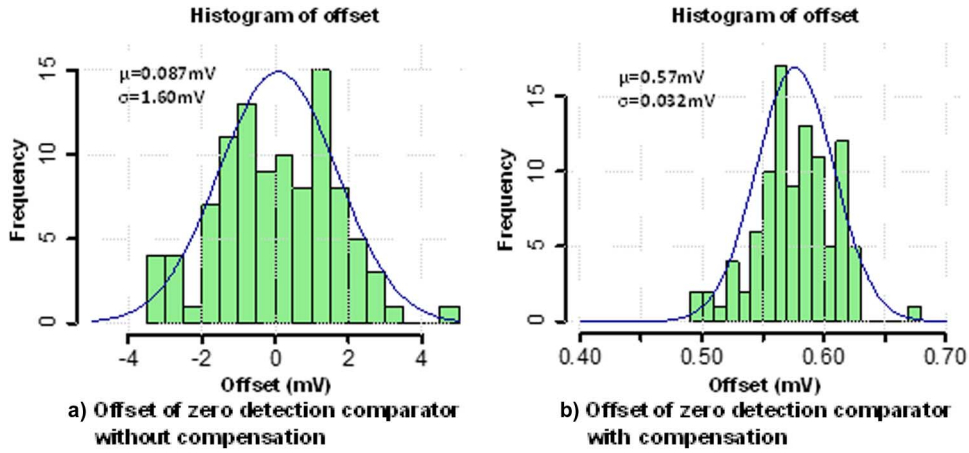


Fig. 13. 100 point mismatch simulation of the zero detection comparator. (a) Offset without the offset compensation technique shows a 3σ variation of ± 5 mV. (b) Offset with the offset compensation technique shows a $\pm 3\sigma$ variation of less than 1 mV.

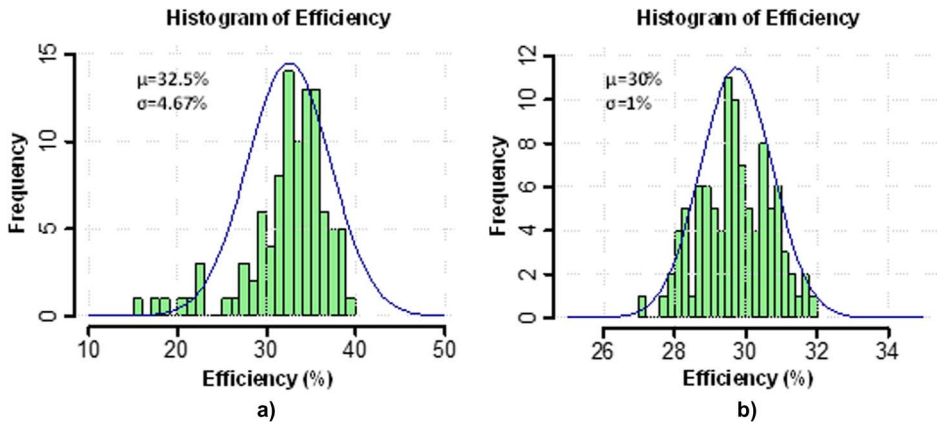


Fig. 14. 100 point mismatch simulation of efficiency of the boost converter at 10 mV V_I and 1 V V_O. (a) Efficiency without offset compensation zero-detection shows a minimum efficiency of 15%. (b) Efficiency with offset compensation zero-detection shows a minimum efficiency of 27%.

design is cancelled in phase ϕ_1 of the switching cycle as follows. In ϕ_1, nodes d and e are set at V_O while f is set at V_{SS}, and switch $T1$ is turned on while $T2$ is off. The feedback from node g sets V_{OFFSET} to remove offset in the comparator. If there is no offset in the design, $V_{OFFSET} = V_{REF}$. The measured comparator offset after compensation was <1 mV. Further, the feedback used for compensating the offset requires that the phase margin for the stable operation of the amplifier should be sufficient. This is addressed by properly choosing the size of C_{OFFSET}. The other comparators in the boost converter use a similar offset compensation circuit. After offset compensation, zero detection is performed in phase ϕ_2.

Fig. 13 shows the 100 point mismatch (only the devices in the zero detection comparator is selected for mismatch) simulation result of the zero-detection comparator C3. Fig. 13(a) shows that the offset in the comparator without the mismatch compensation technique shows a 3σ variation of ± 5 mV. A 1 mV offset corresponds to a 1 mA difference in inductor turn-off current. Fig. 13(b) shows that the offset in the comparator can be brought down to less than 1 mV with the proposed offset compensation technique. Fig. 14 shows the 100 point mismatch (only zero detection comparator is selected for mismatch) simulation result of the efficiency variation of the boost converter at 10 mV V_I and 1 V V_O. Fig. 14(a) shows that the efficiency of the boost converter without offset compensation in the zero detection. The minimum efficiency is 15% in this case. Fig. 14(b) shows that the minimum efficiency with offset-compensation is 27%. The offset compensation technique shows a 3σ improvement of 9% in the efficiency for the zero detection technique alone.

V. Startup Circuits

In this work, we support two startup mechanisms. A cold-start circuit can startup the boost converter from $V_I > 220$ mV. It uses a ring oscillator (RO) that runs on V_I to enable switching. Another startup mechanism is supported from RF. A 30-stage sub-threshold RF rectifier can charge V_O from -14.5 dBm RF input power at 915 MHz to kick-start the normal operation of the boost converter. We will now present the details of these circuits.

A. Cold-Start Circuit

Fig. 15 shows the cold-start circuit for the boost converter. It consists of a ring oscillator (RO) and a clock doubler circuit. When V_O is below 550 mV, the POR signal is low, which enables the RO on V_I. The RO can oscillate for $V_I > 200$ mV and generate non-overlapping signals p_1 and p_2. Signals p_1 and

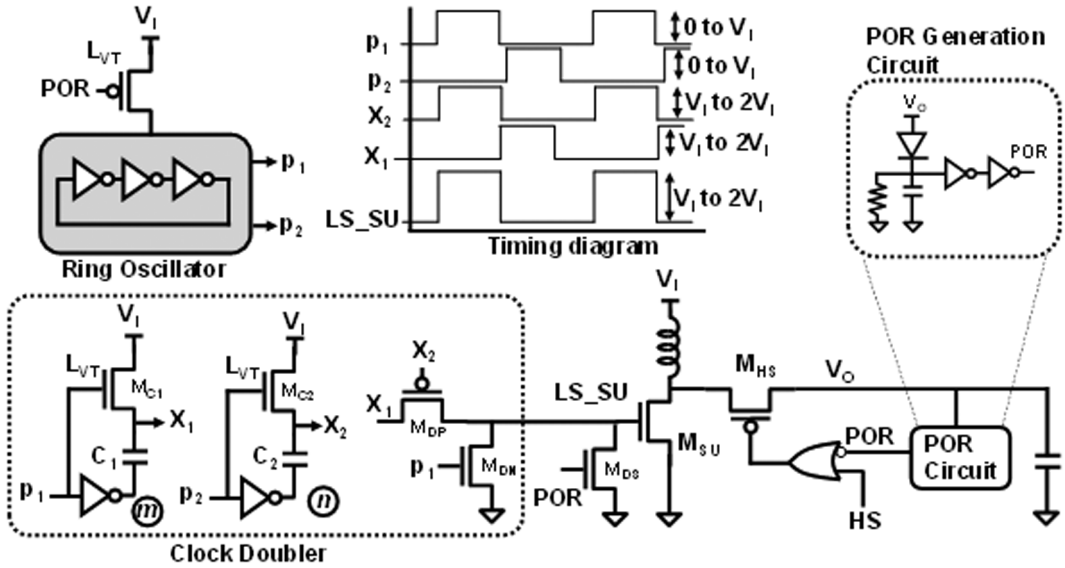


Fig. 15. Cold-start circuit for 220 mV startup using clock doubler.

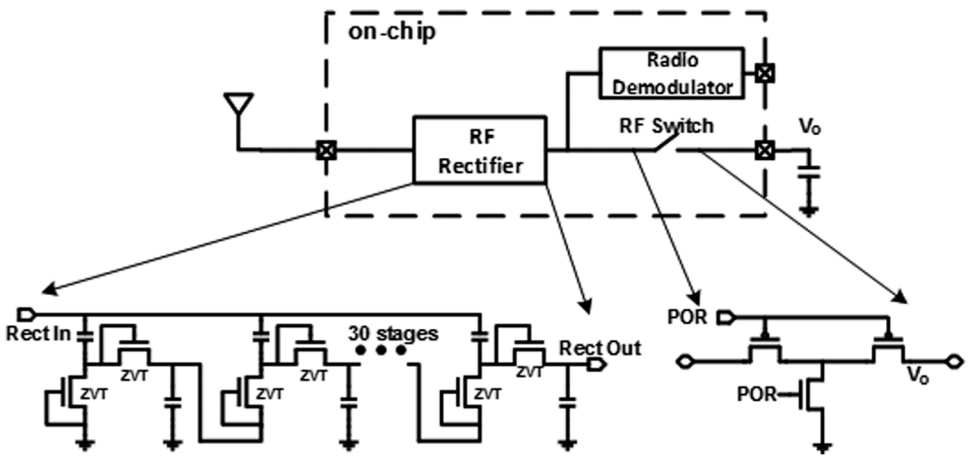
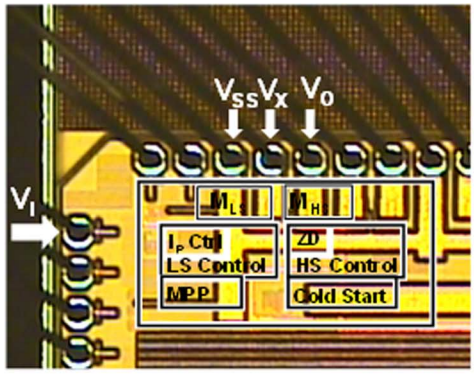


Fig. 16. RF kick-start circuit with RF switch.

p_2 go to the clock doubler circuit, which generates LS_SU to control the startup switch M_{SU}. Phase p_1 and p_2 are used in the clock doubler circuit to generate signals that swing from 0 to $2V_I$ (Fig. 15). The bottom plates of C_1 and C_2 are connected to the output of inverters driven by p_1 and p_2, and their top plates are driven by L_{VT} nMOSs whose drains are connected to V_I and gates to p_1 and p_2 respectively. The top plate of capacitors C_1 and C_2 will charge to V_I in the absence of switching. The bottom plate of C_1 and C_2 swing from 0 to V_I when switching, and the top plate swings ideally from V_I to 2 V_I as shown in Fig. 15. Next, we convert to signals with full 0 to 2 V_I swing. When p_1 is high, X_2 is also high, so LS_SU is pulled down to ground. When p1 is at 0, X_2 is at V_I and X_1 is at 2 V_I. The pMOS transistor will turn on and pass the X_1 level to LS_SU, which ideally swings from 0 to 2 V_I (in reality, the output voltage is below but close to 2 V_I because of the switching losses involved). The increased swing is used for inductor switching to charge V_O. In this configuration the inductor current is not controlled and is restricted by the switch resistance. The HS control is disabled, and the circuit uses M_{HS} in diode configuration to pass high. This switching path is not efficient, but it charges V_O without adding load to it. Once V_O reaches voltage greater than 550 mV, the POR signal goes high enabling the normal operation of the boost converter. The POR signal goes high and disables RO and pulls down the gate of MSU to ground, disabling the cold-start switching.

B. RF Kick-Start Circuit

in with fast charging time. The RF kick-start circuit provides a kick-start from RF energy and consists of a broadband RF rectifier and an RF switch, as shown in Fig. 16. The input sensitivity of the rectifier is -32 dBm with no load [18] and an RF matching network. In this boost converter design the off-chip RF matching network was not used to enable startup from different RF frequencies. Further, during startup, the V_O voltage sees a load of 200 nA to power the bias and control circuits for the boost converter. The measured sensitivity of the rectifier at 915 MHz RF signal is -14.5 dBm with a 200 nA load at V_O. The rectifier's structure is the same as the Dickson multiplier, with the exception that all transistors operate in



Die photograph of the boost converter.

Resistance breakdown of LS

Parameter	Value
Technology	130nm bulk CMOS
Total area	600 µm x 200 µm
Inductor value	L=10 µH
V_{IN}-to-V_{SS} LS resistance	300 mΩ (Target)
Inductor DCR	70 mΩ
Bondwire	50 mΩ (1mm,1mil,gold)
NMOS Res	120 mΩ
Layout parasitic	60 mΩ

Fig. 17. Implementation of the boost converter.

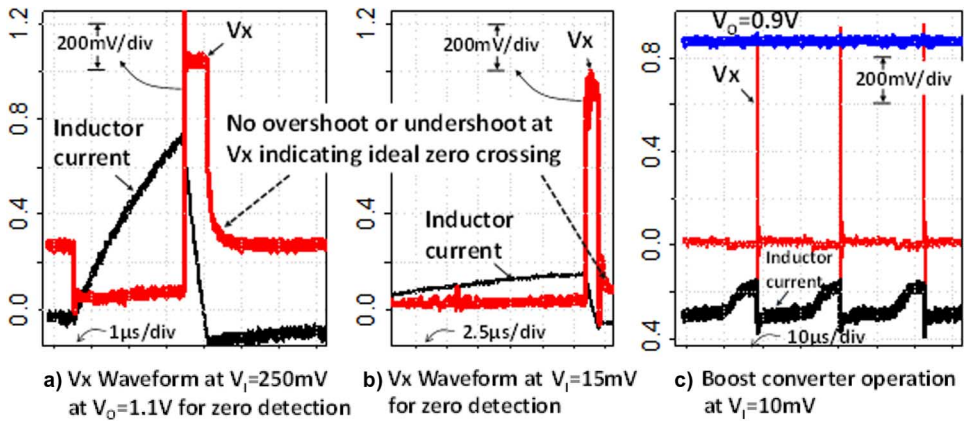


Fig. 18. Inductor switching waveforms: (a) Vx at $V_I = 250$ mV and (b) $V_I = 15$ mV showing near ideal zero crossing. (c) Switching operation at 10 mV.

the sub-threshold regime. The rectifier needs to operate in the subthreshold region to harvest RF power from very low inputs and the output voltage. This subthreshold rectifier uses zero-threshold transistors and 30 stages to achieve sufficient RF ga

An RF switch is required because the RF rectifier is used both for the RF kick-start and as an RF front-end of a low power radio. The RF switch is turned on during kick-start mode when output voltage V_O is lower than POR threshold voltage and normal boost operation is disabled. Fig. 16 shows the circuit diagram of RF switch. During kick-start mode POR is low and V_O is connected with Rect_Out. V_O starts rising with the incoming RF signal. Once the voltage crosses 550 mV, POR goes high and the RF switch is turned off. The rectifier can be used for the RF front end now. The RF switch provides a ground shielding to prevent the noise from the boost converter to propagate into the rectifier output.

VI. Measurement Results

The chip was fabricated in 130 nm bulk CMOS. Fig. 17 shows the implementation of the boost converter where it consumes 0.15 mm^2. A low power lower voltage bandgap reference circuit which can provide reference voltage from 0.5 V [17] V_O is used for generating the reference voltage for the boost converter. The area of the bandgap reference circuit is 0.03 mm^2. The LS resistance, which is critical for efficiency at low voltages has a designed value of 0.3 Ω including layout and component parasitic. The value of the inductor used in our measurement set-up is 10 μH, the output capacitor at V_{CAP} is greater than 100 μF, and the capacitor at the input of V_I is 5 μF. The output of the boost converter will be used as a storage node for storing energy in a typical IoT application. A clamp circuit is used to clamp the output voltage of the converter. Fig. 18(a) and (b) shows the measurement of V_X at the inductor current zero crossing. Node V_X does not have overshoots or undershoots at the zero crossing which indicates near-ideal zero detection using our offset compensated ZD comparator. Fig. 18(c) shows measurement of boost converter operation at $V_I = 10$ mV with a 5 μA load at the output. Fig. 19(a) shows the measurement of boost converter operation from cold start. In this measurement, V_I was set at 250 mV for cold start. After cold start, V_I is slowly decreased to 20 mV. The measurement shows operation at 20 mV. Fig. 19(b) shows the measurement of MPP operation at $V_I = 50$ mV in the open circuit configuration with a 10 Ω source resistance. V_I quickly reaches 25 mV, operating the converter at the source's MPP. The minimum cold-start voltage was measured at 220 mV with an instantaneous power consumption of 308 μW during cold-start. The minimum measured operating V_I is <10 mV. The tracking efficiency at 20 mV open circuit voltage and 5 Ω of series resistance is 92%, and it increases to 99% at 100 mV of open circuit voltage. The boost

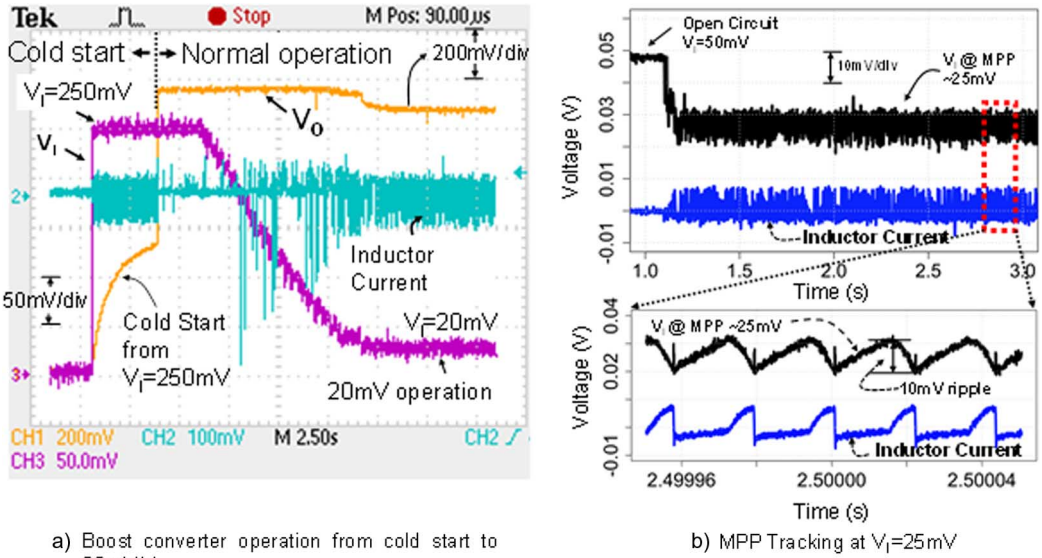


Fig. 19. (a) Boost converter operation from cold start at 250 mV to operation at 20 mV V_I. (b) MPP tracking of the boost converter circuit at an MPP of 25 mV using a source with an open circuit voltage of 50 mV and a source resistance 10 Ω.

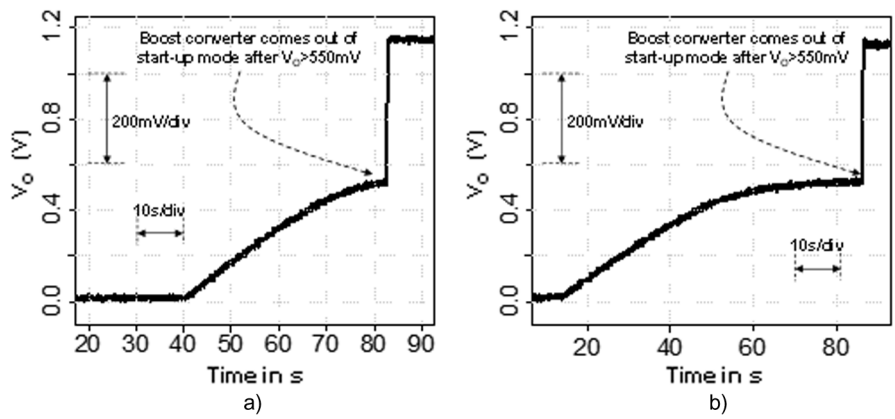


Fig. 20. Measurement of RF kick-start of the boost converter. (a) RF kick-start with a 915 MHz RF signal and an input power level at −14.5 dBm. (b) RF kick-start with a 2.45 GHz RF signal and an input power level at −8.5 dBm.

converter circuit can supply a peak power of 22 mW at the output for a V_I of 0.3 V. Fig. 20 shows the measurement of the RF kick-start circuit. In this set-up, V_O was completely discharged, and V_I was connected to 50 mV, and an output load of 5 MΩ is connected at V_O. Since V_I is too low for cold-start, V_O will not charge from V_I. Fig. 20(a) shows the measurement of RF kick-start when an RF signal of 915 MHz is applied at the RF_{IN} (Fig. 16). V_O goes to 550 mV with an input RF power of −14.5 dBm. Fig. 20(b) shows the result with a 2.45 GHz RF signal. At 2.45 GHz, an input RF power of −8.5 dBm or more is needed for kick-start operation. In our set-up, a matching network for the RF signal is not used, and so the sensitivity of RF signal for kick-start is lower. The kick-start circuit will startup at even lower input RF power if a matching network for the RF signal is used. Fig. 21 shows that efficiency of the boost converter ranges from 21% at $V_I = 10$ mV to 83% at $V_I = 0.3$ V and $V_O = 1.1$ V. We also measured the boost converter performance with a TEG (Laird 430857-500). The resistance of the part is 2 Ω. We measured the boost converter in an application

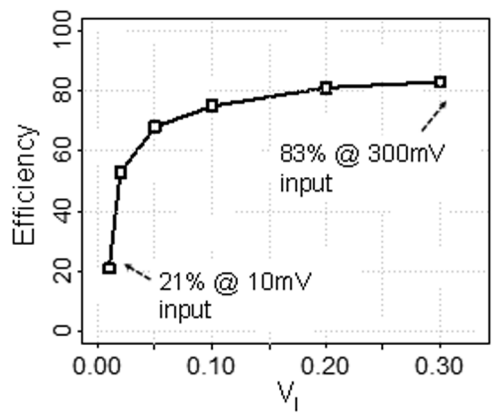


Fig. 21. Measured efficiency of the boost converter with V_I at V_O of 1.1 V.

set-up where the TEG was put on a human hand with one side exposed to ambient, and it produced an open circuit voltage of

TABLE II
COMPARISON WITH STATE-OF-THE-ART ENERGY HARVESTER CIRCUITS

	This work	[3]	[4]	[5]	[6]
Harvesting	TEG/Solar	TEG	TEG	TEG/Solar	TEG
Min. V_I	10mV	20mV	25mV	-	40mV
Cold-Start V_I voltage	220mV	600mV	35 mV w/ mech. kick	330mV	40mV w/ X-former
RF Kick-Start	-14.5dBm @915MHz	✗	✗	✗	✗
IDDQ	300nW	~1μW	-	~330nA	-
IP Control	✓	✗	✗	✗	✗
MPP tracking	✓	✗	✓	✓	✓
η @ V_I	83% at 0.3V	75% at 0.1V	58% at 0.1V (end-end)	80% at 0.5V	61% at 0.3V (end-end)
η at low V_I	53% at 20mV	46% at 20mV	-	-	30% at 50mV
Technology	130nm	130nm	350nm	-	130nm

40 mV. The functionality and performance of the boost converter was also tested with a photo-voltaic cell with an open-circuit voltage of 540 mV. Table II compares this work with previously reported micro-power boost converters for low input voltages. Our work reports harvesting from the lowest input voltage at 10 mV, with an efficiency of 21%. Our static power consumption is 300 nW, and the circuits are designed in 130 nm. We support two startup methods. The cold-start does not require external assistance and starts operation from 220 mV V_I, which is 110 mV lower than in [5]. Further, we also support startup using 915 MHz and 2.4 GHz RF signals.

VII. CONCLUSION

A thermoelectric boost converter combines an I_P control scheme with offset compensation and duty cycled comparators to enable energy harvesting from TEG/solar cell inputs as low as 10 mV, 50% lower than prior work. Controlling the I_P allows the converter to sustain high efficiency across a broad V_I range, achieving 53% and 83% efficiency at 20 mV and 300 mV, respectively, which improves on prior designs. A cold-start circuit enables operation from 220 mV, 110 mV lower than previous work [5]. Further, the design supports constant voltage MPP tracking and startup from 915 MHz and 2.45 GHz RF signals. These features allow the converter to extend the operating window for thermal harvesting with low thermal gradients, which is ideal for body worn sensors.

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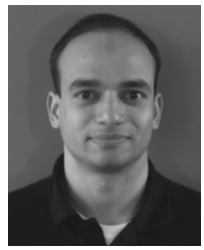

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