Combined SRAM Read/Write Assist Techniques for Near/Sub-Threshold Voltage Operation

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Internet of Things
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Source: A. Klinefelter, ISSCC 2015

IoT specific SoCs harvest energy and operate in sub-threshold to reduce energy/power consumption
Internet of Things

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Memory consumes a significant portion of the digital power.
Large impact of variations in subthreshold causes read and write failures.
Half selected cells also experience disturb during a read/write operation which might corrupt their data.
SRAM Challenges

- Static margins are used as metrics
  - Performance is not a constraint for most IoT SoCs.
  - For high performance platforms, we are assuming DVFS.

- Two technologies were studied: Commercial 130nm and sub-20nm FinFET.
  - High-$V_T$ devices were used in the 130nm bit-cell.

- Monte-Carlo simulations at the worst case corner for each operation was performed.
SRAM Challenges

For 130nm bit-cell, write cannot be guaranteed below 0.8V and half select disturbs will occur below 0.8V.
For FinFET bit-cell, write cannot be guaranteed below 0.5V and half select disturbs will occur below 0.4V.
SRAM Challenges

Applying a write assist technique improves the write $V_{MIN}$ but not the HS $V_{MIN}$.
Current Approaches

- Using higher $V_{DD}$ for SRAMs,
- Using alternative bit-cell topologies,
- Using a read-before-write approach,
- Implementing banks with one word per row,
- Simultaneously applying a read assist technique with a write assist technique.
This talk...

- Write Assist Techniques
- Read Assist Techniques
- Combined Read/Write
Write Assist Techniques

- Assist techniques: WL boosting (BWL), NegBL, and Lowering Column $V_{DD}$ (LCV$_{DD}$)
- Assist was applied as a percentage of the $V_{DD}$.
- Impact on the Write Margin across $V_{DD}$.
- Impact on the Half Select Margins across $V_{DD}$.
For the 130nm bit-cell, high percentages of assist are needed to lower the write $V_{\text{MIN}}$ down to 0.4V.
Write Assist - WM

BWL provides the highest improvement in write margin at $V_{DD} > 550\text{mV}$
**Write Assist - WM**

LCV\textsubscript{DD} provides the highest improvement in write margin at V\textsubscript{DD} < 550mV
Write Assist - WM

(a) 130nm CMOS

(b) FinFET

The FinFET bitcell exhibits similar behavior but only 10% of assist is needed to reduce the write $V_{MIN}$ to 0.35V.
Write Assist - SNM

For 130nm bitcell, row HS $V_{MIN}$ is raised by BWL from 700mV to above 800mV.
Write Assist - SNM

(a) 130nm CMOS

(b) FinFET

For FinFET, BWL increases the row HS $V_{MIN}$ to 0.55V
Write Assist - SNM

For 130nm bitcell, applying 40% LCV\_DD increases the column HS V\_MIN to 0.75V.
For 130nm bitcell, applying 40% NegBL increases the column HS $V_{\text{MIN}}$ above 0.8V.
For FinFET bitcell, applying 10% NegBL or LCV\textsubscript{DD} degrades the margins but does not raise the V\textsubscript{MIN}
## Write Assist Summary

<table>
<thead>
<tr>
<th>(in mV)</th>
<th>130nm (40% WA)</th>
<th>FinFET (10% WA)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Write $V_{\text{MIN}}$</td>
<td>HS $V_{\text{MIN}}$</td>
</tr>
<tr>
<td>No Assist</td>
<td>&gt;800</td>
<td>700</td>
</tr>
<tr>
<td>NegBL</td>
<td>450</td>
<td>&gt;800</td>
</tr>
<tr>
<td>LCV_{DD}</td>
<td>400</td>
<td>750</td>
</tr>
<tr>
<td>BWL</td>
<td>400</td>
<td>&gt;800</td>
</tr>
</tbody>
</table>

- Write assist improves the write $V_{\text{MIN}}$ at the cost of HS $V_{\text{MIN}}$
- At low $V_{\text{DD}s}$, LCV_{DD} provides the highest improvement in the WM.
Read Assist Techniques

- Assist techniques: WL Underdrive (UDWL), NegBL, and Raising $V_{DD}$ ($RV_{DD}$)
- Assist was applied as a percentage of the $V_{DD}$.
- Impact on the Half Select Margins across $V_{DD}$.
- Impact on the Write Margin across $V_{DD}$.
For the 130nm bit-cell, high percentages of assist are needed to reduce the HS $V_{MIN}$ to 450mV.
For both bit-cells, $RV_{DD}$ shows the most improvement in the row HS $V_{MIN}$. 
Read Assist - WM

- For 130nm bitcell, Write $V_{\text{MIN}}$ is already above 0.8V.

- For FinFET bitcell, both read assist tech. degrades the write $V_{\text{MIN}}$, but UDWL shows more degradation
Read Assist Summary

- Read assist improves the HS $V_{\text{MIN}}$ at the cost of write $V_{\text{MIN}}$
- At low $V_{\text{DD}}$s, $RV_{\text{DD}}$ provides the highest improvement in the RSNM.

| (in mV) | Write $V_{\text{MIN}}$ | HS $V_{\text{MIN}}$ | Write $V_{\text{MIN}}$ | HS $V_{\text{MIN}}$
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>130nm (20% RA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No Assist</td>
<td>&gt;800</td>
<td>700</td>
<td>500</td>
<td>400</td>
</tr>
<tr>
<td>RV_{DD}</td>
<td>&gt;800</td>
<td>450</td>
<td>550</td>
<td>300</td>
</tr>
<tr>
<td>UDWL</td>
<td>&gt;800</td>
<td>500</td>
<td>650</td>
<td>300</td>
</tr>
<tr>
<td>FinFET (10% RA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Proposed Solution

<table>
<thead>
<tr>
<th></th>
<th>RV_{DD}-NegBL</th>
<th>UDWL-NegBL</th>
<th>UDWL-LCV_{DD}</th>
</tr>
</thead>
<tbody>
<tr>
<td>WL</td>
<td>No change</td>
<td>Under-driven</td>
<td>Under-driven</td>
</tr>
<tr>
<td>BL</td>
<td>Negative bias</td>
<td>Negative bias</td>
<td>No change</td>
</tr>
<tr>
<td>V_{DD} Boosted for Array</td>
<td>No change</td>
<td>No change</td>
<td>Lowered for column</td>
</tr>
</tbody>
</table>
NegBL improves the write delay but when high percentages of assist are used Row & Col. HS limit $V_{\text{MIN}}$
For 130nm bitcell, applying 10% $RV_{DD}$ with 30% NegBL reduces the array $V_{MIN}$ to 600mV.
Proposed - $RV_{DD}$-NegBL

For the FinFET bitcell, applying 15% RVDD with 40% NegBL reduce the $V_{MIN}$ down to 300mV.
UDWL-NegBL

Applying 10% UDWL will not reduce $V_{\text{MIN}}$.
Applying 20% UDWL will increase the $V_{\text{MIN}}$. 
UDWL-LCV<sub>DD</sub>

For 130nm bitcell, starting with 30% LCV<sub>DD</sub> applying 10% UDWL will reduce the write & HS V<sub>MIN</sub> but degrade the read V<sub>MIN</sub>
For FinFET bitcell, applying 10% UDWL will not reduce the write & HS $V_{MIN}$. Applying 20% UDWL degrades the write $V_{MIN}$. 
Summary

<table>
<thead>
<tr>
<th></th>
<th>Array $V_{\text{MIN}}$ (mV)</th>
<th>% lower $V_{\text{MIN}}$ vs. NA</th>
<th>% lower $V_{\text{MIN}}$ vs. WA</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>130nm CMOS</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed</td>
<td>600</td>
<td>&gt;25%</td>
<td>&gt;20%</td>
</tr>
<tr>
<td>[6][7]</td>
<td>650</td>
<td>&gt;19%</td>
<td>&gt;13%</td>
</tr>
<tr>
<td>[6]</td>
<td>650</td>
<td>&gt;19%</td>
<td>&gt;13%</td>
</tr>
<tr>
<td><strong>FinFET</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Proposed</td>
<td>300</td>
<td>40%</td>
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<td>[6]</td>
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<td>30%</td>
<td>13%</td>
</tr>
</tbody>
</table>

The proposed combination allows the most reduction in array $V_{\text{MIN}}$. 
Assist per Corner

- The worst case write corner is different than the worst case HS corner.
- Thus controlling the assist percentage by corner allows more improvement in $V_{\text{MIN}}$.

### 130nm bitcell

<table>
<thead>
<tr>
<th>Corner</th>
<th>NegBL</th>
<th>RV&lt;sub&gt;DD&lt;/sub&gt;</th>
<th>$V_{\text{MIN}}$ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT</td>
<td>10%</td>
<td>0%</td>
<td>450</td>
</tr>
<tr>
<td>SS</td>
<td>10%</td>
<td>0%</td>
<td>450</td>
</tr>
<tr>
<td>FF</td>
<td>0%</td>
<td>10%</td>
<td>450</td>
</tr>
<tr>
<td>SF</td>
<td>40%</td>
<td>0%</td>
<td>450</td>
</tr>
<tr>
<td>FS</td>
<td>0%</td>
<td>20%</td>
<td>450</td>
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</tbody>
</table>
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<tbody>
<tr>
<td>TT</td>
<td>10%</td>
<td>0%</td>
<td>300</td>
</tr>
<tr>
<td>SS</td>
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<td>0%</td>
<td>300</td>
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<tr>
<td>FF</td>
<td>10%</td>
<td>0%</td>
<td>300</td>
</tr>
<tr>
<td>SF</td>
<td>30%</td>
<td>0%</td>
<td>300</td>
</tr>
<tr>
<td>FS</td>
<td>10%</td>
<td>15%</td>
<td>300</td>
</tr>
</tbody>
</table>
Thank You!

Questions?
Backup Slides
At high $V_{DD}$s, the RSNM is most sensitive to PGL and PDR.
The RSNM is most sensitive to PGL and PDR at all voltages → BWL will negatively impact the RSNM.
The HSNM is most sensitive to changes in PDR and PUR at high $V_{DD}$s, but at low $V_{DD}$s PGR starts to play an important role.